

# Design of AMBA APB Protocol using Verilog

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**Abstract**— The AMBA (advanced microcontroller bus architecture) family of protocols includes the Advanced Peripheral Bus (APB) protocol. Tested design under test (DUT) creates a communication channel between the slave (design) and the master (testbench). Its design is predicated on a reusable system-on-a-chip (SOC) methodology, which is crucial to addressing the current VLSI challenges. APB is used to link all the peripheral devices to the bus architecture at a cheap cost, lower frequencies, and low power consumption.

The job entails creating and carrying out the APB protocol for read transactions with and without wait states, as well as single and multiple writes.

**Index Terms**— APB, AMBA, Verilog, Questa sim tool, communication

## I. INTRODUCTION

The AMBA protocol family includes APB. The AMBA specifications standards, which support technological independence and modular system design, are used in the design of superior integrated microcontrollers. An AMBA encourages the repurpose of peripheral devices to minimize the utility of infrastructure of silicon. Numerous protocols fall under the AMBA protocol, such as AXI, AHB, and APB.

Due to its optimization for lower power usage and interface intricate, it is referred to as a less expensive interface. The advanced peripheral bus, or APB for short, is a non-pipelined connection method for low frequency peripherals that don't need to utilize the AXI protocol. APB peripheral integration is as simple as connecting a signal transition to the clock's rising edge in a design flow. At least two cycles are required for each transfer (the setup and access cycles).

### A. Advance Peripheral Bus Block Diagram

The APB is created in accordance with the design specification. Figure 1 of the block diagram that follows shows the basic signaling of the APB.

### B. APB Signals

As illustrated in Figure 1, slave portion of the APB will receive the signals as inputs: PSEL, PWRITE, PRESET, PENABLE, and PCLK. It will output 32 bits of PRDATA. PWDATA and PADDR have 32-bit inputs as well. The signals of APB are explained in Table 1 below.

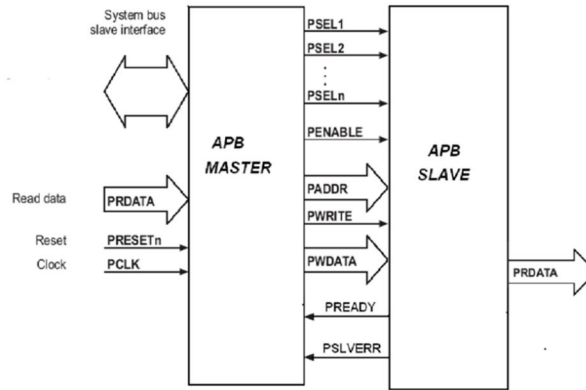


Figure 1: APB Master and Slave communication

TABLE I: APB SIGNALS

S.NO	SIGNALS	SIGNALS FUNCTION
1.	PCLK	APB operates along PCLK's pos edge.
2.	PRESET	Signal to reset
3.	PADDR	Address
4.	PSELX	select
5.	PWRITE	PWRITE=1 (write transfer) or PWRITE=0 (read transfer)
6.	PREADY	Slave is ready to accept data
7.	PENABLE	Enable signal
8.	PWDATA	Write data into slave address
9.	PRDATA	Read data from slave address.
10.	PSLVERR	Transfer error

## II. WORKING MODEL

FINITE STATE MACHINE (fsm) is used to operate the APB. The IDLE, SETUP, and ACCESS states are the three overall states. Every read or write transfer in APB requires a minimum of two cycles, for a SETUP phase, it takes one clock cycle and for the ACCESS phase, it requires another clock cycle. The subsequent transactions are finished in two clock cycles, while the initial transfer either write or read will require at least three clock cycles. The state transfer depicted in below figure

### A. State 1: Idle State

Idle state is the Default state. This condition denotes the absence of any operations. Initially, PSEL, PENANBLE, and PADDR signals will all be unknown (zero). If no transfer is required, idle status will be automatically asserted.

### B. State 2: Setup State

When a transfer is necessary, the setup state is in effect. This setup phase will assert the PSEL signal. This signal will wait for a start of the transfer and checks the availability of PADDR and PDATA. Only when a transfer is

required the bus will go into the setup phase; otherwise, it will stay in the Idle phase. In this phase, PWRITE, PADDR, and PWDATA are also delivered. After one clock cycle of setup, the bus will automatically transit to the final state i.e., ACCESS state on the next positive clock.

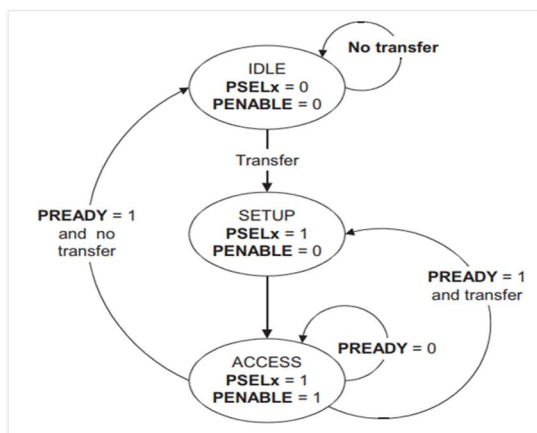


Figure 2: Operating state Diagram

### C. State 3: Access State

Mostly, ACCESS STATE condition is used to indicate that the transfer is finished. The PENABLE signal will go high (1) along with PSEL at the beginning of the ACCESS state, and all other signals, including PADDR, PWRITE, PSEL, and PWDATA, will stay stable as they were during the setup phase. One completed transaction is indicated when each PENABLE and PREADY have been declared high (1) in an access state. The bus enters the setup phase if more transfers are required; otherwise, it enters the default state or idle state.

## III. WRITE AND READ TRANSFERS OF APB

### A. Without wait state of Write Transfer

By default, during clock cycle T0, the bus will remain in the IDLE state. In the next clock cycle of T1 (setup phase), the signals PWDATA, PSEL, PADDR, and PWRITE will be asserted when a write transaction is required. The transaction starts at this point in the arrangement. The following clock T3 rising edge indicated by an assertion of high values for PENABLE and PREADY, indicates the conclusion of a single write operation in APB. As we previously stated, APB will need an absolute minimum of two clock cycles to perform each transaction. In the event that another transaction is required, the PENABLE signal will become zero and return to the SETUP state. PREADY signals is deasserted in tandem with the subsequent write transaction.

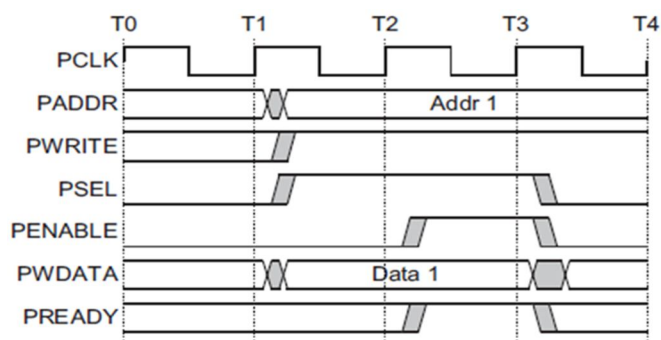


Figure 3: Wait state of Write Transfer

### B. Wait state of Write Transfer

In this instance, the PENABLE signal will stay high until PREADY is similarly declared high. Additionally, it won't proceed to the following write operation until PENABLE and PREADY have been confirmed. Consequently,

the first write transaction must require a minimum three clock cycles as a result of the figure 4 wait condition. The subsequent write transfer should typically take two clock cycles once this requirement is satisfied.

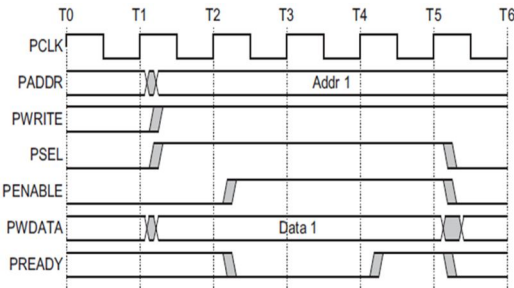


Figure 4: With wait state of Write Transfer

C. Without wait state of Write Transfer

A Read transaction will perform similarly to a write transaction. The Output PRDATA of slave is present at a specific address whenever the PADDR is present. The bus at T0 clock cycle will stay in IDLE state. When a read transaction is needed, the signals PSEL and PENABLE will assert high (1) and PWRITE will be de-asserted at the T1 clock edge (setup phase), accordingly. The start of the read transaction is indicated by this preparation phase. Additionally, On the approaching positive rising edge of T3 clock cycle, both PENABLE and PREADY will be asserted, signifying one read transaction in APB have been completed. As we previously mentioned, APB will need at least two clock cycles to perform each read transaction. In the event that another transaction is required, the PENABLE signal will become zero and return to the SETUP state. PREADY signals is de-asserted in tandem with the subsequent read operation.

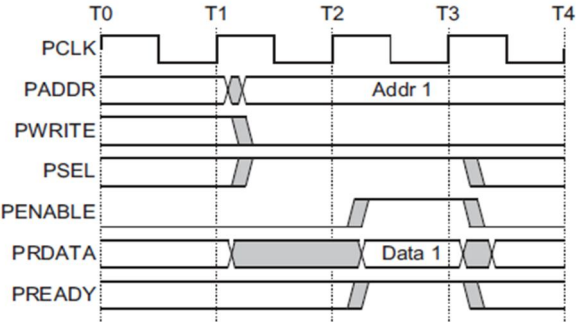


Figure 5: without wait state of Read Transfer

D. With wait state of Read Transfer

If Master wants to read any data from a particular address, PWRITE must be asserted LOW (0). To complete the read transfer in the T3 clock cycle, PREADY must be asserted high. Because of the wait statement in this instance, PENABLE will hold off until PREADY likewise claimed a high.

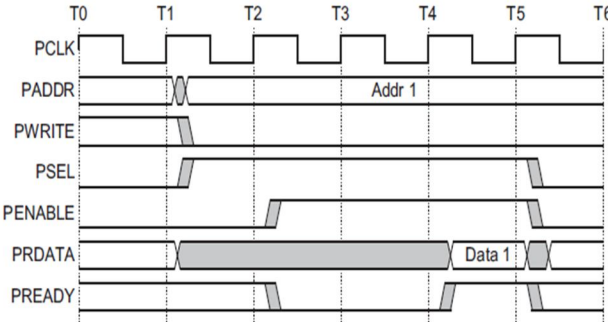


Figure 6: Read Transfer with wait state

#### IV. RESULT

- PRESETn signal is active low at T1 Clock cycle in order to reset the system.
- PSEL signal will be asserted at T2 Clock cycle.
- PENABLE will be asserted in the next Clock cycle of PSEL that is at T3 Clock cycle.
- When PWRITE is asserted, Master is ready to write the data in to the slave Register that is at T4 Clock cycle and also checks whether PSEL and PENABLE are asserted at the same T4 Clock cycle.
- The Address of the slave Register PADDR is taken as 24'h (8bits) and PWDATA is 81'h (8 bits).
- When the Slave is at T9 Clock cycle, it acknowledged to the Master that it is Ready to give the data by asserting PREADY signal. Thus, at the same Clock cycle Master can read the data as 81'h from Slave Register of Address 24'h.

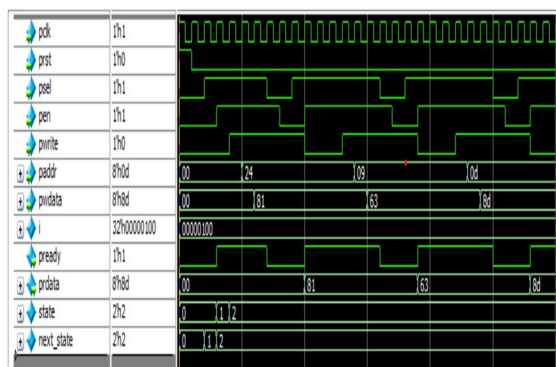


Figure 7: Waveform of Write and Read Transfer in APB

#### V. CONCLUSION

The APB protocol and the AMBA bus design are described in detail in this work. The specification stated above states that QUESTASIM is used for the design and verification of APB. The test case that we described here are the multiple write transactions without wait, and the multiple read transactions without wait. As a result, the system will be operated correctly. Additionally, QUESTASIM guarantees that design is functionally accurate.

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