AN ANALOG INTEGRATED CIRCUIT SENSOR FOR DETECTING THE NEGATIVE BIAS TEMPERATURE INSTABILITY EFFECT IN DEEP SUB MICRON MOS DEVICES

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ABSTRACT: Negative Bias Temperature Instability [NBTI] is an important reliability issue in Deep Sub Micron (DSM) MOS integrated circuits. NBTI cause shift in the threshold voltage of the PMOS devices when it is subjected to negative bias. With the increased use of analog mixed signal blocks in the present integrated circuits, an analog circuit based NBTI monitoring circuit finds significant scope in the design of sensor nodes to monitor the NBTI related issues and take appropriate control actions to minimize the effect. This article presents the use of analog circuits to monitor the effect of NBTI. The proposed circuits are more stable in operation as the signal current is not affected by the bias current of the circuits.

KEYWORDS: Negative Bias Temperature Instability, aging effect, Deep Sub Micron Design.

INTRODUCTION

Three analog Negative Bias Temperature Instability (NBTI) monitoring circuits are presented and the characteristics are verified using 65nm IBM 10RF_IBMFISHKILL model. Two common source amplifier based configurations and a common gate configuration is proposed for monitoring the NBTI effect. The two common source amplifier based configurations are having complementary behavior in the change in gain with respect to the change in threshold voltage and hence with respect to the NBTI effect. So either of the configurations can be used based on the requirement. The proposed circuits are more stable in operation as the signal current is not affected by the bias current of the monitoring circuits. Modern deep sub micron integrated circuits involve complex optimization involving multiple parameters such as area, power, speed and test ability. Traditional design approaches assume the device's electrical characteristics and physical properties are deterministic and do not change during circuit operation. In the design of deep sub micron circuits, new reliability concerns need to be addressed. NBTI is an important reliability issue which cause time based aging of the circuits[1]. NBTI cause an increase in the absolute threshold voltage, a degradation of the mobility, drain current, and transconductance of p-channel MOSFETs. It is almost universally attributed to the creation of interface traps and oxide charge by a negative gate bias at elevated temperature. Various NBTI models have been proposed, of which the Reaction–Diffusion (R–D) model is the most prevalent [2-5]. In this model, interface traps are generated at the SiO2/Si interface (reaction) with a linear dependence on stress time. The RD based model interprets the degradation process as a consequence of the interaction of inversion layer holes with hydrogen passivated Si atoms. When gate is under negative bias, the cold holes from the inversion layer can break the Si-H bonds to create interface traps and neutral H atoms. H2 molecules are formed by the neutral H atoms and can diffuse away from the interface (through oxide) or can anneal the existing traps. The increase in device Vt due to generated interface trap can be represented [6] as

$$\Delta Vt(t) = q\, N_{IT}(t)/Cox = f_{AC}(Sp) * K_{DC} * t^{n} \quad (1)$$

where N_{IT} is the density of the interfacial trap and Cox is the oxide capacitance. KDC is a technology dependent constant, which depends on temperature, Vdd, device geometry, oxide nitrogen concentration etc. Function f_{AC} represents the AC dependency of the process.

NBTI can affect the circuit performance over a period of time. The threshold voltage change of the devices can affect the timing of the circuits and may prevent the timing closure and thus lowering the maximum operating frequency. The noise margin of the circuits may also be affected by this phenomenon. On-chip sensor circuits can be used to accurately estimate the aging phenomenon. The output of the on-chip sensor circuits can be used as the control signals for the adaptive systems designed to overcome the performance degradation [7].

PREVIOUS NBTI MEASUREMENT TECHNIQUES

In the many previously proposed NBTI measurement techniques, emphasis has been given on monitoring digital integrated circuits. Various techniques proposed include delay locked loop based approaches[8], estimating the phase difference between the reference ring oscillator and the stressed one[9],[10]. A slew rate monitor circuitry is proposed in [11] to sense the NBTI effect. Other NBTI measurement techniques include the delay-element based approaches[12], deferentially sized inverter based techniques [13] and using the glitch detection circuits[14]. The presence of large number of analog mixed signal blocks in modern integrated circuits necessitates the development of analog-circuit based NBTI monitoring circuits. On-chip sensor circuits based on operational amplifiers detecting the changes in Vth to monitor NBTI effect is reported in [15] and a Common Gate Amplifier based circuit is proposed in [16].

PROPOSED NBTI MONITORING CIRCUITS

Three NBTI monitoring circuits are presented of which the Common Gate Amplifier (CGA) based configuration is an extension of the circuit reported in [16]. The proposed NBTI monitoring circuits are more stable in operation as the signal current is not affected by the bias current. The two Common Source Amplifier (CSA) based configurations and the one Common Gate Amplifier (CGA) based configuration presented exhibits piece-wise linear relation in gain when the threshold voltage is changed. The amplifier circuit's bias point is varied due to the NBTI effect of the stressed device, thus affecting the gain of the amplifier. The threshold voltage of the stressed device changes due to NBTI effect, while other devices used in the amplifier are not subject to NBTI effect. The two CSA configurations are having complementary behavior in the change in gain with respect to the change in threshold voltage. So either of the configurations can be used based on the requirement. The circuit’s characteristics are verified using 65nm IBM 10RF_IBMFISHKILL model obtained from MOSIS[17]. Before designing the NBTI monitoring circuits, the device characteristics of the 65nm IBM 10RF_IBMFISHKILL model are quantified using spice analysis and the device's change in threshold voltage to a change in substrate potential is analyzed. This property is made use in the spice analysis of the proposed circuits to analyze the circuit behavior when there is a change in threshold voltage of the device due to NBTI effect.

NBTI monitoring circuit 1

An NBTI monitoring circuit based on Common Source Amplifier (CSA) is presented in Fig1. In the circuit, PMOS device M3 alone is susceptible to NBTI effect. The effect of the change in threshold voltage of the device M3 on the amplifier gain is observed. A bulk potential sweep of

0.4VDC to 1.4Volt DC is used to study the effect of threshold voltage change of device M3 on the amplifier gain. The piece-wise linear relation in gain of the amplifier is represented in Figure2 due to the threshold voltage change.

CIRCUIT PARAMETERS OF THE NBTI MONITORING CIRCUIT
Device model: 65nm IBM 10RF_IBMFISHKILL
Spice level: 54
Operating voltage (Vdd) : 1.2V DC
M1, M2: NMOS devices
M3: PMOS device
PMOS and NMOS W/L: 10/0.07 um
RD: 3KΩ, RS: 500E, RB1:10KΩ, R1: 50E
v(vdu): Drain potential of the MOS device M1
v(ng): Gate potential of the MOS device M1
v(nb): Bulk potential of the MOS device M1
vdu and vgp: dummy voltage sources to facilitate measurement of current

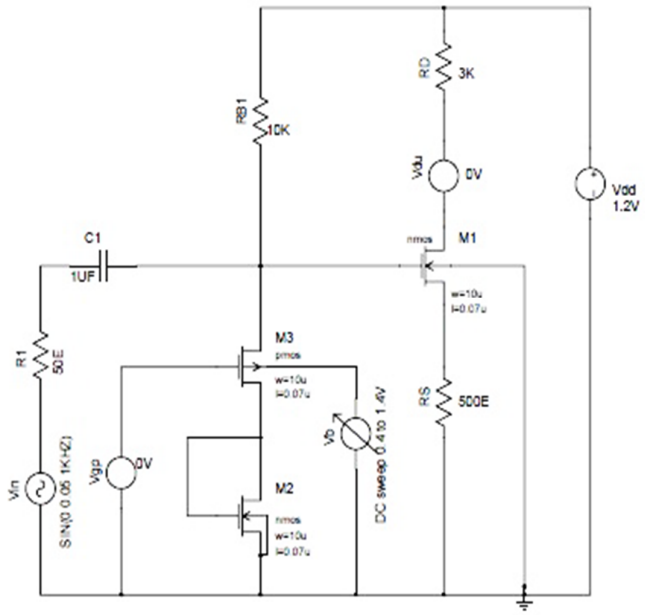

Figure 1. Common Source Amplifier based NBTI monitoring circuit

NBTI monitoring circuit 2

Fig. 3 shows a Common Source Amplifier based NBTI monitoring circuit which has the complementary behavior of the circuit represented in Fig1. In this configuration, the PMOS device M3 is susceptible to NBTI degradation. The effect of the change in threshold voltage on the circuit is analyzed using a dc sweep voltage of 0.4DC to 1.4V DC and the gain variation is shown in Fig 4.

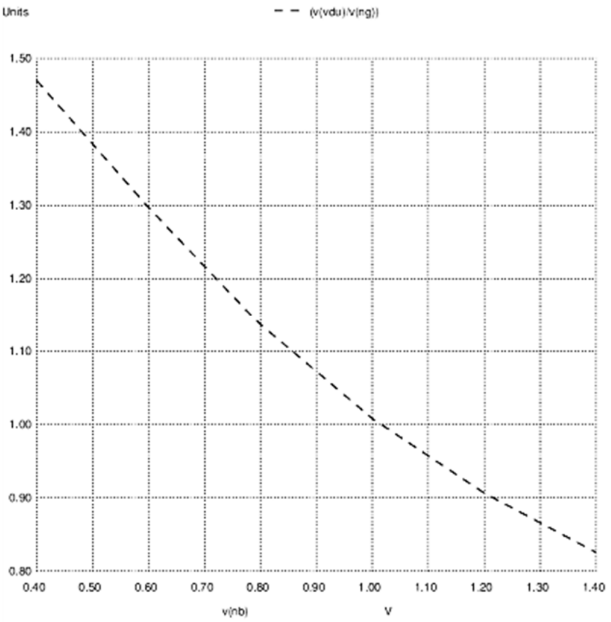

Figure 2. Plot (v(vdu)/v(ng)) vs v(nb) of the circuit shown in Fig. 1

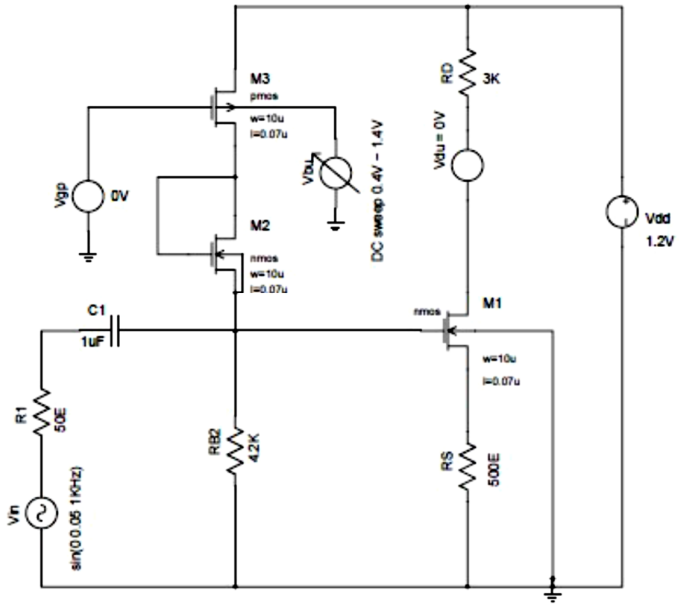

Figure 3. Common source amplifier based NBTI monitoring circuit

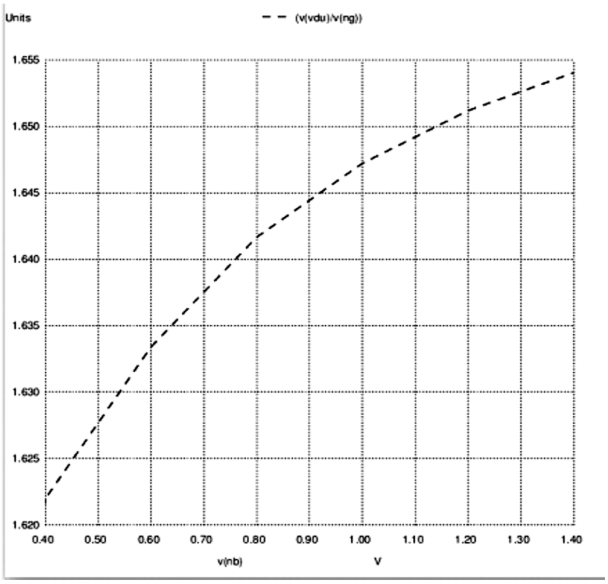

Figure 4. Plot of v(vdu)/v(ng) vs v(nb) of the circuit shown in Fig. 3

NBTI Monitoring Circuit – 3

A Common Gate Amplifier based NBTI monitoring circuit is shown in Fig 5. This amplifier configuration is an improved version of the one reported in [16]. In this configuration the PMOS device MP1 is susceptible to NBTI degradation. The change in gain due to the effect is represented in Fig 6. which shows the voltage gain reduction when the device MP1 is subjected to NBTI effect.

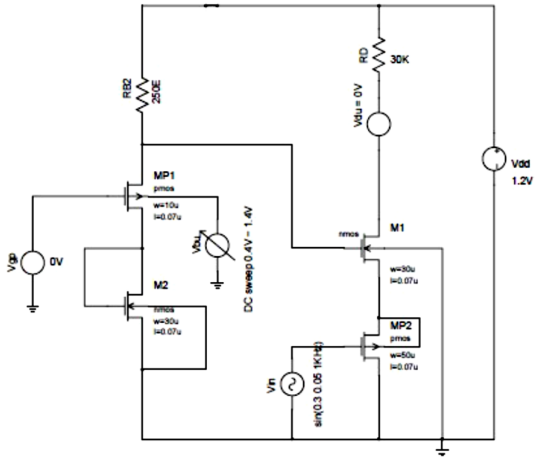

Figure5: Common gate amplifier based NBTI monitoring circuit

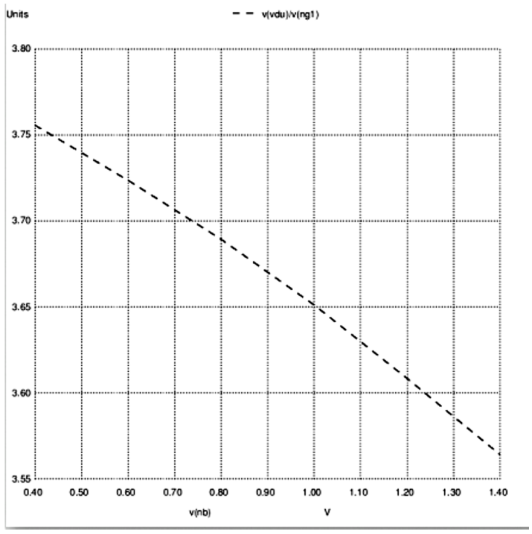

Figure 6: Plot of v(vdu)/v(ng) vs v(nb) of the circuit shown in figure 5

CONCLUSION

Two common source configurations which are having complementary behavior in gain when subject to NBTI effect and a common gate configuration is described in this work. Any of the configurations can be used to monitor the NBTI effect based on the requirement of the processing logic which follows the sensing circuit. Even though the change in gain is not exactly linear throughout, the circuit can be operated in the linear regions of the response. Additional linearizing circuits can be designed to make the change in gain linear with respect to the change in threshold voltage. The circuits proposed can be used as the nodes for detecting the aging effect in an integrated circuit and need to be distributed effectively.

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