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Encoding Schemes For Power Reduction In Noc Links:A Review

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***Abstract*— This paper reviews different encoding schemes for reduction of power dissipation, crosstalk noise and delay. As the number of cores in a chip increases, the role played by the communication system becomes more crucial. An on-chip communication infrastructure based on the Network-on-Chip (NoC) paradigm is today recognized as the most effective and scalable solution. Amongst the communication resources, as technology shrinks, the power ratio between NoC links and routers increases making the links becoming more power hungry than routers. Crosstalk is increased by enhanced switching activity which is often main cause for the malfunctioning of any VLSI chip. Consequently, delay and power dissipation also increases due to enhanced crosstalk. Reduction in switching activities through coupled transmission line results in enormous reduction of power dissipation, crosstalk and delay. The researchers therefore often concentrate on encoding schemes that reduces the transitions of the signals. This paper reviews all such encoding schemes.**

***Index Terms*— NoC , VLSI, SoC, IP.**

I. INTRODUCTION

In current nanoscale technology power dissipation, propagation delay and crosstalk performance of interconnects determines the overall performance of a chip, and on chip communication is currently the most prominent bottleneck in scaling SOC complexity. A system on a chip is an integrated circuit(IC) that integrates all components of a computer or other system into a single chip. It may contain digital, analog, mixed signal processing and often radio frequency functions all on a single chip substrate. SoCs are very common in the mobile electronics market because of their low power consumption. To meet the growing computation intensive applications and the needs of low-power, high-performance systems, the number of computing resources in single chip has enormously increased. Current VLSI technology can support such an extensive integration of transistors by adding many computing resources such as CPU, DPS and specific IPs etc... to build a system in system on chip which has increased the interconnection challenges issue, by the end of the decade SoCs using 50nm transistors operating below one volt will grow to 4 billion transistors running at 10GHz according to the international Technology Roadmap for Semiconductors. In multicore era as number of cores increases significantly on SoC, communication system also needs to change to support multi core communication. NoC is solution to scalability issue of future many core systems. Several Network on chip (NoC) architectures have been proposed to solve the problem of communication in complex SOC. Propagation delay across long on chip buses is becoming a limiting factor in high speed designs. Crosstalk

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resulting from interaction of electromagnetic fields generated by neighboring data signals as they propagate increases the delay and the power dissipated by the links of a network-on-chip (NoC) and starts to compete with the power dissipated by the other elements such as the routers and the network interfaces (NIs). The scalable and modular nature of NoCs and their support for efficient on-chip communication lead to NoC-based system implementations. In recent years, there has been an evolving effort in error detection and correction mechanisms in the communication subsystem, and crosstalk avoidance codes (CACs) are considered as effective way to reduce the mutual inter-wire coupling capacitance and hence the energy dissipation of wire segments. To increase the reliability of system, the crosstalk avoidance and error detection scheme has become the critical issues in Network on Chip (NoC) design. Dynamic power dissipation in interconnects is a major contributor to power consumption in NoC links. This is mainly due to two factors, self-switching activity of the particular link and coupling switching activity among adjacent links. Dissipation of power is due to the switching activity both self and coupling induced by subsequent data patterns traversing the link. The interconnection network dissipates a significant fraction of the total system power budget.

II. Related Work

Authors in paper [1] proposed An encoding scheme which aimed at minimizing the power dissipation on serial links. They proposed scheme called adaptive low power transmission coding (ALPTCS) which switches between 2 coding schemes when data pattern changes. The efficiency was checked with 2 multimedia applications. Results showed that method adapts to more data patterns and is suitable for serial communication in NOC.It was also observed that the proposed scheme offered area overhead of ALPTCS codec about three times than that of SILENT(serialized low energy transmission coding),the transitions reduction is noticeably significant. It was concluded that ALPTCS is superior to SILENT in reducing transitions, and is almost 2.5% to 8.4% better than SILENT. Future enhancement of this work could be that the proposed method can be used for SoCs and NoCs in nanoscale era where the power dissipation as a prime regard. Authors in paper[2] proposed a routing algorithm with permanent faults in 2-D mesh networks. The approach discussed was adaptive and distributed with no extra circuitry or routing tables for operation.It also included deadlock handling for robust system operation.The alogorithm was demonstrated using a 6*6 2D mesh for simulation.The number of sources taken into account were 25 and destinations 10. Initial in network under zero faults is 81.5 clock cycles.Latency increases with the link fault rate.Authors also discussed throughput of the network. Results showed a 100% throughput when at least one path exists to destination.Throughput becomes zero when the link fault is 95%.

Authors in paper [3] proposed to achieve a low-power network-on-chip (NoC). The area of the asynchronous switch is increased by 25% as compared to the synchronous switch. The power dissipation of the asynchronous architecture could be decreased by up to 55%. Even though clock gating is used, the asynchronous design achieves significant power reduction of 28%. The total metal resource required to implement the asynchronous design is decreased by up to 12%. As technology advances and network density increases, the reduction in power

dissipation reaches 22% for 256 IPs with the same chip size. The asynchronous butterfly fat tree (BFT) architecture dissipates the minimum power as compared to other NoC topologies.

Authors in paper [4] proposed method of gray code input helping for better power analysis As gray codes have a change of only one bit at a time the power consumed is less at input side. In this work, the gray encoding technique was implemented for reducing the transition activity in the NOC. The gray encoding scheme used here was aimed at reducing the power dissipated by the links of an NOC. In fact links are responsible for a significant fraction of the overall power dissipated by the communication system. The proposed encoding schemes were agnostic with respect to the underlying NOC architecture in the sense that our application does not require any modification neither in the links nor in the links. The coding was done in VERILOG language and its power is calculated using Xilinx software. Output was simulated and synthesized using Modelsim software. In the future, the Network on Chip (NOC) implementation using different types of router technique can be analyzed. Comparison on many encoding techniques such as gray encoding techniques can be analyzed in which the area, delay, power and the performance of the NOC will be investigated and use for high speed applications. Author paper [5] demonstrated a generic framework which allows efficient implementations of crosstalk avoidance codes. The main feature of the proposed approach is

based on the partial coding concept. Quantitative analysis performed in 32nm technology which shows that substantial savings in area and energy costs can be obtained using the proposed technique when compared with the existing coding solutions or conventional methods such as shielding and repeater insertion. Partial coding algorithm was proposed to allow area and energy efficient implementation of crosstalk avoidance codes. Quantitative analysis in 32nm technology has shown that the proposed approach can achieve in most cases with the same bus speed but with lower energy and area overheads compared to existing coding schemes, like shielding and repeater insertion. The current technology scaling trend leads to more crosstalk noise. Therefore it is anticipated that the proposed partial coding approach will play an increasingly important role in achieving the speed requirement at low area and energy costs.

Authors in paper [6] incorporated joint crosstalk avoidance and double error correction coding to the present works done by various authors. It is possible to simultaneously enhance the reliability of the NOCs and lower the energy dissipation, despite the associated redundant wires and codec logic requirements. As verified by the author through detailed analysis and simulations, they proposed CADEC scheme which lowers the energy dissipation compared to all other existing schemes studied here. The packet length was assumed to be 16 flits. Simulations were performed assuming 130 nm technology nodes. The channel BER is assumed to be 10−20 [30] in these simulations. The energy savings arise from two factors, namely the possibility of lowered voltage swing, and reduction of mutual switching capacitance of the inter-switch wire segments. From the analysis carried out in their work, it can also be concluded that coding schemes with higher order correction capability outperform sole retransmission-based mechanisms in terms of energy and area overhead. In future Author suggested that higher order error correcting codes will be more area efficient than retransmission-based mechanisms.

Authors in paper [7] proposed the concept of using data encoding to mitigate crosstalk delay on buses. Authors presented a practical framework for understanding crosstalk immune coding. The encoder and decoder proposed in paper reduce crosstalk delay about 14% to that of available techniques. Future work proposed by the author was that research should be done so as to design an efficient encoder and decoder to reduce crosstalk in on chip buses.

Authors in paper [8] compared the topologies of different benchmarks synthesized by using four different methods. The algorithm proposed in paper was Rectilinear Steiner Tree (RST) and the algorithm proposed was without using a shared bus. Experimental results showed that the proposed algorithm performs better than CosiNoC and that the Rectilinear-Steiner-Tree-based method in most of the cases was used. The reasonable explanations were 1) the solution space of the algorithm is not limited by a fixed type of structure; 2) The power reduction is guaranteed after each refinement; 3) Algorithm is A Tree based, which results in smaller latency.

Authors in paper [9] considered only two adjacent bits of the physical channel. Sixteen different combinations the encoding technique is implemented for reducing the transition activity in the NOC. The encoding scheme was aimed at reducing the power dissipated by the links of an NOC and that the schemes were agnostic with respect to the underlying NOC architecture in the context that our application does not require any modification neither in the links nor in the links. The proposed architecture was coded using VERILOG language and is simulated and synthesized using Modelsim and Xilinx software. Overall, the application scheme allowed 40% power saving and with less than 5% area overhead in the NI compared to other data encoding scheme. Future work of the paper was that Network on Chip (NOC) implementation has to be done using different types of router and network interface technique and should analyze the area, delay and power with previous techniques for enhanced results.

Authors in paper [10] focused on a unified codec scheme for reduction of area and crosstalk in RC and RLC modeled interconnects using both bus encoding and shielding insertion technique to detect the various types of crosstalk couplings with the semi-custom and full-custom design implementations. All the possible cases of crosstalk were implemented and tested using Spartan3 FPGA kit and Cadence Analog Virtuoso Design Suite. Power analysis was done using the Xpower tool of Xilinx ISE Suite for semi-custom design. The power & time delay calculations are performed for same codec scheme using Visualization & Analysis XL Calculator provided in CadenceSpectre tool for full custom design in 0.18µm CMOS technology.

III. Conclusion

Most of power is dissipated by links, routers and NI. In all the papers they focused on the power reduction by using encoding technique. Out of the different coding techniques compared in Table 1 adaptive technique gives a maximum of 8-60%reduction in overall switching activity.

IV. Future Work

Coding schemes with higher order correction capability outperform sole retransmission-based mechanisms in terms of energy and area overhead. Future work includes the evolution of coding schemes in NoCs is implemented using state of the art technologies, where the power consumption of channels becomes more relevant due to relevant increase in wire capacitance. Use of multiple coding schemes need to be done for better matching and reduction of the transition activity patterns.

TABLE 1: COMPARISON OF DIFFERENT ENCODING SCHEMES

Sl. No	Ref Paper	Year	Methodology Proposed	Results
1	Paper [5]	2015	Partial coding	40% area saving and crosstalk reduction
2	Paper [4]	2015	Gray coding technique	Reduced power consumption due to gray coding up to 30%
3	Paper [9]	2015	Encoding of adjacent bits only	40% power saving with less than 5% area overhead
4	Paper [10]	2013	Bus encoding	Reduced crosstalk couplings
5	Paper [1]	2012	Adaptive low power transmission coding	8-60% reduction in switching activity
6	Paper [2]	2011	Adaptive fault tolerant routing for 2D mesh	100% throughput for atleast one path
7	Paper [3]	2015	Asynchronous butterfly fat tree coding	Metal source reduces up to 12%, 28% power reduction for 256 IP
8	Paper [7]	2011	Data encoding to mitigate cross talk delay on buses	Reduced crosstalk about 14%
9	Paper [8]	2011	CosiNoC rectilinear steiner tree (RST)	Reduced latency effect
10	Paper [9]	2007	CADEC (cross talk avoidance double error correction codes)	Lowered voltage swing and reduction of mutual switching capacitance

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