SUB THRESHOLD DUAL MODE LOGIC FOR ULTRA LOW POWER APPLICATIONS

M. MAHABOOB BASHA
AVR & SVR College of Engineering & Technology, Nandyal, JNTUA, A.P, India
mmehboobbasha@gmail.com

K. VENKATA RAMANAIAH
YSR Engineering College, Yogi Vemana University, Kadapa, A.P, India
ramanaiahkota@gmail.com

P. RAMANA REDDY
JNTU College of Engineering, Department of ECE, JNTUA, Anantapur, A.P, India
prrjntu@gmail.com

R. SINDHU
AVR & SVR College of Engineering & Technology, Nandyal, JNTUA, A.P, India
chinnureddy452@gmail.com

ABSTRACT: Sub-threshold is a new paradigm in the digital VLSI design today. Circuits which operate in the sub-threshold region use a supply voltage that is close to or less than the threshold voltages of the transistors, so that there is a significant reduction in both dynamic and static power consumption. Leakage currents have become important sources of power consumption in modern nano scale CMOS integrated circuits. This paper acquaint with new logic family called dual mode logic, designed to operate in sub threshold region. The proposed DML logic topologies can be switched between static and dynamic modes of operation based on the system requirements. It allows operation in two modes (Dual mode), very fast in the dynamic mode while energy efficient in the static mode. This can be achieved with a simple design principle. Overall power consumption can be reduced by using sub threshold operating region. Power consumption of DML based gates are compared with conventional gates. The tanner EDA tool briefly discusses simulation results.

KEYWORDS: Dual mode logic (DML), Sub threshold, Low Power.

INTRODUCTION

Due to advancement in technology and the extension of mobile applications, power consumption is one of the considerations in VLSI digital design [1]. High on-chip temperature caused due to larger power consumption resulted in reduced operating life of the chip and battery life. The low power requirement of the CMOS based circuits has been satisfied by introducing sub-threshold logic which involves voltage scaling below the device threshold. Hence Digital sub-threshold circuit design is one of the main focus areas for low power to ultra-low power applications [1],[2]. Utilization of a supply voltage (VDD) which is less than the threshold voltages of the transistors, in circuits, which operates in the sub threshold region, made a notable scaling down of both dynamic and static power. However, a belligerent scaling of supply voltage inversely affect performance and a much larger sensitivity to process variations and fluctuations in the temperature

[3]. One of the most common logic family used for sub-threshold operation currently is the Complementary Metal Oxide Semiconductor (CMOS) logic family.

Ultra low Voltage operation originally introduced in 1972 [4], was originally used for low throughput applications like sensors, wrist watches and biomedical devices [5]. By maintaining low to moderate performance, it gives low power dissipation. In 1970's, Dynamic logic, termed as domino logic, has been widely used for high-performance applications. However, due to known problems of dynamic gates such as charge sharing, susceptibility to glitches and to cross talk noise, and sensitivity to process variations in nano scaled technologies have prevented utilization of Domino logic in low voltage designs [6].

Here a novel low power subthreshold dual mode logic (DML) family have been introduced and designed for operation. The proposed DML logic topologies can be switched between two modes of operation: static CMOS like mode and dynamic np-CMOS-like mode (referred as a dynamic mode) as shown in Figure 1. The DML logic gate has very low-power dissipation with moderate performance in static mode, and higher performance in the dynamic mode of operation, at the expense of improved power dissipation. This specific feature of the DML gives the provision to control system performance on-the-fly and accordingly supports the application with a flexible workload which is needed.

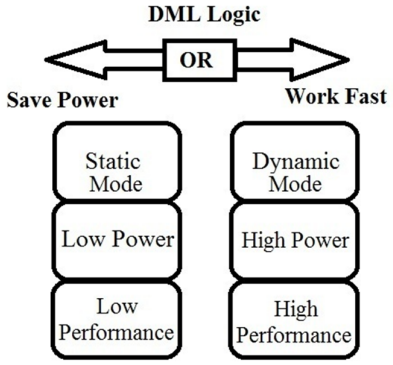

Figure 1. Static and Dynamic modes of operation.

High immunity to process variations helped Dual mode logic gates to operate from a supply voltage as low as 300 mV. Simulations were performed on basic NAND gates, indicate that while operating in the dynamic mode, sub threshold DML achieves an improvement in speed of up to 10× compared to a standard CMOS, while dissipating 1.5× more power. In the static mode, a 5× reduction of power consumption is achieved, compared to a basic domino, at the price of a magnitude degradation in performance. Tanner simulations of DML represent a drastic enhancement in performance when comparing to domino logic. Section II introduces the reader to DML overview and operation methods. A comparison of energy dissipation, DML speed and robustness with Complementary Metal Oxide Semiconductor and dynamic logic are elaborated. Comparative performance analysis through simulations describes in section III, section IV presents simulation results and discussions on the proposed gates. Section V concludes this paper.

DML STRUCTURE AND PRINCIPLE OF OPERATION

The primary DML gate architecture is inclusive of a standard CMOS gate and an additional transistor M1, whose gate is connected to a global clock signal, as shown in Figure 2. This architecture looks similar to the noise tolerant pre charge (NTP) structure, introduced by Yamada et al. [7]. But, in contrast to the NTP, which was developed as a high-speed, high-noise-tolerance dynamic logic, the DML targets to operate in two operating modes namely static mode and dynamic mode.

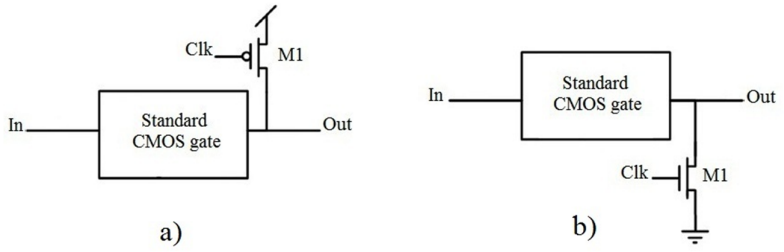

Figure 2. DML Topology (a) Type A un-footed. (b) Type B un-footed

The Clk is equipped with an asymmetric clock, in dynamic mode operation, which allows two distinct phases: pre charge and evaluation. The output is charged to high/low, Based on the topology of the DML gate, the output is charged to high/low throughout the pre charge phase. The output is analysed and calculated based on the values obtained at the gate inputs during evaluation phase. Our proposed DML topologies, termed Type A and Type B, are illustrated in Fig. 2. Type A is characterized by an addition of p-MOS transistor which, on pre charge phase, pre charges the output to a logical "1".Addition of n-MOS features Type B, on precharge phase, pre charges the output to a logical "0." Implementation of dynamic logic gates makes use of a footer, which needs an extra transistor. The footer eliminates the ripple effect of the data propagating through the cascaded nodes thereby decrease pre charge time and also allows faster pre charge. Switching the DML gate to function in CMOS like (i.e., static mode) operation is fairly instinctive: The global Clk should be fixed constantly low for Type B topology and high for Type A topology. Thus, the gate accomplishes similar topology to CMOS, aside from the negligible extra parasitic capacitance. Implementing a DML node based on a CMOS gate is as follows: for the pre charge phase an additional transistor is "glued", and, in footed gate scenario, In Type A gates, an extra n-MOS transistor gets added as footer and a p-MOS transistor as a header in Type B gates.

DML nodes which operate in dynamic mode possess many merits over traditional dynamic nodes which inherited from DML topology. It has distinct potential to shift between various operations modes. The DML genetically characterizes an active keeper made from the CMOS complementary logic. It is acquired from the node structure which consists of fully functional CMOS part, and also supports in retaining the output level. This vital constraint to the immunity to temperature fluctuations, process variations and resolving domino's popular disadvantages such as crosstalk noise, charge sharing and susceptibility to glitches, which escalates with voltage and process scaling.

While designing a DML gate, the design methodology used is to fix the pre charge transistor in parallel to the stacked transistors. As a result, evaluation is done based on the parallel transistors thus makes it faster. The stacked transistors will be aligned to very low widths so as to reduce intrinsic capacitances, expanding dynamic operation performance over decreased static operation performance. This principle also reduces power dissipation when compared to conventional CMOS gates. The pre charge transistor is also kept at minimum size so as to reduce leakage currents during evaluation and static operation.

The gates can be designed either of topologies(Type A or Type B), neglecting the above mentioned optimization guidelines. The ideal design methodology while designing with DML gates is to cascade connects Type A and Type B gates, exactly like in np-CMOS gates. This type of design methodology is characterized by minimize area , maximum performance and maximum power efficiency, it is possible to connect same types of gates by making use of an inverter buffering between them, as done in the dual mode logic. Same types of gates can be connected without inverters when a header/footer is used at each stage, however, after the ends of precharge, glitches were present until the evaluation data ripples through the chain. These are basic common challenges when designing with dynamic gates [11]. The DML's inherent keeper allows to recover the logical value when compared to the standard dynamic logic.

COMPARATIVE PERFORMANCE ANALYSIS THROUGH SIMULATIONS AND MEASUREMENTS

Comparison of DML topologies to their CMOS and domino counter parts by power as a constraint with NAND gate have been simulated and analysed. The power is calculated by simulating conventional NAND with different DML topologies in Tanner EDA 13.0

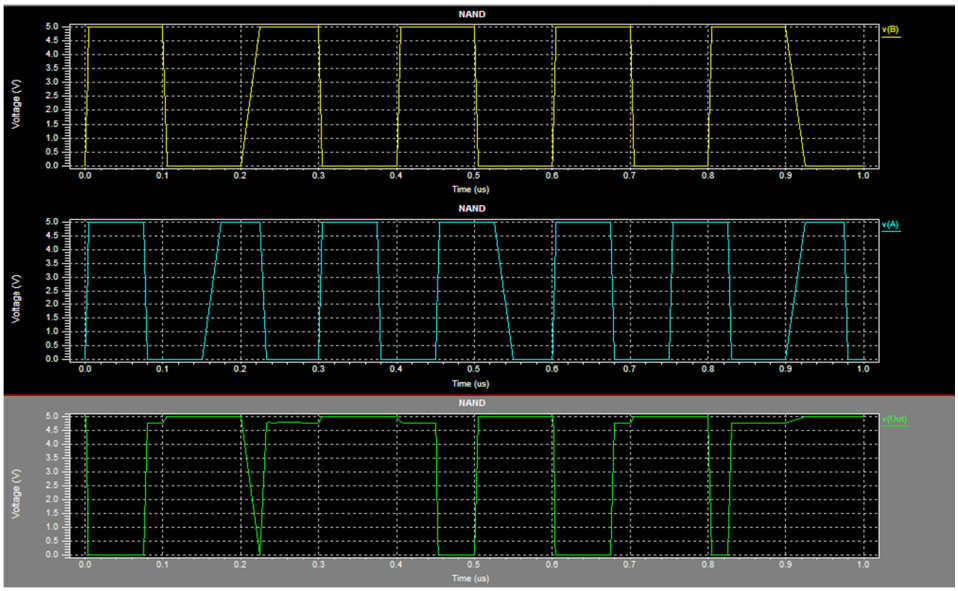

Figure 3: Power Output of 2-input conventional NAND gate

The power output of conventional 2 – input NAND is calculated using tanner and shown in Figure 3. The average power is 2.879674e-004w.

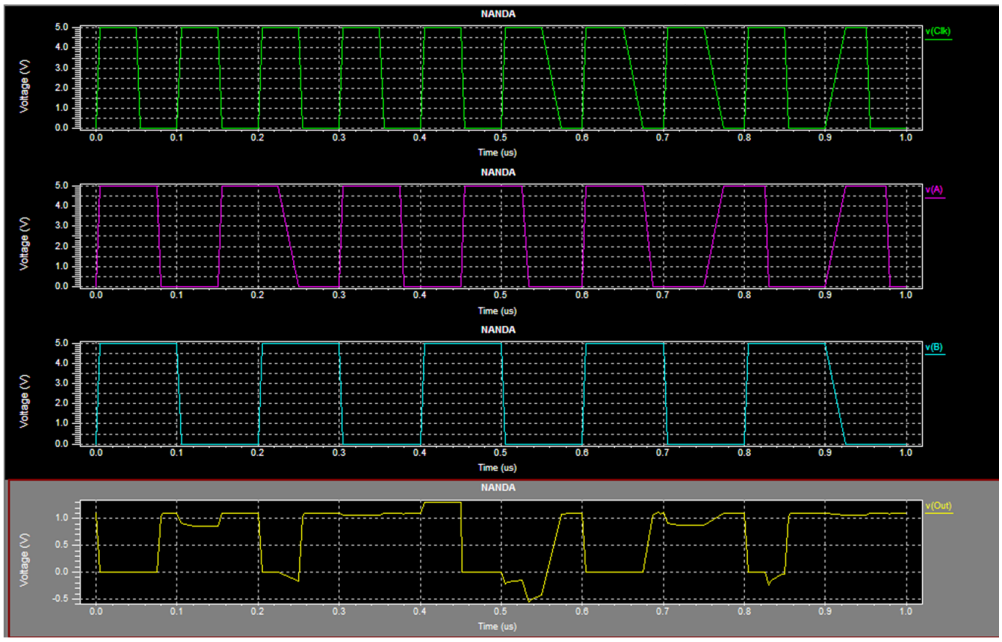

Figure 4. Power output of un-footed DML Type A Topology NAND gate.

The power output of an un-footed DML Type A topology 2- input NAND gate is shown in Figure 4. The average power calculated is 1.297666 e-007w, hence the power consumption is reduced.

The power output of an un-footed DML Type B topology 2- input NAND gate is shown in Figure 5.The average power calculated is 8.207475 e-005w, hence the power is decreased.

The power output of 2-input NAND gate with header and footer switch is shown in Figure 6. The average power calculated is 7.712058e-006w, hence the power is lowered.

SIMULATION RESULTS AND DISCUSSION

In this section, the results on the benchmark circuits have been presented for the existing and proposed styles.

The simulation results of conventional NAND gate with DML topologies NAND gate with Tanner EDA tool have been obtained. From the simulated results shown in table I, it has been observed that DML based NAND gate offer better performance in terms of reduced power consumption.

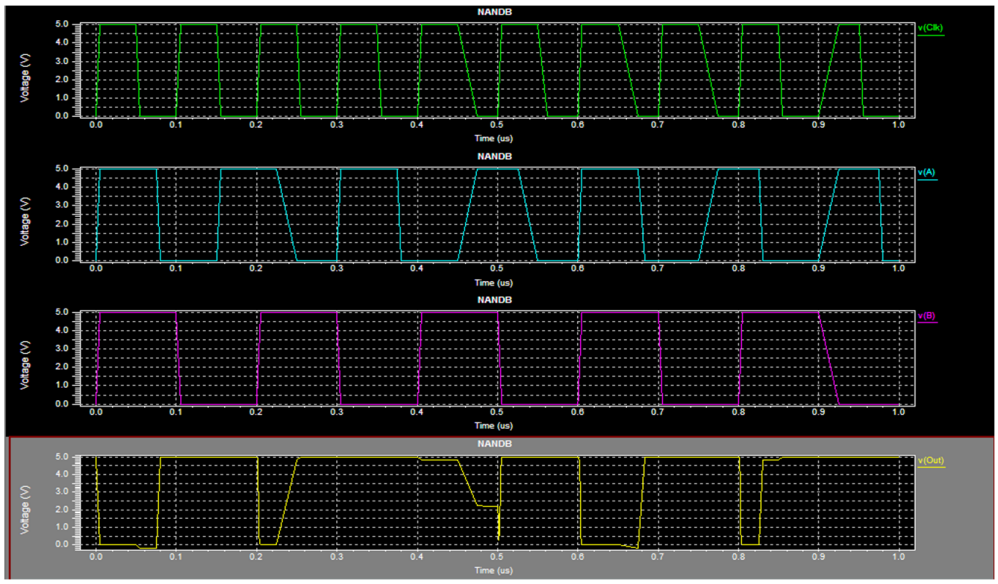

Figure 5. Power output of un-footed DML Type B Topology NAND gate.

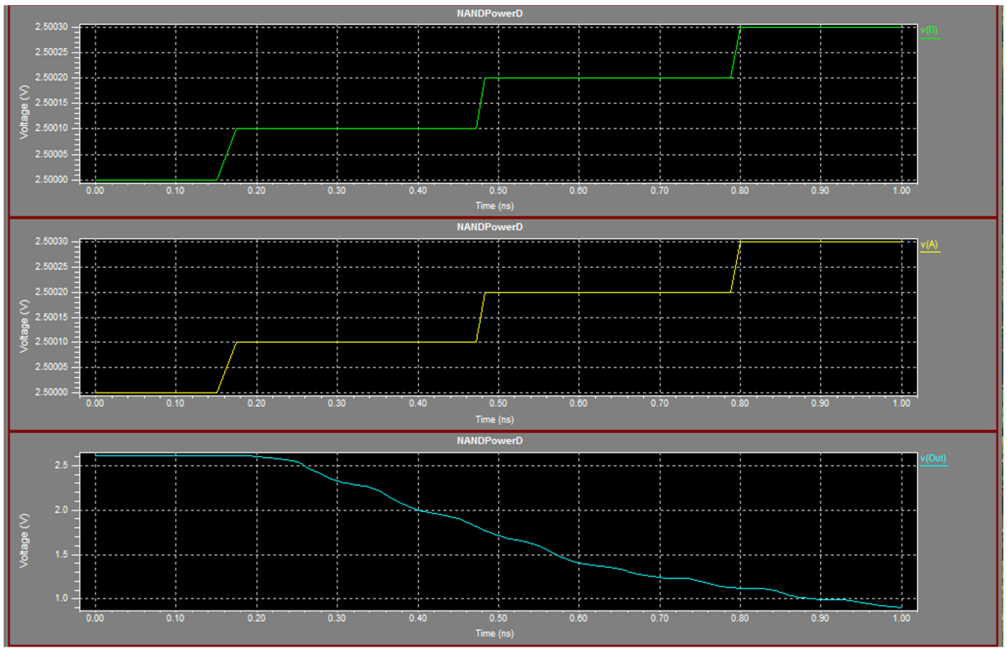

Figure 6. Power output of 2 input NAND with header and footer switch

Table 1. Power Consumption

Logic	Circuit	Average Power Consumption
Conventional	NAND	(2.879674e-004)W
DML Type A	NAND	(1.297666e-007)W
DML Type B	NAND	(8.207475e-005)W
Proposed	NAND	(7.712058e-006)W

CONCLUSION

In this short article, a novel DML family for sub threshold operation have been explained. When compared to CMOS, DML dynamic mode resulted an average 10× speed enhancement and better robustness when compared to a standard dynamic logic. The DML static mode illustrated the lowest energy dissipation: 2.2× less than CMOS on average, and 5× less than the domino. Dual mode logic was considered as an energy efficient compared to standard CMOS logic. Future work will include the optimization of the Dual mode logic gates for operation with standard supply voltages with different stacking power gating techniques.

REFERENCES

D. Markovic, C. C. Wang, L. P. Alarcon, and J. M. Rabaey, "Ultralowpower design in near-threshold region," *Proc. IEEE*, vol. 98, no. 2, pp. 237–252, Feb. 2010.

M. Alioto, "Ultralow power VLSI circuit design demystified and explained: A tutorial," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 1, pp. 3–29, Jan. 2012.

N. Verma, J. Kwong, and A. P. Chandrakasan, "Nanometer MOSFET variation in minimum energy subthreshold circuits," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 163–174, Jan. 2008.

R. Swanson and J. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," *IEEE J. Solid- State Circuits*, vol. 7, no. 2, pp. 146–153, Apr. 1972.

B. Zhai, L. Nazhandali, J. Olson, A. Reeves, M. Minuth, R. Helfand, S. Pant, D. Blaauw, and T. Austin, "A 2.60 pJ/Inst subthreshold sensor processor for optimal energy efficiency," in *Symp. VLSI Circuits, Dig.Tech. Papers*, *ISBN*:1-4244-0006-6, pp. 154–155, 2006.

H.Soleman, K.Roy, and B.Paul, "Sub-domino logic: Ultralow power dynamic sub-threshold digital logic," in *IEEE Proc. 14th Int. Conf. VLSI Design, ISSN : 1063-9667*, pp. 211-214, 2001.

H. Yamada, T. Hotta, T. Nishiyama, F. Murabayashi, T. Yamauchi, and H. Sawamoto, "A 13.3 ns double - precision floating-point ALU and multiplier," in *Proc. IEEE Int. Conf. Comput.Design: VLSI Comput. Process.*, Oct. 1995. pp. 466-470.

B. H. Calhoun, A. Wang and A. P. Chandrakasan: "Modeling and sizing for minimum energy operation in Sub threshold circuits", in *IEEE J. Solid-State Circuits*, vol. 40, no.9, pp. 1778-1786, 2005.

M. Mahaboob Basha, Towfeeq Fairooz, Nisar Hundewale, K Vasudeva Reddy, B. Pradeep, "Implementation of LFSR counter using CMOS VLSI Technology," Lecture notes of the Institute for the computer sciences, Social Informatics and Tele Communication Engineering, *ISBN* : 978-3-642-32573-1, Volume 62, 2012, pp. 275-281.

Y. Pu, J. P. de Gyvez, H. Corporaal, and Y. Ha, "An ultralowenergy/ frame multi-standard JPEG co-processor in 65 nm CMOS with sub/near-threshold power supply," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, *ISBN* :978-1-4244-3458-9, pp 146–147-147a, Feb. 2009.