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4-Bit Even Parity Generator on 45nm Technology

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***Abstract*—In computer networks, while data transmission there is a possibility of getting errors that is data loss. The role of parity generator is, it generates parity bit while data is transferred from one device to other device. In this we have even parity and odd parity based on number of ones in the transferring data. Here the 4-bit parity generator has been developed using NAND circuitry. The design implementation and analysation is done by using the Microwind V3.1Tool. Microwind is a EDA (Electronic Design Automation) and schematic editor/simulator tool respectively having higher speed, low on power and size of technology. Simulation results show the comparison of the area and the power factor.45nm technology feature size has been used for the performing the verification of architecture developed which retains the parity generator functionality.**

I. INTRODUCTION

Electronics as we know today are characterized by reliability, low power dissipation, extremely low weight and volume, and low cost, coupled with an ability to cope easily with high degree of sophistication and complexity[2].When binary data is transmitted and processed, it is susceptible to noise that can alter or distort its contents. Digital systems must be accurate to the digit, errors can cause a serious problem so it should be ensured that the data is error free during the process of data transmission in the form of binary bits[5]. Errors may occur due to various reasons such as interference due to electro-magnetic waves, cross-talk caused due to closely connected signal wires, power supply surges, logical noise etc., so, the detection of faults is a major concern for the present communications as there should not be any loss of information during data transmission. In communication systems error correction technique is a most important area that has been exploited [4]. The data will be found defective, when the data entered at the receiver side has different parity compared to the parity present at the transmitter output. The parity bit is suitable only for detecting errors it cannot correct any errors, as there is no way to determine which particular bit is corrupted. Several schemes have been devised to detect the occurrence of a single bit error in a binary word, so that whenever such an error occurs the concerned binary word can be corrected and re transmitted [5]. Successful transmission can take a long time, or even never occur on a noisy transmission medium. Because of error detection and correction parity generator and checker circuit has being exploited in many applications such as Satellite communication, broadband, Wireless communications, digital television, Compact disc players, Wireless Sensor networks[4]. As the parity generator is implemented using nand gates, Figure 1 shows the symbol and the truth table of the gate.

This present paper is organized as follows, in Section II parity generator and design, Section III proposed schematic ,Section IV layout, Section V Simulation results for different technology approaches. Section VI Results and discussion comparison of the approaches that too in graphical

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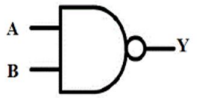


Inputs		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig 1:Nand gate and its Truth table

representation describes the comparative study of technology approaches of 4-bit parity generator. Section VII concludes the paper.

II. Parity Generator

For the detection of errors during transmission of binary information parity bit is used. A parity bit 0 or 1 is attached to the data bits such that the total number of 1s in the word is even for even parity and odd for odd parity. The parity bit can be attached to the code group either at the beginning or at the end depending on system design [5]. The message, including the parity bit, is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator [3]. It is combinational circuit that accepts an n-1 bit stream data and extra bit that is to be transmitted is generated with the bit stream. In the case of even parity the occurrence of bits whose value is 1 is counted. If that count is odd, the parity bit value is set to 1, making the total count of occurrences of 1s in the whole set (including the parity bit) an even number. If the count of 1s in a given set of bits is already even, the parity bit's value is 0. Figure 2 shows the 4-bit parity generator using xor gates and Table 1 displays the truth table.

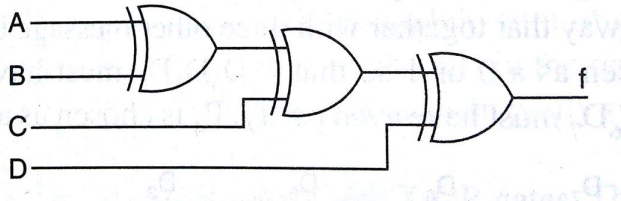


Fig 2:4-bit even parity generator

4-bit data input				Output
A	B	C	D	parity bit (f)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Table 1 Truth Table of 4-bit parity generator

III. SCHEMATIC DIAGRAM

The 4-bit even parity generator is implemented using NAND gates and requires 12 gates. Figure 3 shows the schematic diagram of 4-bit even parity generator using NAND gates.

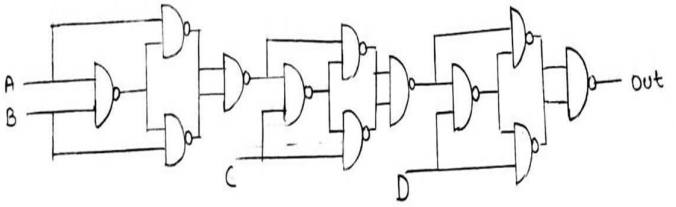


Fig 3:NAND gate Implementation

IV. LAYOUT

Figure 4 shows the layout of 4-bit even parity generator which is implemented on 45nm foundry using Microwind V3.1 Tool. The DRC is checked for the errors before the simulation.

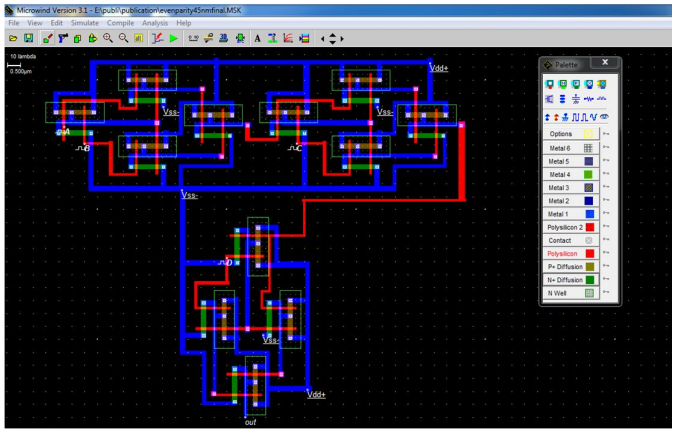


Fig 4: 4-Bit even parity generator layout

V. SIMULATION RESULTS

Timing waveforms are verified in accordance to the architecture of 4-Bit even parity generator. The timing waveforms displays out the input and output featurette, representing the outputs for the different inputs [1].Figure 5 and figure 6 show the output (Voltage Vs Time) signals of the implemented circuit on 45nm and 90nm technologies respectively. As compared with the 45nm foundry 90nm has a delay.

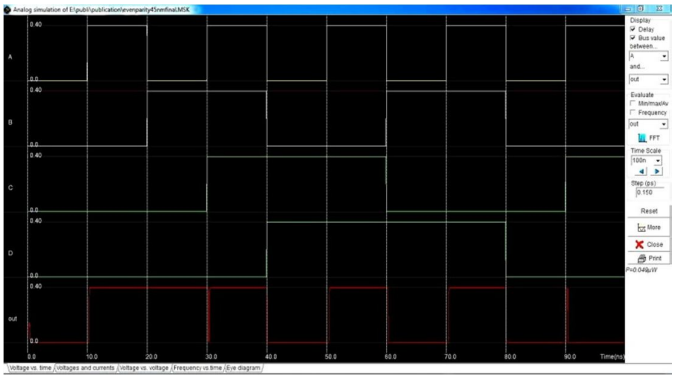


Fig 5: 45nm Technology (Voltage Vs Time)

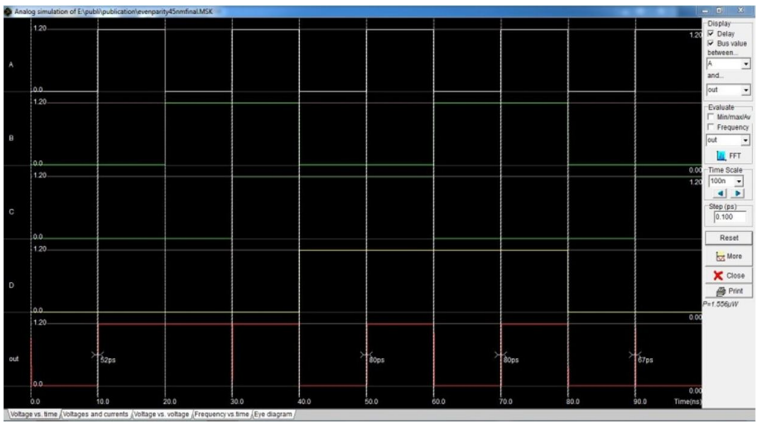


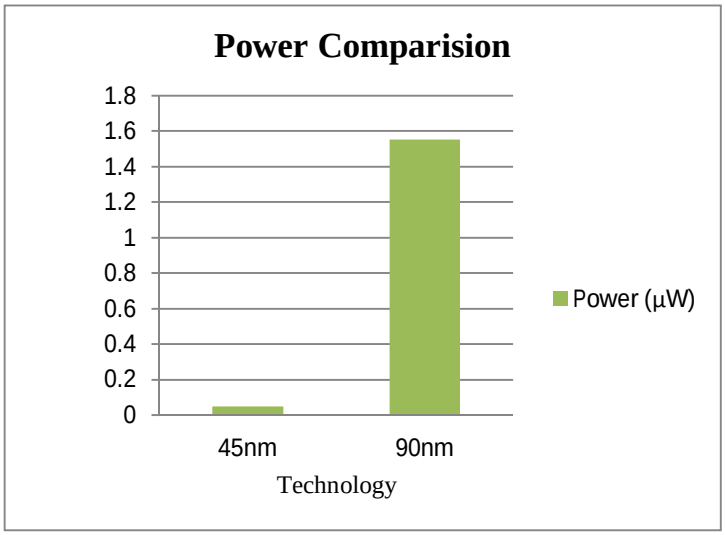
Fig 6: 90nm Technology (Voltage Vs Time)

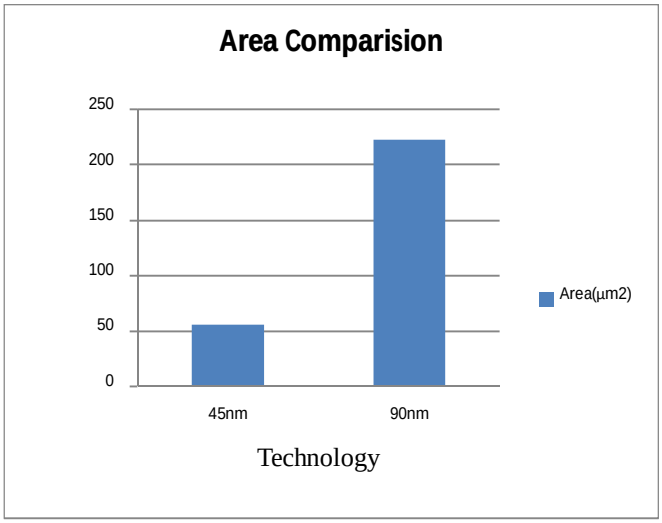
VI. Results and Discussion

The CMOS circuitry is implemented and synthesized. The area and power consumption parameters are compared in both proposed design technologies. The performance comparison of the 45nm technology generated 4-bit even parity generator to the 90nm technology. Area and power are to be the performance parameters. The comparison resulted in, Table 2 yields to the comparative narration of the parameters in the tabular form. The width of the 45nm technology layout results to the 8.15µm and height to 6.825µm. Resulting to total surface are of 55.62µm^2 . Also, the power of the 45nm technology layout resulted to 0.049µW. The width of the 90nm technology layout results to the 16.3µm and height to 13.65µm, resulting to total surface are of 222.495µm^2 .The power measure of the 90nm technology results to the 1.556µW. The comparative analysis of area and power is shown in the graphical representation.

TABLE II: COMPARISON OF TECHNOLOGIES USED

S.NO	TECHNOLOGY USED	AREA(µm^2)	Power (µWatt)
1	45nm	55.62	0.049
2	90nm	222.495	1.556





VII. Conclusion

From the above analysis, it clear that 45nm technology designs are more efficient in area and power in comparison to the 90nm technology . So the utilization of 45nm technology over the 90nm technology should be kept in consideration were the area and the power factor for the designing are to be considered.

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