Grenze International Journal of Engineering and Technology, Jul Issue

A Comparative Study on different Proposed Nanotube TFETs

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***Abstract*—In these paper, we review some nanotube TFET based papers. Based on their device parameters , we decide which device is better for a particular application. Earlier designs gave impressive results, some of them were more focused on subthreshold swing (SS_{avg}) and threshold voltage , whereas some designs are more focused on a good I_{on} current. We can also see the effect of high-k dielectric which used as gate oxide material for better tunneling current. Drain current(I_{on}) comparision with several TFET designs are given in this study.As unit parameters, the electric field, electric potential, and energy band diagram have all been observed.**

***Index Terms*— *Terms* Review, TFET , Nanotube TFET, device parameter, Linearity parameters.**

I. INTRODUCTION

Analog device are characterized by three parameters power, speed and area .We all required a device which has low power consumption, high speed and low area. This requirement is done by scaling of device. Individual device scalability has its limits, and as process technology went down closer to 20 nm, it became difficult to achieve adequate scaling of different device parameters. Scaling below nanoscale has some drawbacks ex. high power dissipation, short channel effect (SCE)[11]. So we need a device which have less effected from SCE. Scaling the supply voltage in the case of MOSFETs will reduce power consumption [8]. The leakage current increases exponentially as the threshold voltage (V_{th}) is scaled up [1][10]. To address the shortcomings of traditional MOSFETs, a new operating theory has been tested using a particular kind of transistor construction, non-silicon based materials [1]. So we have to use a TFET which have a good I_{on} /I_{off} [9] ratio with low subthreshold swing[13]. But the limitation of TFET structure is a less Ion current. So to eliminate this problem, we use different types of structures and architectures of TFET [7][15].

II. RELATED WORK

A. Electrostatic Doped Nanotube TFET

In this paper [1], comparison to other nanowire TFET architectures, this one has a larger tunneling region and a higher drain current (NW-TFET). While comparing with gate-all-around (GAA) TFETs, nanotube TFETs have been improved gate controllability as well as efficiency. With almost the same dimensions as nanowire TFETs, NT-TFET enhances ON-state current (I_{on}). The tunneling region of nanotube TFETs is larger than that of

Grenze ID: 01.GIJET.7.2.14

nanowire TFETs, allowing for a better ON-current (I_{on}). This device drain current (I_{DS}) is 3×10^{-5} A/μm, as well as its OFF current (I_{off}) is on the order of 10^{19} A/μm. The suggested design demonstrates a better I_{on}/I_{off} current ratio for sensing and RF applications. With a V_{DS} of 1.2 V, the device has a Vth of 0.6 V as well as a high SSavg of 20 mV/dec, The device presented is appropriate for use in analogue electronics uses, according to the linearity parameter. Higher order distortion HD2 and HD3 having sufficient values of 2×10^{-2} dBm and 10^{-3} dBm respectively. IMD3 and IIP3 have values of -50 dBm and -50 dBm, which are very small for analogue electronics applications. This paper reviewed with the aim of expanding the analysis to the level of structure design and circuit design.

B. Dual-gate all around core-shell nanotube TFET

This paper [2] shows the superiority of a Silicon-based Nanotube Tunnel FET above a traditional Nanowire TFET has been shown. They also illustrated the prevailing qualities and functions of the device structure that was suggested in comparison to the nanowire structure [12] by simulations of the systems in Silvaco Atlas. The Silicon Nanotube Tunnel FET being capable of overcoming the Nanowire properties owing to its vertical device structure, resulting in a significantly enhanced ON-state current. Furthermore, with in context of this TFET, the analogue and RF specifications were exceptional, considering it acceptably reasonable and also its relevance important for very small current and power requirements. Estimated DIBL value of traditional Nanowire TFET studied and determined to really be 495.8 mV/V, whereas the result with this Dual Gate Nanotube TFET reached 175.29 mV/V, demonstrating also that suggested design has a significantly higher DIBL values. Perhaps it emphasises a suggested device's tolerance to short-channel effects, which would be a significant feature.

C. Junctionless Silicon Nanotube TFET

In this paper [3], a silicon nanotube JL-SiNTTFET was developed which is junctionless and examined in terms of productivity analysis in this research. The suggested approach improves device productivity by enhancing gate controllability on a particle, allowing for a larger energy band difference close to the source channel interface. Whenever the oxide gets developed upon on base inside a transistor, every one of the silicon linkages weren't properly linked with oxygen ions, leading to dissatisfied and dangled bonds just at junction, which can be caused via contamination inside base. Traps are the result of this. This base material may drastically modify its electrical properties of semiconductor because of existence of such flaws within silicon.
In contrast to the traditional junctionless silicon nanowire TFET, I_{on} rises by 117% at V_{DS} =0.5 V, while I_{off} , SS_{avg} lower about 99% and 43.47%. Furthermore, since both equipments are examined at elevated heat, the device has a larger Ion/Ioff ratio, with in a range of 10^{10} at temperatures over 300 K.

D. Cylindrical Nanowire-TFET with Core-Shell Channel Architecture

In this paper [4], the proposal configuration of the gate all around (GAA) tunnel field transistor is modelled and studied, including nanowire-GAA, core-extended source, and core-extended source/drain structures. The drain current improved with in core-extended supply structure and core-extended source/drain structure [17], according to the findings. Energy band bends for nanowire structures becomes sharper, but beginning of tunnelling throughout the distance is delayed in this structures. This structure begins tunnelling towards the source-channel interaction from the side. Tunneling possibility reduces in this structure because of increasing screened depth. The core-extended source/drain design has a higher current drive ability. The driving current in nanowire design can be attributed to tunneling, while in core-extended models, its current being due to both tunneling and thermionic phenomena.

E. High k silicon Nanotube tunnel FET device

This paper [5] suggest a new tunnel FET structure inside this study to obtain greater tunnelling rate. Regarding low-power uses, short-channel effects should always be addressed with in nanoscale range. Short-channel effects should be controlled in the nanoscale regime for low-power uses. The figure-of-merit, which included I_{on}/I_{off}, transconductance, and SS_{avg}, was measured and calculated at the same time. To demonstrate the ability, TCAD simulations are being used to evaluate the results of silicon nanotube and silicon nanowire TFETs. The better intensity of the electric field inside a nanotubes structure with a large dielectric constant HfO_2 insulated gate leads in increased particles mobility. Its maximum electric field location states that the overall mobility is already at highest near source–channel interaction, resulting in a significant electron density tunnelling to channel from source. Detailed 3D models being used to get a better description of the physical aspects of energy barrier width and recombination rate heterogeneity with bias and time. The I_{on} is improved by examining various dielectric materials.

F. Core-Shell Dual Metal-Dual Gate Cylindrical GAA Silicon Nanotube-TFET

In this paper [6], the hetero-metal technique for core as well as shell gate electrodes is used to convert a basic nanotube transistor on a dual gate configuration. For improved device parameters, the thin nanotube structure actually reduced substrate content while increasing electrostatic influence on channel[16]. The existence of material with such a less work function at source-channel interaction causes reversed charged particles to accumulate inside channel, allowing minority charged particles to tunnel out of source early. An initial increase in current flow contributed with in improvement of such structure's SS_{avg} value and threshold voltage[14]. Several performance parameters are used to demonstrate and assess the performance superiority of the suggested system, the Silicon-based Hetero Metal-Dual Gate Nanotube Tunnel FET, on above Single Metal-Dual Gate Nanotube Tunnel FET.

III. CONCLUSION

In this article, we will conclude that if we want to improve TFET structure performance, which is primarily power speed, we must use different types of architecture than only we can TFET with MOSFET in analog or digital applications. We can now recognise and use high-k dielectric materials as gate oxide materials.

In comparison to gate-all-around (GAA) TFETs, nanotube TFETs have improved gate controllability and efficiency. With almost the same specifications as nanowire TFETs, NT-TFET enhances ON-state current (I_{on}). The tunnelling region of nanotube TFETs is larger than that of nanowire TFETs, allowing for a better ON-current (I_{on}).

Table.I present a comparison of analog parameters for the various TFET configurations proposed earlier. Since they are all using different TFET architectures, we can see that they have different values for I_{on} , $I_{off,}$ I_{on}/I_{off} and SS_{avg}.

TABLE I. COMPARISON OF ANALOG PARAMETERS OF VARIOUS NANOTUBE TFET

Parameter / Designs	I_{on} (A/μm)	I_{off} (A/μm)	I_{on} /I_{off}	SS_{avg} (mV /dec)
EDNT-TFET [1]	3×10^{-5}	1.5×10^{-17}	2×10^{12}	20
NT-TFET[2]	5×10^{-6}	4.5×10^{-19}	1.1×10^{13}	58.3
JL-SiNT-TFET [3]	1.1×10^{-6}	3.5×10^{-17}	3.2×10^{10}	19.87
CNT-TFET [4]	1.8×10^{-5}	3.6×10^{-18}	5.0×10^{12}	16
HK-Si-NT-TFET[5]	3.7×10^{-5}	5.2×10^{-11}	7×10^{5}	52.4
GAA CNT-TFET[6]	2.9×10^{-6}	1.5×10^{-18}	1.9×10^{12}	60

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