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Design and Analysis of Ultra-Low Power CMOS based Charge Pump for Hand Held Devices

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***Abstract*—Hand-held devices, such as smartphones, tablets, and wearable technology, have become an integral part of our daily lives. These devices require high-performance and energy-efficient power management circuits to extend their battery life and reduce heat dissipation. This work describes the design and analysis of a low power CMOS based charge pump for hand held devices in piezoelectric harvesting circuit. The charge pump circuit is designed using 45nm technology, which allows for low power consumption and small area requirements. The proposed charge pump circuit is designed to operate at low input voltages and provide high voltage gains with minimum power consumption. The circuit is analyzed using Cadence simulation tool and the results show that the proposed charge pump circuit can provide a voltage gain of 10 with an efficiency of 75% at an input voltage of 100mV with the required output voltage of 1V. Overall, the proposed low power CMOS based charge pump for piezoelectric harvesting circuit using 45nm technology offers a promising solution for energy harvesting in hand held devices.**

***Index Terms*— Power conversion efficiency, piezoelectric transducer, voltage gain, Complementary Metal oxide semiconductor(CMOS).**

I. INTRODUCTION

In the ever-evolving landscape of handheld devices, the demand for efficient power management solutions has grown exponentially. One such solution that has gained significant attention is the charge pump. A charge pump is a type of DC-DC converter that has found widespread use in various portable electronic devices, including smartphones, tablets, and wearable gadgets. Its ability to efficiently boost or step up voltage levels makes it a crucial component in ensuring the smooth operation of these devices. The rapid advancement of technology has led to the development of increasingly sophisticated handheld devices with higher power requirements and smaller form factors. This presents a challenge in terms of supplying sufficient power to these devices while maintaining compact designs. Charge pumps offer an elegant solution to this dilemma by efficiently converting and managing electrical power. Piezoelectric energy harvesting has emerged as a promising technology to supplement the power needs of hand-held devices. This paper presents the design and analysis of a charge pump circuit using 45nm CMOS technology and discussion of different charge pump topologies and finally the proposed charge pump is developed with low power consumption and high efficiency, making it suitable for use

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in hand-held devices powered by piezoelectric energy harvesters[1]. The performance of the proposed circuit is evaluated in terms of output voltage, power consumption, and efficiency. The results demonstrate that the proposed CMOS-based charge pump is a promising solution for powering hand-held devices using piezoelectric energy harvesting.

II. Methodology Proposed

The design of the piezoelectric harvester circuit will be based on the provided block diagram in Figure 1, which outlines the proposed vibrational energy harvester. The design process will involve analyzing various charge pump topologies and selecting an appropriate oscillator. The overall architecture of the vibrational energy harvester will consist of the following components: a piezoelectric generator, a charge pump, an oscillator, energy storage (such as a supercapacitor), and a load. Firstly, the circuit methodology begins with the initialization of a piezoelectric generator (PEG) or transducer. The primary reason for choosing a piezoelectric generator for the circuit is its high energy density and ease of integration. The PEG is responsible for converting mechanical energy into electrical energy, resulting in an electrical signal. This converted signal is then measured, and it is found to have a voltage of 100mV. To power the circuit, the 100mV DC voltage is supplied to both the charge pump and the ring oscillator. The desired output voltage of the charge pump is 1V, which is then stored in a supercapacitor. For this purpose, a 1F supercapacitor is chosen as it is capable of storing voltages ranging from 1V to 2V. The voltage stored in the capacitor can be subsequently utilized to power any handheld device. The flow of the harvesting circuit is presented, and the analysis and design of the charge pump, ring oscillator, and piezoelectric generator are discussed in detail.

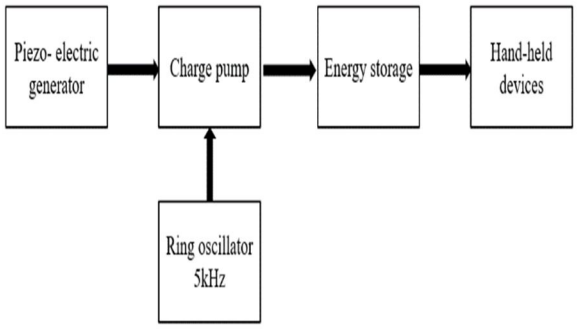

Fig. 1. Block Diagram of piezoelectric harvester

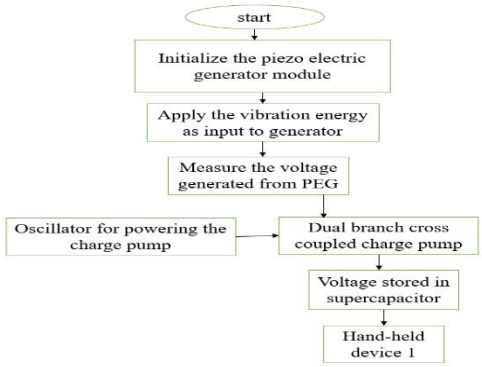

Fig. 2. Proposed Methodology

A. Piezoelectric transducer

In the simulation of a piezoelectric device, it is common to model it in both mechanical and electrical domains, as depicted in Figure 3. The interaction between these domains is captured by an electrical transformer, as shown in Figure 4. In the mechanical domain, there are three key parameters: R_p represents mechanical damping, Cm corresponds to the reciprocal of mechanical stiffness, and L_m takes into account the effective mass. On the other hand, the electrical domain includes the vibrational excitation, which can be modeled as a current source. This current source incorporates parasitic capacitance (C_p) and resistance R_p. Typically, R_p is significantly larger than the impedance of C_p, allowing us to neglect it. The proposed CMOS active rectifier design employs a standard model for a piezoelectric device, represented by C_p, R_p, and the sinusoidal current source $I_p(t) = I_p Sin(2\pi ft)$

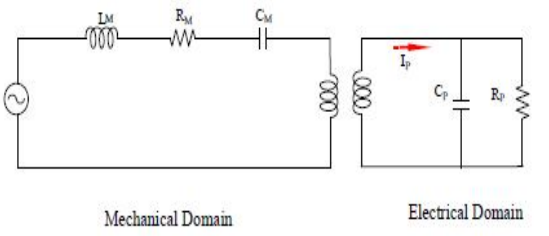

Fig. 3. Schematic of a piezoelectric transducer showing mechanical to electrical domain[13]

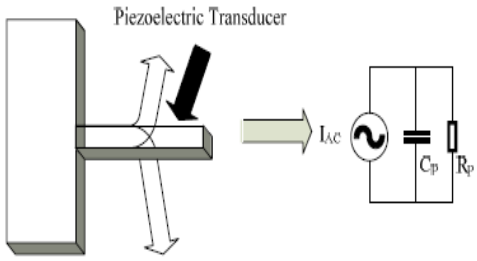

Fig. 4. Simplified model of a piezoelectric transducer[13]

B. Ring oscillator

Prior to creating the schematic, an examination and analysis of the inverters and current mirror were conducted to understand their behavior. The schematic designs underwent simulation to obtain the DC operating characteristics. For the ring oscillator shown in figure 5, an output frequency of 5kHz was chosen deliberately[1]. The reason behind selecting this frequency is that a higher frequency for the charge pump would result in longer pumping time for the charge to transfer from one stage to another. This extended delay in the circuit would adversely affect its performance, hence opting for a lower frequency to mitigate such issues.

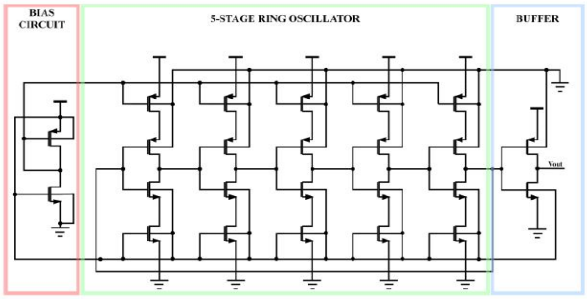

Fig. 5. Schematic diagram of CMOS Ring oscillator[1]

The performance of a circuit is influenced by several factors, with one significant aspect being the delay between stages. In this context, the delay introduced by each inverter between stages is referred to as the propagation delay (τpd). The propagation delay is determined by averaging the transition delays for both the high-to-low and low-to-high transitions within each stage.

$$\tau_{pd} = (\tau_{pd} + \tau_{pd})/2 \qquad (1)$$

Second factor affecting performance of ring oscillator is its frequency. For N stage, oscillator frequency is given as:

$$f_{osc} = \frac{1}{\tau_{pd}} = \frac{1}{2N\tau_p} \qquad (2)$$

The frequency of the ring oscillator depends upon the τp which in turn depends on the circuit parameters. The two parameters

τ_{phl} and τ_{plh} can be determined for a single stage inverter from the equations given below.

$$\tau_{phl} = \ln(2)(C_l)\left(\frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_{gs}-V_{tn})}\right) \qquad (3)$$

To determine the number of stages with the desired frequency, the formula below is used. To obtain a 5kHz frequency,

$$5kHz = \frac{1}{2N(21.5680u)} \qquad (4)$$

$$N = \frac{1}{(5kHz)(2)(21.5680u)} \qquad (5)$$

The voltage gain of a circuit is influenced by the magnitude of the frequency and the number of stages. When the amplitude of the frequency signal is higher, it can generate a larger voltage swing across the capacitor in each stage. Consequently, by allowing an increase in the amplitude of the frequency signal, the output voltage can be rapidly increased. Therefore, to reduce the number of stages in a charge pump and enhance the voltage gain of the circuit, the frequency magnitude should surpass the voltage Vdd. This ensures that the voltage swing across the capacitor is sufficient for generating the desired output voltage amplification.

$$A_v = \frac{V_{out}}{V_{in}} \qquad (6)$$

The Voltage gain of the CP is determined by no of Stages and voltage per stage. Each stage in CP provide Voltage gain of 2 which means the output voltage doubles with each stage by the below equation.

$$\frac{V_{out}}{V_{in}} = 2^N \qquad (7)$$

C. Charge pump design

The diagram in Figure 6 illustrates a two-stage Cockcroft-Walten multiplier comprising two capacitors and two diodes in each stage. Specifically, the first stage includes capacitors C1 and C2, as well as diodes D1 and D2, while the second stage consists of capacitors C3 and C4, along with diodes D3 and D4. While the Cockcroft-Walton circuit connects the coupling capacitors in series, which leads to a high output impedance with increasing

stages, the Dickson charge pump circuit connects the coupling capacitors in parallel. However, in the Dickson circuit, the coupling capacitors must be able to handle the full output voltage. As a result, the Dickson circuit exhibits a low output impedance as the number of stages increases. Both circuits require the same number of diodes and capacitors and can be proven to be equivalent. One drawback of the Dickson charge pump circuit is that the boosting ratio is reduced due to the threshold voltage drops across the diodes .After performing manual calculations, it has been determined that a minimum of nine stages is required to meet the desired specification of achieving 1V output with a minimum input of 100mV. However, in order to incorporate an overdesign approach, the researcher has decided to utilize 16 stages.The final design, as depicted in Figure 7, showcases the 16-stage modified Dickson charge pump. It employs a uniform transistor size and a capacitance value of 37fF, which is implemented using a Metal-Insulator-Metal (MIM) capacitor. In parallel with this on-chip implementation, an off-chip capacitor with a value of 1pF will be employed.

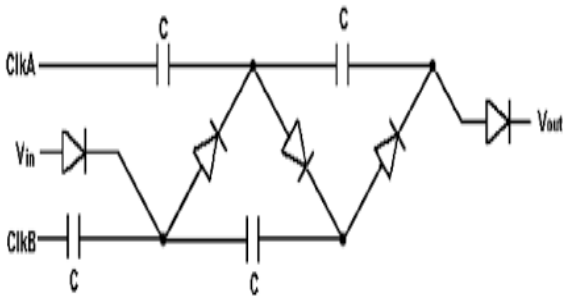

Fig. 6. Schematic diagram of Crocroft Walten Charge pump[24]

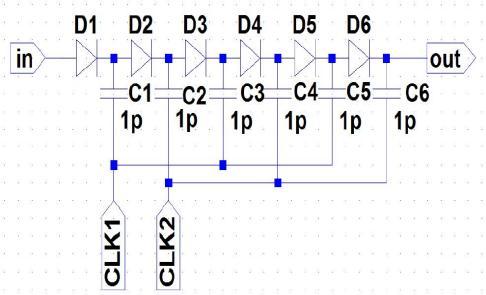

Fig. 7. Schematic diagram of Diode based Dickson Charge pump[24]

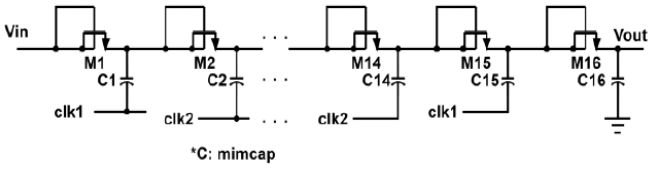

Fig. 8. Schematic diagram of MOSFET based Dickson Charge pump[1]

In Figure 8, it is observed that an NMOS transistor is employed in a diode connected configuration where the transistor's bulk [1] is connected to both the source and gate. Consequently, the maximum voltage gain per stage (Vg) of the Dickson charge pump circuit can be determined by the equation Vg = Vin - Vt, where Vt represents the threshold voltage of the NMOS transistor. Traditional charge pump topologies, such as the Dickson charge pump, utilize MOS devices connected as diodes, which suffer from voltage drops caused by the threshold voltage (Vth). In a typical nanometer-scale CMOS technology, each VTH drop corresponds to an approximate 0.4V decrease in the conduction path. This reduction becomes significant for energy harvesters operating in the millivolt output range, as evident from the typical expression for the charge pump's output voltage, VOUT, which is obtained from

$$V_{out} = (N+1)(V_{dd} - V_{th}) - N\frac{I_{out}}{f_{clk}C_{pump}} \qquad (8)$$

Employing two branches in a cross-coupled configuration enables the generation of a higher output voltage compared to a single branch charge pump. Moreover, the cross-coupling aspect aids in reducing ripple and enhancing the stability of the output voltage. Figure 9 depicts the schematic diagram of a dual branch cross-coupled charge pump.

When dealing with small input signals, the diode-connected transistors operate within the weak inversion or subthreshold region. Consequently, they conduct a time-varying current without resorting.

$$I_{d,sub(t)} = I_{so}\frac{W}{L}e^{\frac{V_{gs(t)}}{nV_t}}(1-e^{\frac{V_{ds(t)}}{V_t}})^{(1-\lambda V_{ds(t)})} \qquad (9)$$

At the same time, there is a leakage current being conducted given by:

$$I_{leak}(t) = I_{so}\frac{W}{L}(1-e^{\frac{V_{ds(t)}}{V_t}})^{(1-\lambda V_{ds(t)})} \qquad (10)$$

Conventional transistors typically exhibit a threshold voltage (Vth) of around 400mV, which proves to be impractical for certain applications. However, there are alternative transistors with lower Vth values, such as those in the range of 150mV. These transistors strike a favorable balance between charging and leakage current. On the other hand, there are also zero Vth transistors available, with an incredibly low threshold voltage of 40mV. While these transistors offer the advantage of minimal voltage requirements, they come with a significant drawback: a considerably higher leakage current. Consequently, the utilization of zero Vth transistors is generally discouraged due to this elevated leakage current.

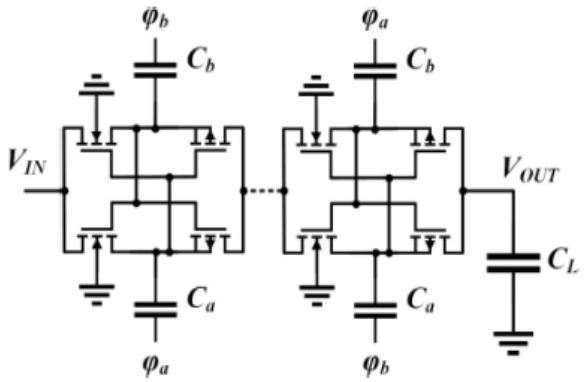

Fig. 9. Schematic diagram Dual branch cross coupled Charge pump

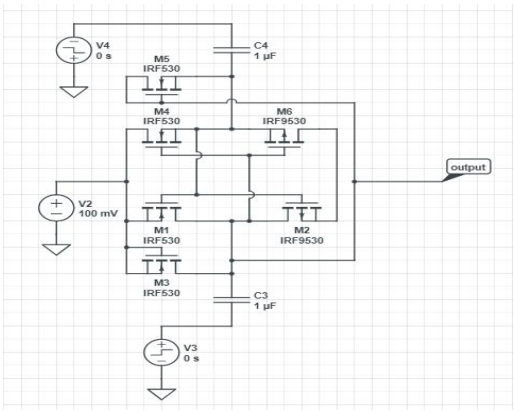

Fig. 10. Proposed diagram Dual branch cross coupled Charge pump

an be mitigated when employing either a sufficiently high frequency or a larger storage capacitance. This observation is supported by examining the equation governing the output voltage.

$$V_{out}=\frac{N}{2}\left[\left(\frac{C_{stage}}{C_{stage}+C_s}\right)V_{RF}-V_{th}-\frac{I_{leak}+I_{out}}{\left(C_{stage}+C_s\right)f_{RF}}\right]-V_{th} \quad (11)$$

Where Vout is the DC output voltage, N is the number of stages, Cstage is the capacitance per stage, Cs is the parasitic stage capacitance, however the parasitic capacitance will be neglected because of low frequency signal VRF is the amplitude of the input frequency signal from the on-chip antenna, is the frequency of operation and Ileak and Iout are the leakage and output current of the pump respectively.

To enhance the charge pump's performance, it is necessary for the output capacitance (Cout) to be greater than the capacitance per stage (Cstage). The number of stages can be reduced if the amplitude of the frequency signal is greater than the input signal. This simplifies the addition of a voltage controller. To design a voltage controller, an additional circuit is required, increasing the number of circuit blocks in the harvesting circuit. However, instead of designing a separate voltage controller specifically for the harvester, an alternative approach involves modifying the charge pump in the harvester to amplify the amplitude of the frequency signal beyond that of the input signal. In the dual branch cross-coupled charge pump, the MOSFET-based Dickson charge pump concept can be employed. According to the MOSFET-based Dickson charge pump, an NMOS with its gate-source-body connection acts as the anode, while the drain serves as the cathode. When a 100mV input signal is applied to the gate-source terminal of the NMOS, the drain terminal voltage becomes twice the input voltage when a pumping capacitor is introduced. By utilizing the charge transfer switch (CTS), the voltage at the pumping capacitor can be doubled, reducing the necessity for additional voltage controllers. The schematic in Figure 10 illustrates the propose cross-coupled charge pump. The CTS refers to the NMOS transistors M3 and M5 in the below figure. The power conversion efficiency can be calculated with the formula

$$\eta = \frac{P_{out}}{P_{out}+P_{loss}}, where\ P_{loss} = P_{in} - P_{out} \quad (12)$$

III. Implementation Results & Comparison

All the implementation is designed in 45nm technology with transient analysis for 200ms

The performance of ring oscillator also depends on the transistor sizing, due to which all the design are simulated in Cadence as it has some library updates we need to some some trial and error method to bring the output frequency of the oscillator foe the expected value. The table of transistor sizing with output value is given in the below table 1

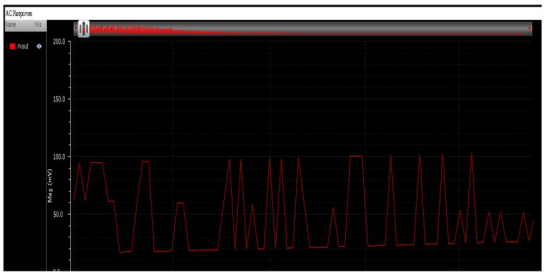

Fig. 11. Output waveform of piezoelectric transducer in electrical domain

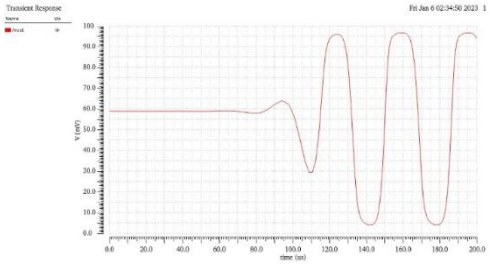

Fig. 12. Output waveform of ring oscillator

TABLE I: W/L RATIO CHANGES TO GET ACCURATE FREQUENCY

PMOS (W/L)	NMOS (W/L)	RESULT
1.3u/45n	120n/45n	5.41kHz
950n/45n	120n/45n	7.9kHz
700n/45n	200/45n	18.3kHz
500n/45n	120n/45n	22kHz
300n/45n	200/45n	25kHz
120n/45n	120n/45n	27kHz

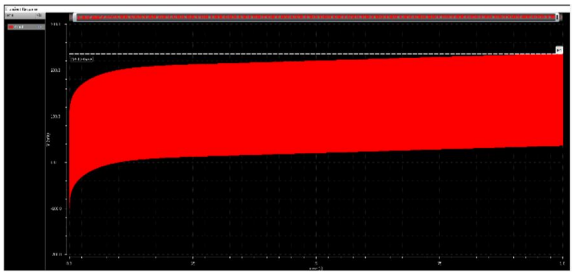

Fig. 13. Output Cockcroft-Walton charge pump circuit in 90nm technology

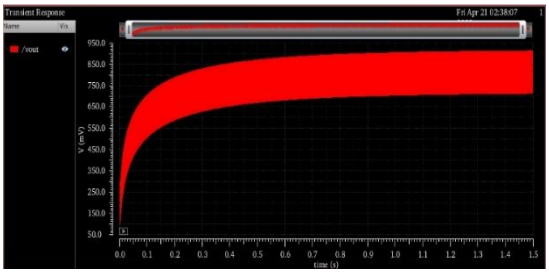

Fig. 14. Output of Diode based charge pump circuit

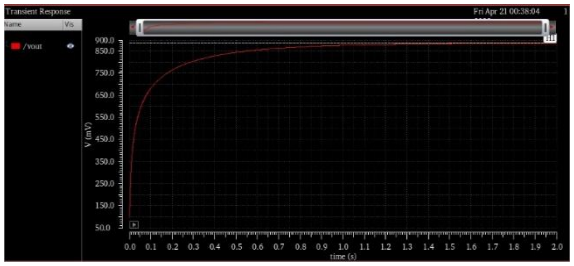

Fig. 15. output waveform of MOSFET based Dickson Circuit charge pump

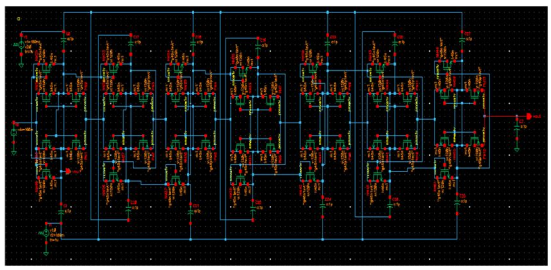

Fig. 16. Implemented Schematic diagram of proposed cross couple charge pump

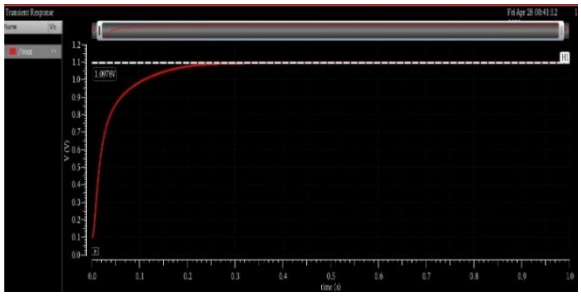

Fig. 17. output waveform of proposed cross coupled charge pump circuit

The below table 2 shows the comparison of performance parameters of different charge pump topologies. By analysing power conversion efficiency and stages of the circuit, the dual branch cross coupled charge pump gives the better results compared to other charge pump circuits.

TABLE II : COMPARISON OF PERFORMANCE PARAMETERS OF CHARGE PUMP

	cockroft Walton CP	**Diode Dickson CP**	**MOSFET Dickson CP**	**Dual branch Cross-coupled CP**	**Proposed Cross-coupled CP**
Vout	200mV	650mV	900mV	1.05V	1.097V
Vin	100mV	100mV	100mV	100mV	100mV
Power dissipation	112.6uW	340.5uW	16.7pW	5.39pW	1.47pW
Stages(N)	3	6	16	11	7
Efficiency	50%	53%	61%	67%	75%
Technology	90nm	90nm	45nm	45nm	45nm

IV. CONCLUSIONS

By observing the ultra-low power CMOS based charge pump topologies for piezoelectric energy harvester has been designed and implemented in 45 nm CMOS process and satisfied the parameter requirements set. Analysis of the performance of the circuit was done using the selected and modified topology for this design. The Ring Oscillator is a 5-stage current-starved inverter connected to a 7-stage modified Dual branch cross coupled charge pump and the output is a 1pF off chip capacitor. The harvester reached or produced the required output voltage of 1V with a time budget of 1 second. Simulation showed that the design met all the requirements after implementing all the necessary techniques and considering all the needed parameters set for. The performance parameters of Charge pump is simulated in 45nm technology and Dual branch cross coupled Charge pump with low on resistance CTS had given better power conversion efficiency, Voltage gain of 10 is achieved and power conversion efficiency of 75%.

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