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Characterization and Optimization of Gate-All-Around Nanowire FETs for RF Applications

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***Abstract*— The Gate-All-Ground (GAA) n-channel nanowire field-effect transistor (NWFET) is simulated using visual TCAD, and DC analysis is carried out with optimized sub-20 nm nodes with a doping concentration of acceptor ions varied from 1x1017 cm^{-3} to 1x1019 cm^{-3}. The proposed GAA NWFET device with a doping concentration of 1x1019 cm^{-3} gives excellent electrical characteristics with a subthreshold swing (SS) of about 59.57 mV/dec, a higher switching ratio (ION/IOFF) of 1010, and drain-induced barrier lowering (DIBL) of less than 10.19 mV/V. Further additional investigation was carried out by varying temperatures ranging from T = 300K to T = 500K; the sensitivity of the device was found to be better at higher temperatures. The proposed GAA NWFET gives a higher switching ratio, which will be suitable for RF applications. The suggested transistor could be a better device in the field of high-temperature and RF applications.**

***Keyword*— Gate-all-around, Nanowire FET, SS, DIBL, High-K, Room temperature.**

I. INTRODUCTION

The semiconductor device plays an imperative role in improving performance in communication, automation, space, computing, and other applications. Because the advantages of these devices can develop with low power, high performance, and compact size, which are the major requirements in the semiconductor industry, specifically portable devices like mobile phones, notebooks, laptops, etc., are used in day-to-day life [1]. The transistor's size is gradually reduced in place of Moore's law, which continues to drive their application [2]. In the complementary metal oxide transistor (CMOS), conventional transistors are scaled down. The transistor has multiple challenges, which lead to degrading the performance of the device due to secondary effects such as short channel effects (SCE), drain-induced barrier lowering (DIBL), etc. The short channel effects arise where the channel length is comparable to the source and drain junction's depletion layer width. At increasing drain voltages, the transistor's threshold voltage decreases due to a short-channel condition referred to as DIBL in MOSFETs. The non-conventional Junctionless transistor will address these issues, but even after scaling down the transistor, the device can maintain the same performance. These junctionless devices, such as FINFETs and GAA FETs, etc. [10]

Gate-all-around nanowire FET has arisen as the most promising device for low-voltage applications in the sub-nano meter regime. GAA NWFETs is capable of withstanding the short channel effect by their geometric design, and they have greater electrostatic control, greater potential, higher packaging density, and transport features [3]. Despite these advantages, it experiences higher series resistance, which arises due to the formation of abrupt junctions between the heavily doped source-drain and the lightly doped silicon body [8][13].

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Using high-k dielectric material like HfO_2 will improve the efficiency of a device by suppressing the series resistance [6], reducing the leakage current, and improving the drive current by increasing the gate capacitance [4].
The semiconductor industry will mainly focus on the size of the transistor; it will directly enhance the speed of the integrated circuits by designing the transistor with low power consumption and operating at high frequency [14][15].
These devices are used for RF, analog, and digital circuits [5]. The optimization of Junctionless transistors has provided an excellent Ion/Ioff ratio, leading to higher switching speeds for digital circuits, and the subthreshold swing is almost equal to the ideal value [7]. The GAA NWFET has better electrical properties, and with high-K, it shows excellent performance by decreasing the Ioff current [11][12]. With proper scaling, a better Ion can be achieved, reducing Ioff, so the Ion/Ioff ratio will improve, making it suitable for switching applications and other performance parameters obtained with high Gm, low DIBL, and SS [5].
This research emphasizes the performances of GAA NWFET, which is implemented in a visual TCAD tool with a high-k dielectric material. The work focuses on the channel doping concentration variation and the integration of high-K dielectric material, and the device with high performance is evaluated by varying temperatures for high-temperature applications [9].

II. Device Structure

The 3D view of the proposed n-channel GAA nanowire FET and its cross-sectional view are shown in Fig. 1, respectively. The NWFET structure is designed with a fixed gate length of 20 nm, and a gate oxide thickness of 1 nm of high-k hafnium oxide (HfO_2) is employed. With the uniform doping, the acceptor doping concentration is varied from 1017/cm³ to 1019/cm³, and in the drain, the source channel region donor concentration is maintained fixed at 1020/cm³. Table 1 gives the device dimension and material configuration. The linear and saturation modes are operating at a voltage VDD of 0.1V and 0.75V, respectively. The N-type GAA NWFET work function is considered to be 4.7 eV, and temperature is varied from 300K to 500K. The proposed device parameters and specifications are shown in Table 1.

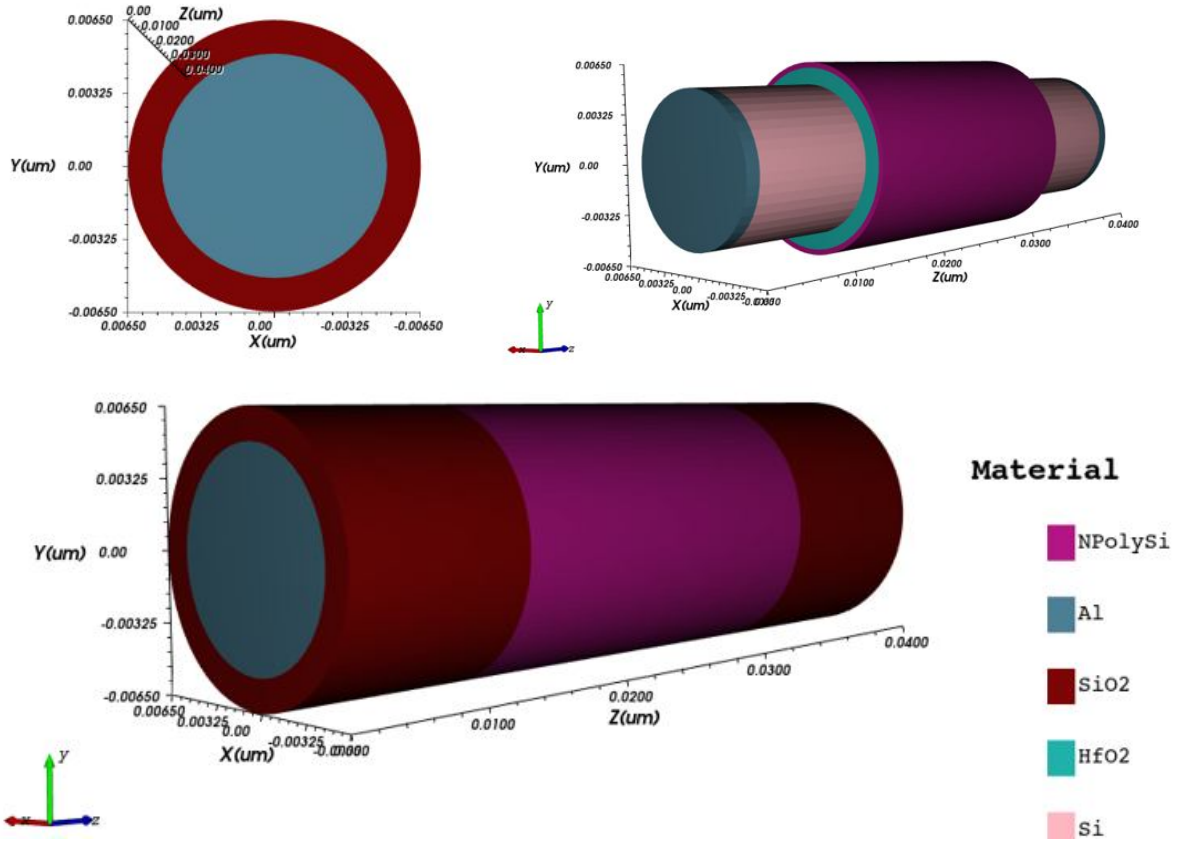

Fig.1 GAA Nanowire FET (A) Top view (b&C) 3D side view

TABLE I. PROPOSED DEVICE PARAMETER AND SPECIFICATION

Parameters	Device Dimensions
Oxide thickness(t_{ox})	1nm
Diameter of Nanowire(t_{nw})	22nm
Drain Length(L_s)	10nm
Source Length(L_s)	10nm
Gate metal work function(Φ_m)	4.7 eV
Channel length (L_g)	20nm
Doping of Channel Region N_D(/cm^{-3})	1x10^{19} cm^3

The analog RF analysis is carried out through a visual TCAD tool with the Lombardi mobility, Poisson equation, and drift-diffusion model for quantum correction in the sub-threshold region. The Lombardi unified mobility model is used, and the total mobility is written as:

$$\frac{1}{\mu t} = \frac{1}{\mu b} + \frac{1}{\mu ac} + \frac{1}{\mu sr} \quad (1)$$

III. RESULT AND DISCUSSION

The GAA NWFET DC transfer characteristics are obtained with drain current with a gate voltage ramp from 0V to 1V by keeping VDS voltage at 0.1V for the linear region, as shown in Fig. 2a, and for VDS = 0.75V for the saturation region, as shown in Fig. 2b, and compared with all three models, the doping concentration of 10^{19}/cm^3 in the linear and saturation regions shows the better OFF current with 10^{-15}A, and for ON current, the doping concentration of 10^{17}/cm^3 gives better results with 10^{-4}A, and the remaining models give the same result in the range of 10^{-5}A. Fig. 3 shows the drain current with the drain-source voltage ramp from 0V to 1V by keeping the gate voltage constant at 0.1V for the linear region shown in Fig.3a and keeping the gate voltage constant at 0.75V for the saturation region shown in Fig. 3b. Both regions show the drain current is saturated with a small gate voltage. The device performance of all three models is evaluated by using DIBL and SS parameters in the nanometer node. In the semiconductor device, DIBL is used to measure and control the threshold voltage reduction, and OFF current characteristics are measured with the SS. All the parameters' metrics, like DIBL, SS, and VTH, are calculated and compared for all three models, as shown in Table 2. The doping concentration of 10^{19}/cm^3 device performance provides better results.

TABLE II. PERFORMANCE METRICS EVALUATED FOR DOPING CONCENTRATION FROM 1X10^{17}CM^{-3} TO 1X10^{19}CM^{-3}

Doping Concentration	Vth Lin (V)	Vth Sat (V)	DIBL (mV/dec)	SS Lin (mV/dec)	SS Sat (mV/dec)
1X10^{17}cm^{-3}	0.379679	0.314102	10.08	60.6237	59.2604
1X10^{18}cm^{-3}	0.370767	0,374435	9.7	60.8065	60.5482
1X10^{19}cm^{-3}	0.434309	0.427682	10.19	59.5784	58.676

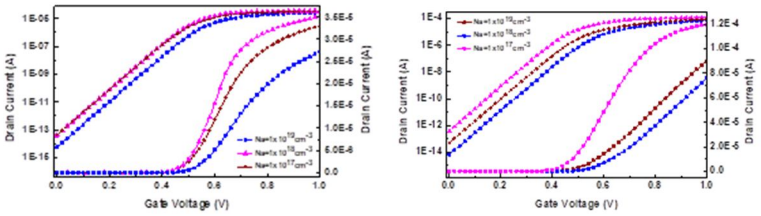

Fig.2 I_D-V_G characteristics(a) linear region and (b) saturation region

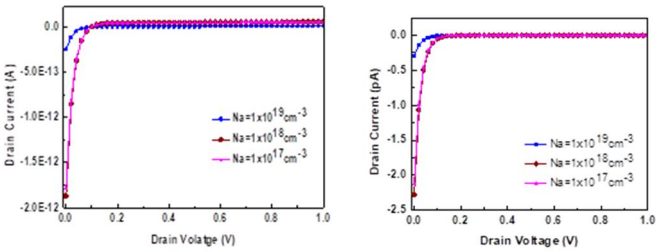

Fig. 3 I_D-V_{Ds} characteristics(a) linear region (b) saturation region

For measurement of device amplification, transconductance (Gm) effectively converts the voltage into current. This parameter is evaluated by a change in drain current (ID) to change the gate-to-source (VG) voltage by keeping the VDS value constant. It is expressed in equation 2.

$$Gm=\frac{\delta Id}{\delta Vg} \tag{2}$$

Fig. 4a and 4b show the Gm plot for the linear and saturation regions of all three models with VDS constant at 0.75 and 0.1, respectively, and Vgs is varied from 0 to 1V. The plot displays a peak Gm of all three models, and a doping concentration of 10^{17}/cm³ gives the better results at VG = 0.6 V and ensures better gain and amplification capability.

Output conductance (Gd) is used to measure the device's efficiency by effectively converting voltage into current. This parameter is evaluated for AC investigation by changing the drain current to change the source voltage by keeping VGS constant. It is expressed in equation 3.

$$Gd=\frac{\delta Id}{\delta Vd} \tag{3}$$

The output conductance plot for all three models is represented by Fig. 5 by plotting the Gd with VDS to set 1V and comparing it with all three models; doping concentrations of 10^{17}/cm³ and 10^{18}/cm³ provide the best results with 6E-11, a low Gd value. This implies getting better channel length modulation and DIBL by improving the inherent gain for analog applications.

Intrinsic gain (Av) is to calculate the maximum voltage gain of the device by the ratio of transconductance (gm) and output conductance (gd). Fig. 6 shows the intrinsic gain concerning gate voltage (Vgs) with drain bias fixed at saturation 1V. It is expressed in equation 4.

$$AV=\frac{Gm}{Gd} \tag{4}$$

In Fig. 6a, all the models are compared, and the doping concentration of the 10^{19}/cm³ model gives a higher gain of 6.49 at a gate voltage of 0.66V. The other two models with doping concentrations of 10^{18}/cm³ and 10^{17}/cm³ have small gains of 1.9 and 1.2, respectively.

$$Ve=\frac{Id}{Gd} \tag{5}$$

Fig. 6b displays the early voltage variation for all the models, and a doping concentration of 10^{19}/cm³ and 10^{18}/cm³ gives a higher voltage value of 2.5 V.

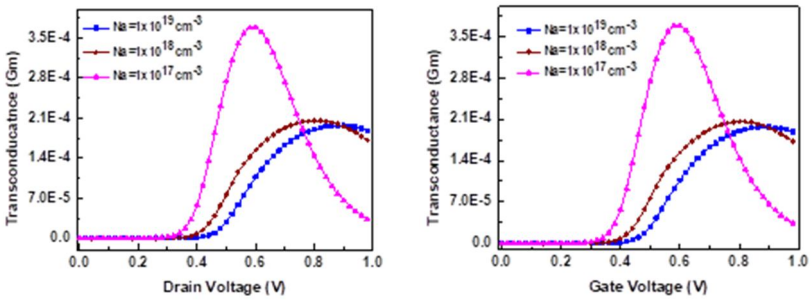

Fig. 4 Transconductance plot (a) at V_{DS} =0.1 V (b) at V_{DS} =0.75 V

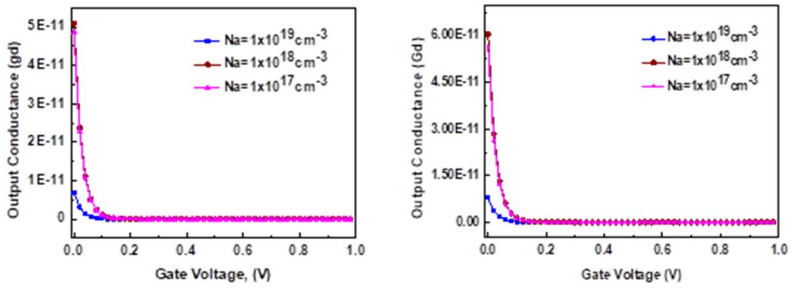

Fig. 5 Output conductance (a) linear region (b) saturation region

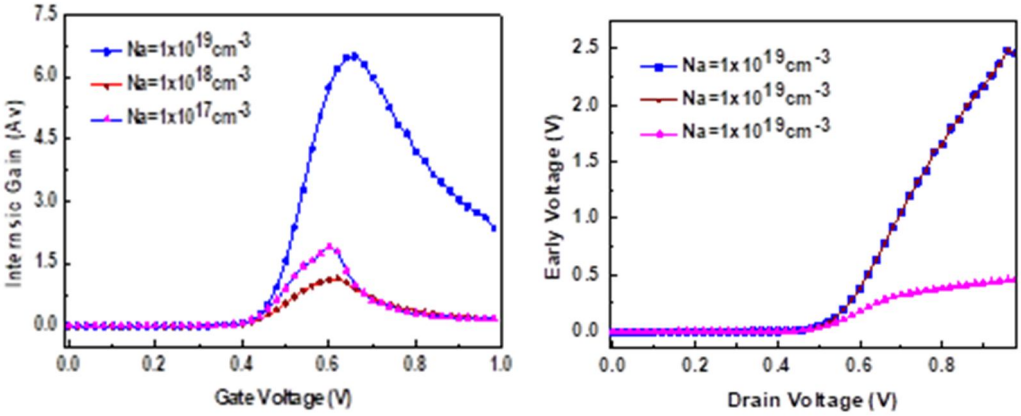

Fig. 6 (a) intrinsic gain (b)Early voltage

TABLE III. I_{ON}/I_{OFF} RATIO FOR LINEAR REGION

Doping concentration	Region	Ioff (A)	Ion (A)	Ion/Ioff ratio
$1X10^{17}cm^{-3}$	Linear	4.05E-14	3.52E-05	8.70E+08
$1X10^{18}cm^{-3}$	Linear	4.29E-14	3.31E-05	7.72E+08
$1X10^{19}cm^{-3}$	Linear	5.61E-15	2.72E-05	4.84E+09

TABLE 4. I_{ON}/I_{OFF} RATIO FOR SATURATION REGION

Doping concentration	Region	Ioff (A)	Ion (A)	Ion/Ioff ratio
$1X10^{17}cm^{-3}$	**Saturation**	3.80E-13	1.20E-04	3.16E+08
$1X10^{18}cm^{-3}$	**Saturation**	5.18E-14	9.02E-05	1.74E+09
$1X10^{19}cm^{-3}$	**Saturation**	6.66E-15	7.62E-05	1.14E+10

Tables 3 and 4 show the performance parameter I_{ON}/I_{OFF} ratio is compared with all three models both in linear and saturation regions. The doping concentration of $1X10^{19}$cm-3 provides good results with low off-current E-15, and all the models give approximately the same result around E-05 for ON current. Due to low IOFF current, the device provides a better I_{ON}/I_{OF}F ratio with 4.84E+09 and 1.14E+10 in linear and saturation regions. All these devices provide a high I_{ON}/I_{OFF} ratio, and it is used for higher switching devices.

A. Temperature analysis

The performance analysis is carried out with different doping concentrations from $1x10^{17}cm^{-3}$ to $1x10^{19}cm^{-3}$, and the device with doping concentration $1x10^{19}cm^{-3}$ provides better results with higher gain and a high I_{ON}/I_{OFF} ratio. In the future, the same device will be evaluated with higher temperatures from 300K to 500K, as shown in Table 5. Table 5 shows the threshold voltage decreases as the temperature increases, and in the same way, DIBL is increased by 48% and 35% at 400K and 500K compared to 300K. The subthreshold swing is also increased by 15% and 26% at 400K and 500K compared to 300K.

The device performs better at room temperature with a better threshold voltage, low DIBL, and low subthreshold swing. For higher temperatures, the secondary effect is exponentially increased. To mitigate these secondary effects, consider the use of different high-K materials, dual-K dielectric materials to reduce the leakage current, and better thermal stability materials. Also, optimization of the device architecture by proper scaling dimension consideration.

TABLE V. PERFORMANCE METRICS EVALUATED FOR HIGHER TEMPERATURE WITH DOPING CONCENTRATION $1X10^{19}CM^{-3}$

Temperature(K)	Vth Lin (V)	Vth Sat (V)	DIBL (mV/dec)	SS Lin (mV/dec)	SS Sat (mV/dec)
300K	0.434309	0.427682	10.19	59.5784	58.676
400K	0.371042	0.351844	29.5	81.09	79.652
500K	0.306881	0.291222	24.09	101.54	100.405

Tables 6 and 7 show the performance parameters like I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} ratio compared with higher temperature from 300K to 500K with device $1x10^{19}$cm-3 doping concentration in both linear and saturation regions. The table shows that as the temperature increases, the OFF current increases and the ON current is almost the same, so the I_{ON}/I_{OFF} ratio decreases and leads to more leakage current in the device.

TABLE VI. I_{ON}/I_{OFF} RATIO FOR LINEAR REGION

Temperature(K)	Region	Ioff (A)	Ion (A)	Ion/Ioff (10^3)
300K	Linear	5.61E-15	2.72E-05	4.84E+09
400K	Linear	1.95E-12	2.83E-05	1.45E+07
500K	Linear	6.60E-11	2.87E-05	4.35E+05

TABLE VII. I_{ON}/I_{OFF} RATIO FOR LINEAR REGION

Temperature	Region	Ioff (A)	Ion (A)	Ion/Ioff (10^3)
300K	Saturation	6.66E-15	7.62E-05	1.14E+10
400K	Saturation	2.83E-12	8.56E-05	3.02E+07
500K	Saturation	8.51E-11	7.93E-05	9.32E+05

IV. CONCLUSION

The designed 20nm GAA NWFET was simulated and analyzed with the three doping concentration models with HfO_2 as a dielectric material. All these models perform better with ION, IOFF, ION/IOFF ratio, SS, and DIBL. The doping concentration of 1x1019cm-3 gives excellent results with a low subthreshold swing that is almost equal to Boltzmann's trinity and better gate control by providing a low leakage current. Improved intrinsic gain with 6.49 and an excellent ION/IOFF ratio with 4.84E+09, so it provides a higher switching ratio used for RF applications. Furthermore, the model is evaluated for high temperatures from 300K to 500K, and the electrical characteristics for room temperature (300K) for the doping concentration $1019cm^{-3}$ produce significant results.

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