

A Novel Optimized Eleven Level Hybrid Cascaded Multi-Level Inverter

Satish kumar S¹, Dr M. Sasikumar² and Kavitha Kumari K S³

¹ Assisnant Professor, Department of EEE, Academy of Maritime Education and Training (AMET) Deemed to be University, Chennai-603112, India

¹ Research Scholar, Sathyabama Institute of Science and Technology, Chennai-600119, India
Email: satishkumarjec@gmail.com

² Professor, Department of EEE, Jeppiaar Engineering College, Chennai – 600 119, India
Email: pmsasi77@gmail.com

³ Assistant Professor, Department of EEE, Aarupadai Veedu Institute of Technology, Vinayaka Mission's Research Foundation, Chennai-603104, India
Email: kavithaksee@gmail.com

Abstract—In recent years, Cascaded H-Bridge multilevel inverter is preferred in many of the industrial applications. Cascaded H-bridge multilevel inverter (MLI) topology became an incredibly main preference in the area of high power medium voltage control. In the conventional system, seven levels AC output voltage is obtained by using eight switches with appropriate gate signal design. The conventional system is controlled by the Sinusoidal Pulse Width Modulation (SPWM) technique. The proposed multilevel inverter generates eleven level AC output voltage with reduced number of switches. The control technique used here is Sinusoidal Pulse Width Modulation (SPWM) technique by TMS320LF2407 digital signal processor (DSP). The main advantage of this technique is reduced harmonic distortion, reduced number of switching power devices and decreased switching losses. The voltage stress in the power devices can be reduced in the proposed system. The conventional multilevel inverter (MLI) and proposed Modified Cascaded H Bridge Multi Level Inverter (MCHBMLI) are simulated to compare their Total Harmonic Distortion.

Index Terms— Multilevel inverter (MLI), Cascaded multilevel inverters (CMLI), Modified Cascaded H Bridge Multilevel inverter (MCHBMLI), Pulse Width Modulation (PWM), Sinusoidal Pulse Width Modulation (SPWM) Total harmonic distortion (THD).

I. INTRODUCTION

Nowadays much industrial application has preferred customised CMLI for the high power applications. The harmonic content in which the HMLI in turn reduces the size, cost of the filter and the level of electromagnetic interference (EMI) generated by switching operation. The multi level inverters are classified as Diode clamped multilevel inverter, cascaded multilevel inverter and Flying capacitor multilevel inverter. Cascaded multilevel inverters are most preferable since it overcomes the other two types of inverters in the following ways. The features of CMLI are Multilevel inverters are generally used in industrial applications. And they are used in the areas where we need medium voltage high power application [1-3]. The key function of inverter is the switching frequency. To convert DC signal into a AC signal, we require a fast switching of DC signal giving us multiple

levels. This turns into a staircase wave that is quite close to a sine wave. The difference between a simple inverter and a multilevel inverter is as follows.

One of the basic and well known topologies is cascaded H-bridge multilevel inverter. It can be used for both single and three phase conversions. The circuit consists of diodes and switches. This is the most common type of inverter and usually uses separate DC sources (SDCs).the concept of this inverter is based on connecting H-bridge inverter in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The voltage levels are obtained with the formula used in $2n+1$, where n is the number of cells. One of the advantages is that it needs less number of components comparative to diode clamped or the flying capacitor[4-7], so the price and the weight of the inverter is less than that of two former types. Advantages are it does not need any diodes or capacitors for clamping. The wave is quite sinusoidal in nature even if don't filter it.

The main advantages of cascaded H-bridge inverter are that it requires least number of components and soft switching can be used. But the main drawback is that when the voltage level increases[8-10], the cost and weight increases due to increase in number of sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcome in cascaded H-bridge inverter.

II. CONSERVATIVE HYBRID CASCADED FIVE LEVEL INVERTER

The figure shows the CHBMLI with a separate DC source. The MLI has designed with four MOSFET devices with add on one switch to obtain the required output voltage in 5 level.

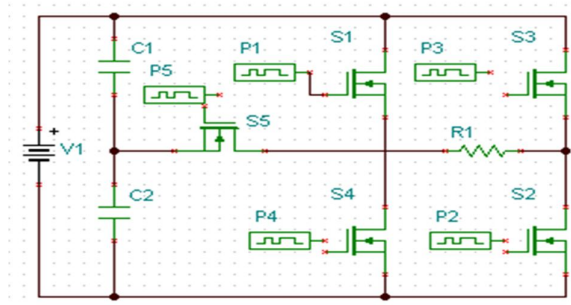


Figure 2.1: Hybrid Cascaded H Bridge Multi level inverter

The above circuit consists of 5 switches, Inhere with 4 switches are general purposes switches and add on single to obtain the require output using the MLI circuit

. The importance of add on switch to obtain the reverse polarity in a CHMLI. The traditional cascaded MLI huge no of switches are required to satisfy the required the output[11-12]. Once the number of switches reduced in the proposed circuit the switching losses also reduced The proposed topology Optimised PWM methods are used to reduce the harmonics.

The proposed topology implement in CMLI for obtaining the same five-level output is available in the literature. The output voltage of the HCMLI can have five possible values $0, V_{dc}, 2V_{dc}, -V_{dc},$ and $-2V_{dc}$. The advantages of this topology are:

- Reduced number of switches.
- Higher speed capability
- Low output switching frequency
- Low switching loss
- High conversion efficiency

III. SUGGESTED HYBRID CASCADED ELEVEN LEVEL INVERTER

The Suggested topology is simple in enterprise and compared to the existing topologies, it consists of two dc sources and five switches. It also has additional features like only two switches directing at an interval of time. One switch is used for polarity reversal and the remaining four switches are used for waveform generation. The widespread expression for the number of switches and the number of dc sources for the suggested topology is given by:

$$\text{Number of switches} = (N+5)/2$$

A proposed system generates eleven level output with appropriate gate signal design. This system reduces the switching losses and harmonic distortion with the reduced number of switches. Here, eight switches are used to generat eleven level AC output voltage.

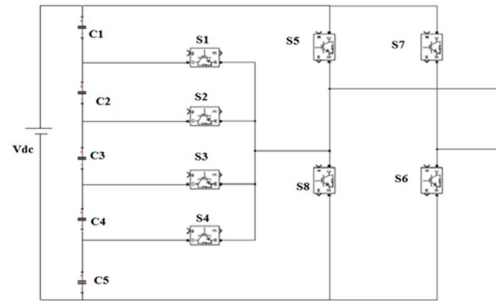


Figure 3.1: Suggested HCMLI

Fig 3.1 shows the novel customised topology used in the eleven level inverter. The input voltage divider is composed of five series capacitors C1, C2,C3,C4 and C5. The divided voltage is transmitted to H-bridge by four IGBT. The output voltage observed across the switches.. The proposed multilevel inverter generates eleven levels AC output voltage with the appropriate gate signals design.

$$\text{Number of voltage sources, } V = (N-1)/2$$

$$S = (N+5)/2$$

Where N= number of levels

S= number of switches and

V=number of dc voltage sources.

The required eleven voltage output levels ($\pm 5V, \pm 4V, \pm 3V, \pm 2V, \pm V, 0$) are generated as follows:

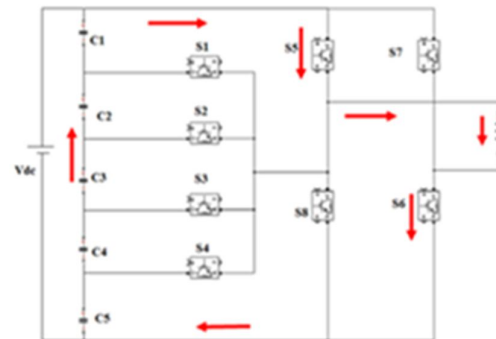


Fig.3.2 (a) Mode 1

In the first mode the output voltage level is equal to 5V, S5 and S6 is enable at the moment of the positive half cycle. Power is observed through the voltage balancing circuit and the direction of current flow in this mode.

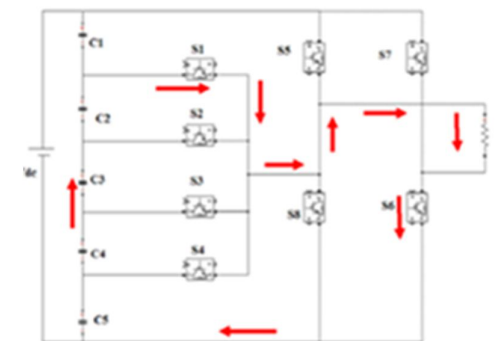


Fig.3.2 (b) Mode 2

In the second mode, the output voltage level is equal to 4V, S1 and S6 is enable at the moment of the positive half cycle. Power is observed through the voltage balancing circuit. Fig.3.2.(b) shows the direction of current flow in this mode.

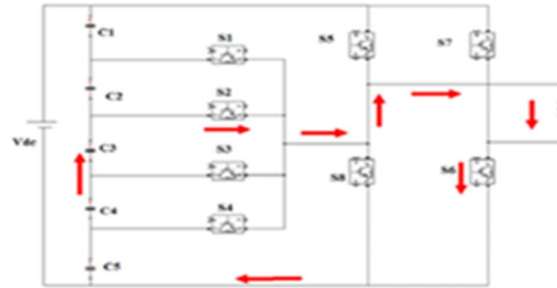


Fig.3.2(c) Mode 3

In the third mode the output voltage level is equal to 3V, S2 and S6 is enable at the moment of the positive half cycle. Power is observed through the voltage balancing circuit and also Fig..3.2.(c) shows the direction of current flow in this mode.

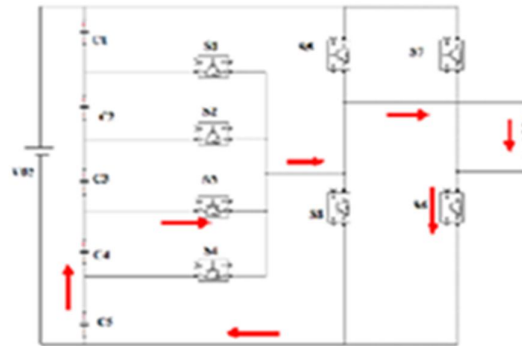


Fig.3.2 (d) Mode 4

In the fourth mode the output voltage level is equal to 2V, S3 and S6 is enable at the moment of the positive half cycle. Power is observed through the voltage balancing circuit Fig..3.2(d) shows the direction of current flow in this mode.

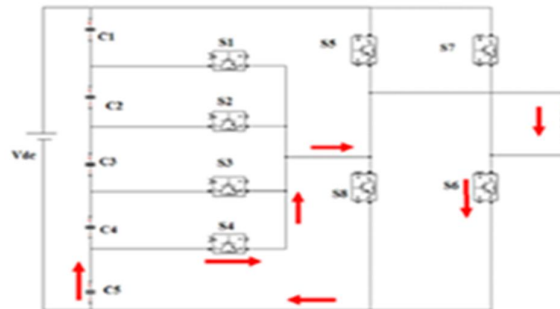


Fig3.2(e) Mode

In the fifth mode the output voltage level is equal to V, S4 and S6 is enable at the moment of the positive half cycle. Power is observed through the voltage balancing circuit .Fig..3.2.(e) shows the direction of current flow in this mode.

The modified cascaded multi level inverter has been enabled the switches as per the mention sequence to obtain the required output voltage. The positive and negative half cycle the half cycle level are equally distributed as

TABLE I: SWITCHING SEQUENCE OF MLI

S,no	S1	S2	S3	S4	S5	S6	S7	S8	Output voltage
1	0	0	0	1	0	1	0	0	$V_{dc}/5$
2	0	0	1	0	0	1	0	0	$2V_{dc}/5$
3	0	1	0	0	0	1	0	0	$3V_{dc}/5$
4	1	0	0	0	0	1	0	0	$4V_{dc}/5$
5	0	0	0	0	1	1	0	0	V_{dc}
6	0	0	0	1	0	0	0	1	$-V_{dc}/5$

per the sequence order .So the Proposed MLI gives the eleven level output voltage with educed switches with minimise the harmonics.

IV. HPWM TOPOLOGY

The Optimized novel HPWM topology is, the combination of carried and reference with the required the pulse generation [4-6] In suggested topology the generation of pulse to ignite the operation of switching devices, the designed HPWM signals generated to obtain the output voltages. The switching pattern are obtained with the combination of carrier signal and reference signal. The carrier signal V_c would be compared with V_{ref} until V_{ref} reaches zero. This results in the producers of required swapping pattern as shown.

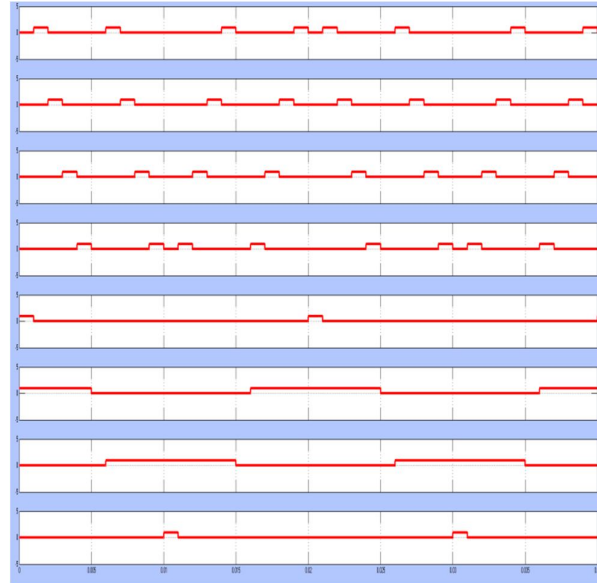


Figure 4.1: Hybrid PWM pulse generation Scheme

V. SIMULATION RESULTS

The Optimized novel eleven level cascaded multi-level inverter operation and the voltage and current waveform of CHMLI are verified and compared the intended value The simulation diagram of Novel Hybrid Cascaded H bridge multi level inverter is shown in Figure 51.

The switches are used in novel optimized multi-level inverter and voltage balancing circuits. The MOSFET switches are preferred to use in CMLI circuit, In these switches one of the switch be operated in bidirectional and others be operated in unidirectional and the resistive load is taken as 100 ohms. The dc source voltage is taken as 100V.

The novel CHMLI circuit diagram as shown in the fig5.1 the designed circuit to obtain 11 level output voltage with the reduced number of switches The Matlab Simulink is executed and verify the output voltage and current waveform and also THD calculated using FFT analysis.

The voltage and current waveform of novel optimize CHMLI as shown in fig5.2 the output voltage waveform in staircase in nature we try to obtain the waveform in smooth sinusoidal waveform The level of output voltages

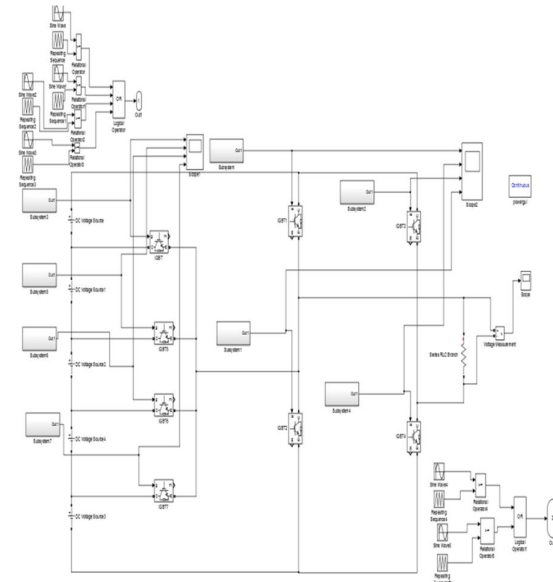


Figure 5.1: Simulation diagram for Novel CMLI

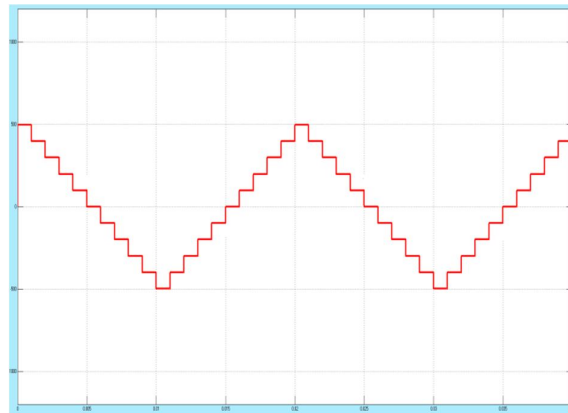


Figure 5.2: Output Voltage and Current waveform for HCBMLI

peak to peak voltages is nearly 5V. The Hybrid modulation technique is incorporated in the circuit with the help of HPWM schemes. The FFT analysis used to obtain the THD value and verified with calculated once.

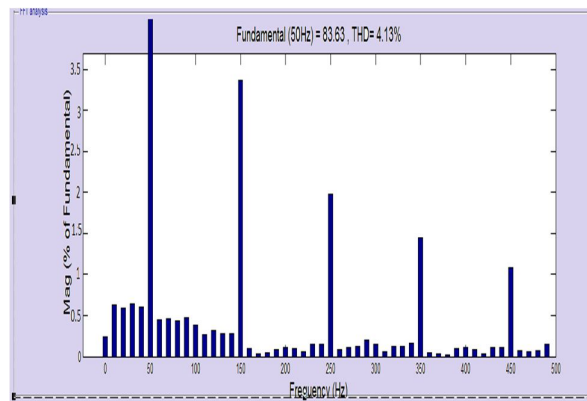


Figure 5.3: HCBMLI THD analysis

The suggested novel optimized HCMLI is executed and calculated the THD value using Fast Fourier Transform (FFT) analysis is show in figure 5.3. THD is 4.46% with a fundamental frequency of 50 Hz for its output voltage.

VI. CONCLUSION

Optimized HCMLI has been designed with pulse generation using hybrid PWM topologies. The bidirectional switches are used to obtain the swapping the polarity of the supply with separated DC sources. The optimized HPWM topology for harmonic reduction is simulated using MATLAB/SIMULINK. The THD analysis for the designed CMLI is obtained with fundamental frequency of 50Hz. The suggested methodology is incorporated with the less number of switches with voltage balancing circuit. The future scope of the CMLI smoothening the wage form and less THD value for the electric vehicle application.

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AUTHORS PROFILE



Mr. S. Satish Kumar has received the Bachelor degree in Electrical and Electronics Engineering from Manonmaniam Sundharanar University, Tirunelveli Tamilnadu, India in 2000 and completed his Master of Engineering in Power Electronics and Industrial Drives from Sathyabama University, Chennai Tamilnadu India in 2007. He is pursuing the Ph.D. degree in the faculty of electrical engineering. His area of interest includes in the fields of power converter with soft switching PWM schemes. He is currently continuing his carrier in the Department of Electrical and Electronics Engineering in AMET Deemed to be university Chennai. He has published 15 research papers in referred International Journals and 20 paper presented in National journals.



Dr. M. Sasikumar has received the Bachelor degree in Electrical and Electronics Engineering from K.S. Rangasamy College of Technology, Madras University, India in 1999, and the M.Tech degree in power electronics from VIT University, in 2006. He has obtained his Ph.D. degree from Sathyabama University, Chennai in 2011. Currently he is working as a Professor in Jeppiaar Engineering College, Chennai Tamilnadu, India. His area of interest includes in the fields of wind energy systems, Hybrid systems and power converter and and Head soft-switching techniques. He is a life member of ISTE.



Mrs.K.S.Kavitha Kumari received Bachelor of Engineering Degree in Electrical and Electronics Engineering from Priyadharshini Engineering College , Anna University Chennai in 2005 , Master degree with Power System Engineering from Velammal Engineering College, Anna University in 2007 and pursuing phd in Sathyabama Institute of Science and Technology, Chennai. Currently she is working as Assistant Professor in Department of Electrical and Electronics Engineering , Aarupadai Veedu Institute of Technology, Chennai. Her area of interest includes Smart grid, micro grid, Flexible AC Transmission systems , power system operation and control and Application of power electronics in power system.