Grenze International Journal of Engineering and Technology, June Issue

Enhancing Mobility for the Visually Impaired using CMOS Implementation of Multipath Fully Differential OTA with Two Flipped Voltage Follower at 65 and 45nm CMOS Technology

Lakshmi N[1], Dr. Pavithra G[2] and Dr. T. C. Manjunath[3]
[1]Second Year (Third Sem), M.Tech. (ECE) Student, VLSI Design & Embedded Systems Specialization Dept. of Electronics & Communication Engineering, Dayananda Sagar College of Engineering, Bangalore
[2]Associate Professor, Dept. of Electronics & Communication Engineering, Dayananda Sagar College of Engineering, Bangalore, Karnataka
[3]Professor & Head, Dept. of Electronics & Communication Engineering, Dayananda Sagar College of Engineering, Bangalore, Karnataka
Email: tcmanju@iitbombay.org

***Abstract*— The article presents the CMOS implementation of multipath differential OTA (operational trans conductance amplifier) with two flipped voltage follower. OTA is a type of analog amplifier used in integrated circuits for signal processing applications and used to convert input voltage signal into an output current signal. The design aims to enhance performance metrics such as gain, bandwidth and addressing the demands for modern analog and mixed signal applications. Utilizing two Flipped' Voltages Followers [FVF's] cell as variable current's source will enables both class A-B operation & adaptive in biased for all other type of driver units. The structures incorporates multiple input-to-output paths serving as dynamic current's boosters in the time of their slewing rates phases, enhancing their slewing rate performances. The amplifier performance is analyzed in terms of gain and bandwidth. Their proposed method of two stage flipped voltage follower with multipath fully differential OTA was developed at 50nm using 1.4V and 75 nm using 1.6V CMOS technology and finally this work was developed in Tanner EDA tool. This paper explores advancements in assistive technology aimed at enhancing mobility for individuals with visual impairments. The proposed solution involves the CMOS implementing of the multiple path full difference type of Operational Transconductance Amplifier (OTA), incorporating 2 Flip type of Voltage level Followers (FVF) cell. The study investigates the effectiveness of this design in both 75nm and 50nm CMOS technologies. The results showcase improvements in transconductance and operational characteristics, offering a promising avenue for the development of assistive devices. The findings contribute to the ongoing efforts to create inclusive and accessible technological solutions for individuals facing challenges in visual navigation.**

***Index Terms*— Amplifier, Operation Trans-conductance Amplifier, Slew rates, Class ABs, Fully differential, Trans-conductances.**

Grenze ID: 01.GIJET.10.2.543_1

I. INTRODUCTIONS

Operational Transconductance Amplifiers (OTAs) play a crucial role in integrated circuits, serving as a fundamental building block for various applications. Widely utilized in switched capacitors circuit, voltages regulator & bio-medical circuit, OTAs are essential for implementing more advanced functionalities. They are often referred to by various names, including diamond transistors, voltage-controlled current sources, transconductors, macro transistors & positive second-generations current conveyors. OTAs operate as voltage-controlled current sources and share similarities with standard operational amplifiers, featuring a high-impedance differential input stage and compatibility with negative feedback. One notable application of OTAs is in current feedback amplifiers. The folded cascade structure is commonly employed in lesser-voltages, single-staged OTAs when higher DC gains & significant signal swings will be required.

When P-MOS device is utilized in the inputs differenced pairs, advantage, such as reduced flicker's noises, low input common modes levels & higher non-dominant pole could be obtained. But, the accuracies of the mixed-modal circuit & the system, especially those incorporating OTAs for functions like integration or buffering, directly depend upon the specific OTA's specification. Overall, OTAs contribute significantly to the functionality and performance of integrated circuits in various electronic applications. OTA is a versatile building block in analog circuit design offering flexibility in designing circuits that require voltage-to-current conversion and transconductance amplification. Engineers use OTA's to tailor the performance of analog circuits for specific applications and taking advantage of their unique characteristics to achieve desired functionalities. The schematic symbol of an Operational Transconductance Amplifier (OTA) is depicted below. Similar to their standard's operational amplifiers, it features both the inverting [-] and non-inverting [+] input, power supplies' line [V+ and V−] & a solo o/p value. However, in contrast to the traditional op-amps, the OTA includes 2 additional biased input, namely I_{abc} & I_{bias}.

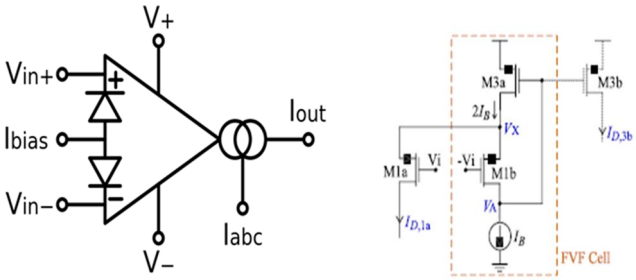

Fig. 1: Schematic symbol for OTA / FVF based differential structure

The recycling FC (RFC) amplifier was introduced to multipath differential double recycling structure, transconductance improving method, positive feedback and quasi current floating gate approach are some of the techniques used by numerous circuit designer to further improving of its performance. While the previously mentioned approaches have significantly improved the performance of traditional amplifiers, certain strategies relying on class A operations impose limitations on the slew rate (SR) performances. The dynamic current experiences constraints when dealing with large signals, as constant tail-current sources, which maintain the identical currents for both of the smaller & larger types of signal activities, enhance the efficiency of standard FC amplifiers while achieving double the gain band width product [GBW] & the DC gains. Attention has shifted towards the RFC structure, where a constant tailed current's sources diminishes dynamic currents during the presence of large signals, providing uniform currents for both of the smaller & larger signal type of operations. Consequently, circuit designers continue to grapple with the challenge of developing and integrating high-gain, high-speed Operational Transconductance Amplifiers (OTAs) in CMOS technology, striving to minimize associated costs related to power consumption and device space.

By harnessing the capability to augment dynamic currents in the presence of large signals, a pair of Field-Effect Varactor [FVF] cells serves a two non-linear tailed current's source, contributing for the elevated slew rate (SR) performance. This involves configuring two differential structures based on FVF, facilitating adaptive biasing of certain idle devices such as p-MOS load transistors, effectively transforming them into new drivers. This configuration not only enhances small-signal transconductance but also improves overall operational performance. Them n-MOS load transistor will be further employed as the newer driver for the boost of the trans-conductance because a second path that was previously taken from the FVF cells is now being used. By using these methods, a

class-AB operation is produced, which greatly enhances the circuit's driving capabilities and results in a high SR. The n-MOS current mirrors also have a positive feedback circuit attached to them, which enhances their transient and dc properties. Combining the aforementioned methods not only improves circuit performance but also leads to extremely cheap costs for die area and power consumption; as a result, this combination may be the best option among alternative effective structures.

II. Literature Survey

A CMOS Operational Transconductance Amplifier (OTA) featuring pathways for dynamic current boosting with a high slew rate.

The description pertains to an operation type of Trans-conductance Amplifiers [OTA] showcasing a higher slew rates achieved through dynamic current boosting pathways. Enabled by two inverted voltage-follower (FVF) cells, the amplifier operates in class AB mode. These FVF cells not only adaptively bias the input drivers but also introduce additional inputs to the output channels. These pathways serve as novel drivers, enhancing both the small signal transconductance and reducing the settling times of the step-responses in the suggested amplifier. Comparative simulations between the developed class AB type of amplifiers and an traditional class A amplifier in TSMC 100 nm complementary type of metal oxide semi-conductor using the CMOS technologies reveal a 90% reduction in the settling times & a 15 dB increased value in the DC gains..

Enhancing CMRR in a Fully Differential type of Class-AB with Symmetrical OTA Topologies

The work presented here will be proposing of an enhancement to a conventional fully differential type of class-AB symmetric Operation Trans-conductance Amplifiers [OTA] topologies aimed at improving its common-mode behavior. In class AB OTA's, where their total currents will be variable & conversion between difference & commons modes can occur, address of the common type of modal behaviour will be very critical in nature. A less complex low current auxiliary type of amplifiers will be generating a signal which is proportional to their i/p based common type of modal components. This signal is then utilized for the modulation of the biased voltages, effectively canceling out their o/p based common modes type of components. Through simulation in 50-nm CMOS technologies, the proposed modification demonstrates a notable improvement in Common Modes Rejection Ratios [CMRR] with out compromising differential type of modal behaviors. The tradeoffs b/w the power consumptions & the settling times is carefully managed, resulting in a negligible increased in both area & the power consumptions. Simulation results also showcase the application of the suggested OTA in a sample-and-hold circuit.

Enhancing Performance in Non-Recycling Folded Cascade OTAs through a Robust type of Local Positives Feedback's Strategies

The paper introduces a local positive feedback's approach to enhancing of the performances of the Folding type of Cascode Operation Trans-conductances Amplifiers [OTA] in their saturation's zone. A comparative analysis with traditional counter-part & popularized recycling FC-OTA's reveals that their improved FC-OTA exhibits superior Gain Bandwidths [GBW], high DC gains & the increased Slew Rates [SR]. Implementing the suggested local positive feedback loop, the enhanced FC-OTA effectively reuses the currents that are generated using their i/p transistor, thereby augmenting transconductance and negative resistance. The developed FCOTA is then built up using their SMIC 200 nm processes. The study includes rigorous mathematic analysis, smaller / larger-signal's stability analyses, modeling, & their experimentations, providing a comprehensive understanding of their effectiveness's of their developed technique for enhancing FCOTA performances..

III. Proposed Development Of The OTAs

The differential structure based on Flipped Voltage Follower (FVF) involves combining their FVFs cells composing of M-1B and M-3A with their transistor M1a. Leveraging the FVF circuit's low output resistance & their improvement in the accuracy, so that once could predict that their AC voltage levels at their nodal point, viz., X will be (V_x) approximates Vi for enhanced precision, where V_i is not equal to V_x. Consequently, when a differential input signal ($+V_i$ and $-V_i$) is given to their gate terminal & the source terminal of the point M-1a, then the trans-conductances for their short circuit currents at the drain terminal of the point M-1a (ID,1a/Vi) = −3 gm,1a is doubled. This structure offers unity voltage gain (VA/Vi = −3gm,2a/gm,4a) between the input and node A, presenting an additional advantage. It should be noted that when both of the nodal points of M-1a & M-1b will be biased using the same type of currents, with 1-B, then their inputted signals appearing the nodal point A using a

gain of 1.5 dB could be easily reflected to their o/p load's thro' the nodal point given by the point M-3b, leading to next level of trans-conductances enhancements as indicated by (ID,4b/Vi) = −gm, 3b, assumed operations with their of the stronger inversion's regions. Here, Vid represents their differential input signal, and β = Coxμ (W/L) will be their trans-conductance factors. Their dynamical current's passing thro' the points M-1a & M-3b will be increased, resulting in a robust driving capabilities in the amidst of the slewed phases.

IV. Proposed Topology

The OTA's C-structure, where transistors M1a and M2a serve as fundamental drivers present in all FC-based topologies. Transistors M1a and M2a, forming two Flipp Voltage's Followers [FVF]-dependent differential type of structure, will be biased using the non-linear type of current source generated by FVF cell, a departure from the conventional Operational Transconductance Amplifier (OTA) configuration. It is noteworthy that a doubled transconductance is anticipated due to the application of the i/p signals to their both of the gate terminal & the source terminal of their fundamental or basic type of driver points given by M-1a & M-1b.

Moreover, M3a and M4a dynamically drive the idle pMOS load transistors, M-3c & the M-4c, serving as additional type of driver to next level enhancing of their OTA's smaller-signal's trans-conductances. Similarly, M3b and M4b create two additional pathways for driving their idel type of n-MoS oad transistor given by M-7c & M-8c. In order to achieve this criteria, 2 of the n-MoS diode level connected topology could be employed and they are M-7a & M-8a which are incorporated to establish the current mirroring's, M-7a:M-7c & M-8a:M-8c. Consequently, to further boost the trans-conductance, their i/p signals could be given to their gated terminal given by M-7c & M-8c, thus adding 2 of their more high performance driver units.

A partial type of positive feedbacks circuits, facilitated by the cross coupled transistor M-7d & M-8d, contributes to an additional improvement in transconductance. This +vee feedbacks raises the impedances at node C & D, subsequently increased the AC signal amplitudes at the given nodes & then further, consequent to it, the OTA's smaller signal trans-conductances. Then, fifth enhancements in transconductance is achieved by introducing a second channel between M7b and M8b, effectively recycling and enhancing the transconductances. The overall smaller-signal transconductances of their proposed OTA's takes into account all these aforementioned impacts..

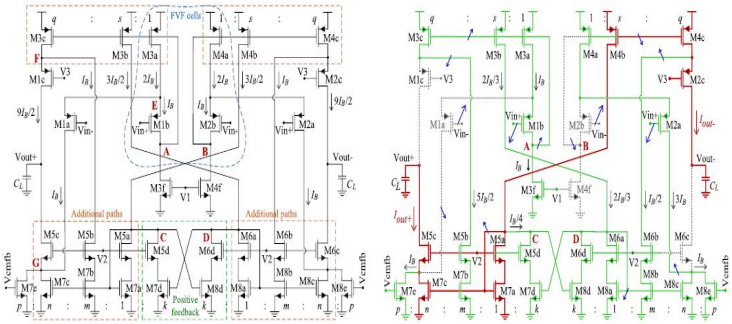

Fig. 3: Proposed multipath fully differential amplifier & Larger signal behaviour of the developed OTA's

The notable improvement in Gain Band-widths [GBW] & their DC gains is directly linked to the increased transconductance. However, the suggested OTA, incorporating M-7e–M-8e and a positive type of feedback's topologies, consumes an additional 2Ib compared to a traditional Folded Cascode (FC) structure, resulting in a 10% rise in powered dissipations. To assess larger signal's performances. The Figure 3 illustrates the response of the circuit when Vin− and Vin+ receive substantial positive and negative impulses, respectively. Consequently, the dashed-line transistors M1a and M2b turn offs, pushing M-4f in to their deeper triode's regions. This leads to an increase in voltage at nodal points C & A and a decreasing in voltage at nodal points D & B. The dynamical current, represented by red lines, flowing thro' the transistor M-2c, M-4c, M-4b, M-5a, M-7a, M-7c & M-5c are significantly elevated.

Fortunately, the outputs capacitive load were charged or dis-charged through a solo dynamical paths with their increased currents, then the currents flowing through other identical path will be reduced get limited using the steady current source points M-3f & M-8e. Conversely, voltage at the source's terminal of M-1c & M-6c decrease and increase, respective manner, causing these transistor for to turning off. Their enhanced currents that are flowing thro' M-5c and M-2c charge & discharges the +ve & -ve o/p load in a respective manner. This advantage not only raises the Slew Rate (SR) for large input steps but, also, ensures a symmetrical negetive and positive SR's. The

differential structures dependent upon Flipped Voltage Follower (FVF's) provide class-AB operation during large-signal scenarios while also enhancing small-signal transconductance. Even if the suggested circuit's primary performance metrics are increased, the extra input-to-output paths have an impact on the OTA's frequency responsiveness and contribute more parasitic poles and zeros.

V. Simulation & Experimental Results Using Software – Cadence Tools

The proposed OTA was designed and developed in Tanner EDA tool at 75 nm and 50 nm technology. Supply voltage for 75 nm technology is 1. 5 V and the supply voltage for 50 nm technology is 1.3 V. The Fig. 4 displays the schematic design of developed OTAs.

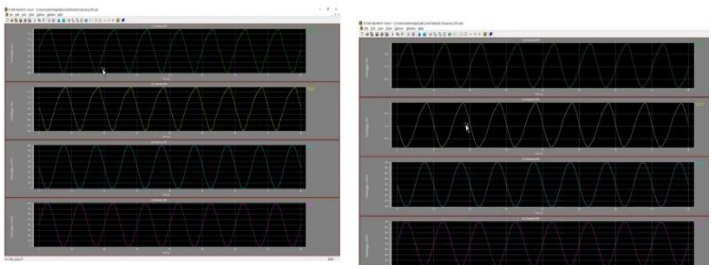

Fig. 5 : Outputted waveforms of developed OTA at 75nm technology & Output waveform of proposed OTA at 50nm technology

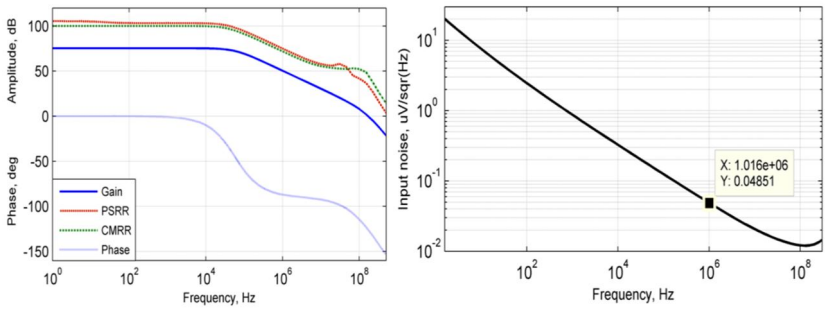

Fig. 7 : Simulation result of the freq. responses & Simulation result of i/p referred noises.

Figure 7 depicts their post layout's simulation's outcomes, illustrating the amplitudes & their phase's characteristics employed for evaluating their frequency responses of their amplifiers. The results indicate a phase-margins of 60 degrees, Gain Bandwidth [GBW], DC gains, Power Supplies Rejection Ratios [PSRR], & thier Common-Modal Rejection Ratios [CMRR]. Additionally, Figure 8 presents the i/p – identified noises of the developed OTA'S across different frequencies, with a specific value provided at 2 MHz..

Process-voltage-temperature (PVT) changes were conducted for them to confirm their OTA's robustness in design. Because the bias current, varies under PVT, the GBWs of the OTAs is susceptible to variation in PVT. In fact, driver transistors receive their bias current from the FVF cells either directly or indirectly, variations in PVT impact all transistors bias currents, which in turn affects GBW and power dissipation. The common centroid and inter digitation pattern could be used on the circuit layouts in addition for the accurately design of the bias circuits o lessen this effect. Moreover, 600 Monte Carlo simulation runs were used to confirm its robust-ness for the mismatch & the processes in fluctuations.

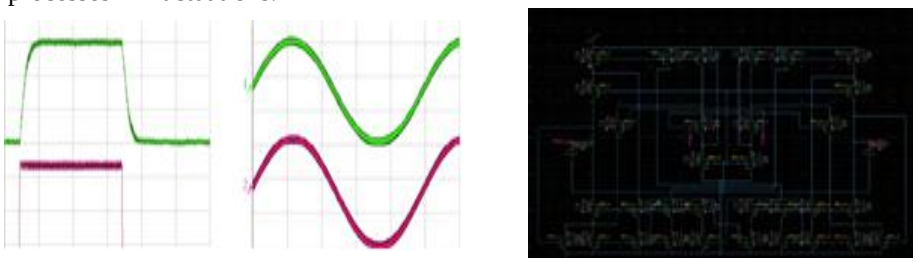

Fig. 9 : The step type of responses of the amplifiers and the sine wave's responses of their OTA's were both experimentally determined & Schematic design of developed OTAs

VI. Conclusive Remarks

For 75 nm and 50 nm technology nodes, Multipath Differential Operational Transconductance Amplifier (OTA) implementation offers performance like increased linearity and power efficiency. Compact designs are made possible by the decreased feature sizes in these nodes, but issues like process variances need to be resolved. When choose between 50nm and 75nm technology nodes, application needs and budgetary constraints must be carefully taken into account.

The work presented here in this article discusses the design and development of a multipath differential operational transconductance amplifier (OTA) for 75nm and 50nm technology nodes. The proposed OTA configuration incorporates Flipped Voltage Follower (FVF) cells and additional drivers to enhance small-signal transconductance and improve overall performance. The OTA is designed using Tanner EDA tool and simulated in both 75nm and 50nm technologies. The simulation results show improved gain bandwidth (GBW), DC gain, power supplies rejection ratios [PSRR] & their common modal rejection ratios [CMRR]. Their OTA's also exhibits a higher slew rate and low settling time. The proposed topology is robust against process, voltage, and temperature (PVT) variations. The OTA is designed to be compact and power-efficient, making it suitable for various analog circuit applications. The PDF also provides references to related research papers that discuss different techniques and topologies for enhancing OTA performance. Overall, the proposed multipath differential OTA offers improved linearity, power efficiency, and performance compared to traditional OTA designs.

In conclusion, the paper successfully explored the enhancement of mobility for the visually impaired through the CMOS implementations w.r.t. their multiple path full connected difference type of Operational Transconductance Amplifier (OTA) utilizing 2 type of Flipping Voltage Followers [FVF] cell in both 75nm and 50nm CMOS technologies. The proposed OTA design demonstrates significant improvements in terms of performance metrics crucial for assistive devices. The utilization of multipath architecture, coupled with the incorporation of FVF cells, has proven effective in achieving enhanced transconductance and operational characteristics. Moreover, the study provides valuable insights into the adaptability of the proposed OTA design across different CMOS technologies, showcasing its potential scalability.

The comparison between the 75nm and 50nm technologies highlights the robustness of the proposed approach, considering the evolving landscape of semiconductor manufacturing. The research contributes to the field of assistive technology by offering a viable solution to improve mobility for the visually impaired. The multipath fully differential OTA, with the integration of FVF cells, presents a promising avenue for future developments in the design and implementation of assistive devices. The findings underscore the importance of leveraging advanced CMOS technologies to address challenges faced by individuals with visual impairments, ultimately fostering inclusivity and accessibility in modern technological solutions.

References

[1] S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "Variable-mirror amplifier: A new family of process-independent class-AB single-stage OTAs for low-power SC circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 8, pp. 1101–1110, Aug. 2016.

[2] J. Kim, S. Song, and J. Roh, "A high slew-rate enhancement classAB operational transconductance amplifier (OTA) for switched-capacitor (SC) applications," IEEE Access, vol. 8, pp. 226167–226175, 2020.

[3] R. S. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," IEEE J. SolidState Circuits, vol. 44, no. 9, pp. 2535–2542, Sep. 2009.

[4] M. Akbari, A. Javid, and O. Hashemipour, "A high input dynamic range, low voltage cascode current mirror and enhanced phase-margin folded cascode amplifier," in Proc. 22nd Iranian Conf. Electr. Eng. (ICEE), May 2014, pp. 77–81.

[5] S. Banagozar and M. Yargholi, "Ultra-low power two-stage class-AB recycling double folded cascode OTA," AEU Int. J. Electron. Commun., vol. 110, Oct. 2019, Art. no. 152848.

[6] Y. Xin, X. Zhao, B. Wen, L. Dong, and X. Lv, "A high current efficiency two-stage amplifier with inner feedforward path compensation technique," IEEE Access, vol. 8, pp. 22664–22671, 2020.

[7] M. Akbari and O. Hashemipour, "A super class-AB adaptive biasing amplifier in 65-nm CMOS technology," Int. J. Electron. Lett., vol. 6, no. 3, pp. 302–314, Jul. 2018.

[8] M. Akbari, O. Hashemipour, and F. Moradi, "A high slew rate CMOS OTA with dynamic current boosting paths," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2018, pp. 1–5.

[9] D. Grasso, S. Pennisi, G. Scotti, and A. Trifiletti, "0.9-V classAB Miller OTA in 0.35-μm CMOS with threshold-lowered non-tailed differential pair," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 7, pp. 1740–1747, Jul. 2017.

[10] Lopez-Martin, M. P. Garde, R. G. Carvajal, and J. Ramirez-Angulo, "On the optimal current followers for wide-swing current-efficient amplifiers," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2018, pp. 1–5.

[11] F. Centurelli, P. Monsurro, G. Parisi, P. Tommasino, and A. Trifiletti, “A topology of fully differential class-AB symmetrical OTA with improved CMRR,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 11, pp. 1504–1508, Nov. 2018.
[12] E. Cabrera-Bernal, S. Pennisi, A. D. Grasso, A. Torralba, and R. G. Carvajal, “0.7-V three-stage class-AB CMOS operational transconductance amplifier,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 11, pp. 1807–1815, Nov. 2016.
[13] J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R. G. Carvajal,“Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency,” IEEE J. Solid-State Circuits, vol. 40, no. 5,pp. 1068–1077, May 2005.
[14] R. G. Carvajal et al., “The flipped voltage follower: A useful cell for low-voltage low-power circuit design,” IEEE Trans. Circuits Syst. I,Reg. Papers, vol. 52, no. 7, pp. 1276–1291, Jul. 2005.
[15] S. M. Anisheh, H. Abbasizadeh, H. Shamsi, C. Dadkhah, and K.-Y. Lee, “98-dB gain class-AB OTA with 100 pF load capacitor in 180-nm digital CMOS process,” IEEE Access, vol. 7, pp. 17772–17779, 2019.
[16] M. Akbari, M. Shokouhifar, O. Hashemipour, A. Jalali, and A. Hassanzadeh,“Systematic design of analog integrated circuits using ant colony algorithm based on noise optimization,” Anal. Integr. Circuits Signal Process., vol. 86, no. 2, pp. 327–339, Feb. 2016.
[17] Richelli, L. Colalongo, and Z. M. Kovaca-Vanja, “Increasing the immunity to electromagnetic interferences of CMOS OpAmps,” IEEE Trans. Rel., vol. 52, no. 3, pp. 349–353, Sep. 2003.
[18] Shashank S., Kushal K., Abhay Surya Shankar, Madan Kumar G., Dr. Pavithra G., Dr. Sindhu Sree M., Padmavathy M., Dr. T.C. Manjunath, “RFID based attendance system with SMS Alert”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 774 – 782, Jul. - Sept. 2023.
[19] Abhishek, Sujith M.S., Jeevan D., P. Kamalesh, Dr. Sindhu Sree M., Dr. Pavithra G., Dr. T.C. Manjunath, “Design & Development of a Table Assisted Robotic Arm”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 818 – 822, Jul. - Sept. 2023.
[20] Apeksha U., Chithrashree G.S., Divya N.M., Shalmali S. Mankikar, Dr. Sindhu Sree M., Dr. Pavithra G., Dr. T.C. Manjunath, “Wireless LoRa Communication Between Two Arduino Uno for Military Application in Soldier Tracking”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN : 1001- 4055, Vol. 44, No. 3, pp. 768 – 773, Jul. - Sept. 2023.
[21] Akarsh Kesharwani, Ayush P. Chaudhary, Bhanu Pratap Singh, Ved Kumar, Padmavathi M., Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, “A Study on Hand Motion Controlled Robotic Arm”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 812 – 817, Jul. - Sept. 2023.
[22] Leena Jeyakumar, Prerana Aithal, Vismitha R., Pradhan Aithal, Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, “Development of Smart Bridge – Automatic Height Increase When Floodings Take Place”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, HIndex 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 763 – 767, Jul. - Sept. 2023.
[23] Sushanthi Raj, Manohar R., Bhuvan G.S., Deepthi. S.R., Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, “Design and Development of Obstruction Detection and Removal Bot”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 807 – 811, Jul. - Sept. 2023.
[24] Anagha, Jhanavi M., Khushi M.S., Nithin Kumar S., Dr. Sindhu Sree M., Dr. Pavithra G., Dr. T.C. Manjunath, “Paralysed Patient Healthcare Monitoring Device”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 758 – 762, Jul. - Sept. 2023.
[25] Ashmeet Singh, Harsshit Goenka, Prakhar Sahu, Venkatesh L., Pamavathi M., Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, “Development of an Automatic Fire Extinguisher”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 802 – 806, Jul. - Sept. 2023.
[26] Vaishnavi Patil, Dr. Pavithra G., Dr. T.C. Manjunath, “Design, Development of a Diversified Implementation of a Supervisory Control And Data Acquisition based VLSI System (SCADA) framework Utilizing Microcontroller based Programmable Logic Controllers”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN : 1001-4055, Vol. 44, No. 3, pp. 879 – 890, Jul. - Sept. 2023.
[27] Kavya P., Sanjana S., Harika, Teju R., Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, “Design & Development of Drones Using Radio Frequency Controllers”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 707 – 710, Jul. - Sept. 2023.
[28] S.G. Swathi, Aliya Bhandari, Srushti M. B. Kavya A., Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, “Voice Control Robot – Design & Development for Various Domestic Applications”, Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 791 – 801, Jul. - Sept. 2023.
[29] Vaishnavi Patil, Dr. Pavithra G., Dr. T.C. Manjunath, “Design of Smart Wheelchair For Disabled (Handicapped) Persons Using Real Time Embedded Systems & Internet Of Things Approach”, Scopus Journal Q3, Schimago Ranking SJR 2022

0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 871 – 878, Jul. - Sept. 2023.
[30] Biswendu Biswas, Madan V.L., Rakesh B.S., Prathik Chandrapal, Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, "Development of remotely operated military purpose aerial vehicles", Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 638 – 641, Jul. - Sept. 2023.
[31] Akanksha Dash, Amrutha G., Krutika S. Ganpur, Sneha Chatter, Dr. Pavithra G., Dr. Sindhu Sree M., Dr. T.C. Manjunath, "Obstacle Avoiding Robotic Car Using Arduino with Bluetooth and Voice Control", Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 783 – 790, Jul. - Sept. 2023.
[32] Vaishnavi Patil, Dr. Pavithra G., Dr. T.C. Manjunath, "Simulation & design of a VLSI embedded system using Verilog Coding with Modelsim approach in FPGA scenarios for AI applications in automotive sectors", Scopus Journal Q3, Schimago Ranking SJR 2022 0.32, H-Index 24, Tuijin Jishu/Journal of Propulsion Technology, ISSN: 1001-4055, Vol. 44, No. 3, pp. 862 – 870, Jul. - Sept. 2023.