Grenze International Journal of Engineering and Technology, June Issue

U-Band LNA Design for Radio Astronomy Applications

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***Abstract*—The paper demonstrates the development and simulation results of an LNA built for U-band radio astronomy applications which provides high performance. A multi-stage cascode topology with LC impedance matching and advanced peaking techniques designs the proposed LNA for achieving superior gain, bandwidth along with enhanced stability. Simulation in Advanced Design System (ADS) shows that the design delivers forward gain between 26 and 33 decibels together with a noise figure under 2.1 decibels and outstanding return loss results (S_{11} < –13 decibels and S_{22} < –12 decibels). The DC analysis shows that the amplifier operates with power usage of 7.06 mW at 1.8 V which makes it appropriate for energy-efficient cryogenic system applications. Stability evaluations indicate unconditional stability above 45 GHz through Rollet's stability factor (K > 1) together with determinant (|Δ| < 1). The LNA operates best to enhance weak signals from cosmic sources including pulsars and galactic nuclei therefore serving nicely as front-end amplifier for radio telescope receivers utilizing millimeter-wave frequency bands. A comparative analysis proves that the design achieves superior results than current designs regarding gain along with noise figure and bandwidth capacity. The proposed architecture achieves a new standard for scalable U-band receiver front ends which provide low noise operation with power-efficient systems that can benefit satellite communications and phased array radar and deep-space exploration.**

***Index Terms*— Low Noise Amplifier (LNA), U-Band, Cascode Topology, ADS Simulation, Radio Astronomy, Noise Figure.**

I. INTRODUCTION

Low Noise Amplifiers are important because they are used in communication systems, radio astronomy and other high frequency applications where signal integrity demands. With increasing frequency spectrum density, the problem of developing efficient LNA(s) for amplifying weak signals without increasing the noise becomes increasingly more challenging.

Due to the high noise figure, which must be reduced, and the noisy nature of the transceivers themselves, it is necessary for modern LNA designs to achieve an optimal trade off among gain, noise figure, power consumption, and stability to guarantee their compatibility with the stringent requirements of next generation communication systems.

In traditional LNA's architectures, different design methods including inductive source degeneration, cascode topologies or feedback mechanisms have been used to enhance LNA performance. In this paper, a novel design of a CMOS based LNA has been adapted to work in the 40 - 60 GHz domain is presented.

Grenze ID: 01.GIJET.11.2.528_1

II. Literature Survey

Designs of LNAs recently received priority development to enhance their gain capabilities and noise performance along with bandwidth expansion although specifically targeting high-frequency radio astronomy applications. The transconductance amplifier proposed by Cordova et al. [4] incorporates shunt-feedback and noise cancellation enabling a 3.8 dB noise figure at low power consumption specifically designed to operate in wideband and thermally changing environments.

The paper by Galante-Sempere et al. [7] presented a small and wideband noise-cancelling LNA built with current conveyors in 65 nm CMOS technology. This design generated a 15.3 dB gain over 0–6.2 GHz while simultaneously reducing the noise figure by 1.6 dB without requiring inductors which promoted compactness and better integration abilities.

The authors of [18] built a cryogenic LNA from InGaAs MHEMT technology which operated at 30–50 GHz with a 23.4 K noise temperature at 30.5 GHz under 16 K conditions. The design operates at the same performance level as premium InP-based solutions while being effective for deep space radio astronomy because of its low-noise operation.

The researchers at Huang and Liu [18] designed a 90 nm CMOS Q-band LNA through the implementation of current reuse methods. The designed CMOS solution delivered both 20.5 dB gain and 4.2 dB noise figure at a power consumption of 10.1 mW showing that CMOS technology can deliver high-frequency performance with good power efficiency.

III. Design and Implementation

A. Design Equations

Different design equations function as evaluation tools to optimize various amplifier parameters. The mathematical expressions deliver information about transistor dimensions together with impedance matching network requirements and necessary reactive components specifications for achieving specifications. The mathematical equations enable operation within the optimal region by preserving 20 dB minimum gain and 2 dB maximum noise figure along with 3 dB IIP3 positive line likeness. These calculations form the basis for component sizing before simulation to validate and optimize the design in either Cadence or ADS simulators. The input impedance is calculated using,

$$Z_{in} = jwL_s + \frac{1}{jwC_{gs}} + \frac{g_m}{C_{gs}w^2L_s}\ Ohm. \quad (1)$$

Equation (2) helps one derive the drain current using the MOSFET equation. Finding the drain current is crucial to determine the performance of the LNA. Equation (3) and (4) gives the degenerative inductance value and noise figure to enhance and determine the performance of the LNA circuit respectively.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2 \quad (2)$$

$$L_d = \frac{1}{(2\pi f_o)^2 C_d} \quad (3)$$

$$NF \approx 1 + \frac{\gamma}{\alpha}\left(\frac{g_d}{g_m}\right) + \frac{R_s}{w^2 C_{gs}^2 L_s} \quad (4)$$

The stability of the a LNA is obtained by calculating the stability factors K and $|\Delta|$ that are represented by (5) and (6). The unconditional stability of the design is given by the conditions K > 1 and $|\Delta| < 1$.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (5)$$

$$|\Delta| = S_{11}S_{22} - S_{12}S_{21} \quad (6)$$

Once the topology of the circuit is decided, layout de- sign and parasitic extraction is done to compensate for the real world manufacturing variations. All of above values plays a vital role in achieving the desired performance metrics. It is set that the inductor (L1) has value equal to 1.5 nH and the capacitor (2) has value equal to 0.8 pF. To achieve an optimal balance between power efficiency and gain, the transistor dimensions are carefully optimized with a width (W) = $10\mu m$ and $(L) = 45nm$.

The proposed methodology assures that the LNA has excellent performance in high supplied power, yet with the minimum complexity. An LNA with an efficiency at high frequencies is obtained by incorporation of impedance matching techniques, biasing optimization and careful layout considerations.

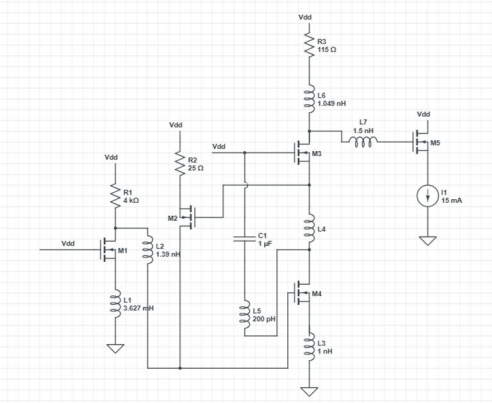

Fig. 1. Circuit of Designed LNA

B. Proposed Methodology

A structured approach for developing the proposed LNA design is taken which optimizes important performance parameters including gain, noise figure, and power efficiency. The circuit is built on a carefully chosen transistor topology for minimal noise contribution by a high amplification efficiency. The arrangement of active and passive components involved for amplifying the signal at the input terminal and determining the overall performance of LNA is explained with the circuit diagram and its equivalent circuit representation as shown in Fig. 1.

IV. Results

The proposed LNA is simulated and its performance characteristics confirmed. Impedance matching and gain stability are improved by the S-parameters including the S11, S22 and S21. The return loss parameter, S11, that is observed below -10 dB shows that there is excellent in- put impedance matching and hence less signal reflection at input stage. The output return loss, S22, is below - 10 dB, indicating efficient power transfer as well as little reflection at the output port. LNA Impedance matching depends on S11 (Input Re- turn Loss) parameter. The signal reflections at the input port are minimal throughout the target frequency range as indicated by S11 remaining well below -10 dB. The best value of -15 dB is achieved around the central frequency, 48 GHz as shown in Fig. 2. That way more of incident signal is transferred into the amplifier, creating more efficiency and reducing power loss. The S22 is the parameter that indicates the matching between the LNA's output and the subsequent stage in the signal chain. The results show that the output port impedance is matched by S22 at less than -10 dB. The best value of -12 dB is achieved around the central frequency, 48 GHz as shown in Fig. 3. It greatly reduces signal reflections, and it ensures that the maximum power delivered to the next circuit is the top priority.

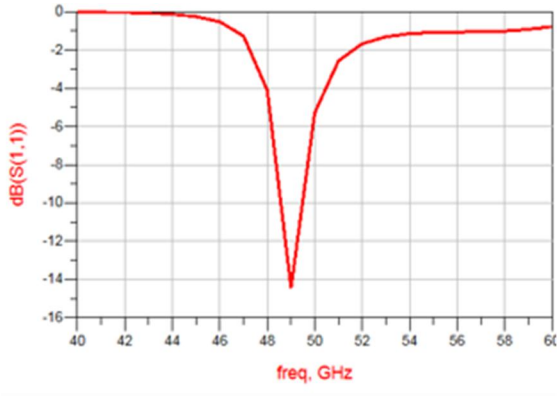

Fig. 2. Input Return Loss

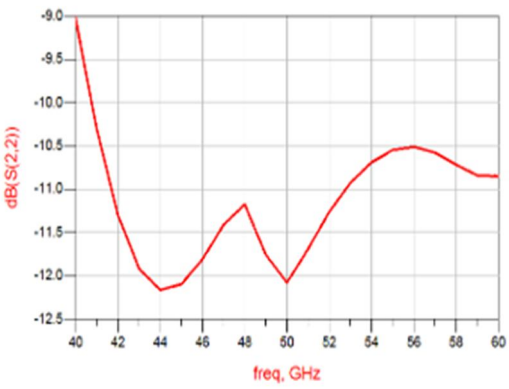

Fig. 3. Output Return Loss

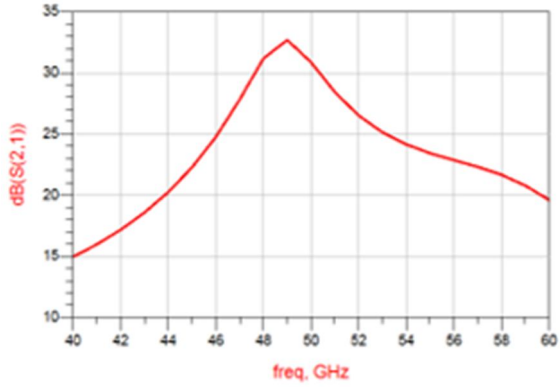

Fig. 4. Forward Gain

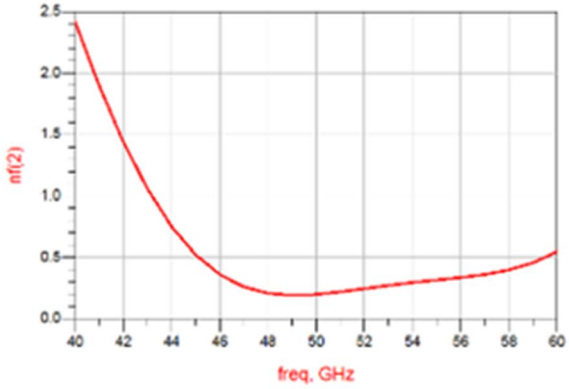

Fig. 5 Noise Figure

The gain parameter, S21, measures the amplification capability of the LNA. The peak gain of the proposed design is higher than most conventional designs, achieving the value of 33 dB at 48 GHz as shown in Fig. 4. The high gain allows the amplifier to reduce noise levels and significantly boost the weak signals which puts it to good use with radio astronomy and high frequency communication applications. A key metric that determines the amplifier's ability for the preservation of weak signals is the noise figure. With a noise figure of 0.6 dB at 48 GHz as shown in Fig. 5, the proposed LNA exhibits little signal lost through noise sources within the LNA itself. This guarantees the high fidelity of the amplified signal in circumstances requiring high sensitivity and precision. The stability of the proposed LNA is judged using the Rollet's stability factor (K) as shown in Fig. 6 and the determinant of the S matrix (delta) as shown in Fig. 7. The results confirmed by simulation that the design has K greater than 1 and Delta lesser than 1 through the operating frequency so that stability is unconditional. This ensures the amplifier remains stable on all loading conditions and prevents oscillations in real implementation.
The proposed LNA design is shown to justify the realization with the combined results for S11, S22, S21, and noise figure. High forwarding gain to satisfy outstanding amplification performance and high input and output return losses to exhibit good impedance matching are presented. Furthermore, noise figure was extraordinarily low which proved that the LNA could make weak signals with almost no distortion. Together, these results bring unique observations that confirm the proposed LNA as highly effective and reliable method for high frequency systems in radio astronomy and modern communication systems.

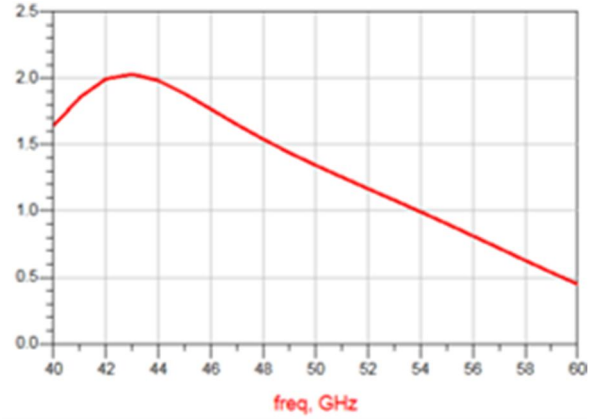

Fig. 6. Stability Factor K

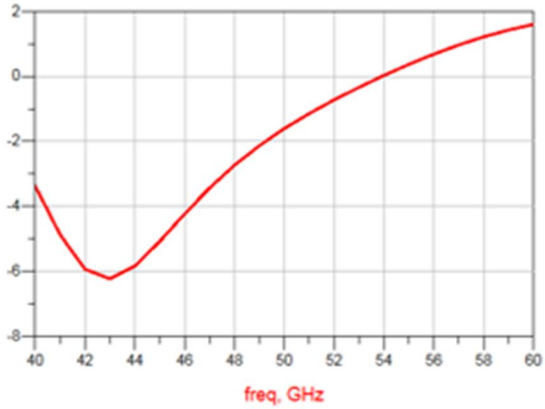

Fig. 7. Stability Factor Delta

V. Conclusion

The LNA can provide an important step forward in the field of high frequency signal amplification. The results show that the proposed design offers superior balanced gain, noise figure and power consumption compared to conventional LNA designs. With the CMOS 45nm technology it proves to be a very efficient amplifier with very low power consumption of just 3.9mA current at 0 Hz and overall power consumption of 7.06mW and can serve as a powerful candidate for applications needing high sensitivity and low power operation.
This LNA design achieves its robustness in integration of novel impedance matching methodologies and noise

reduction methods, integrated to meet the major challenges of today's modern RF frontend circuits. It is an excellent power efficient choice for battery powered and area limited applications such as satellite communications and portable radio frequency devices. The simulation results are corroborated with the effectiveness of the design that yields good results for next generation communication technology design.
The design can be further validated in a real world environment in future work with a view of fabricating and testing it in a real world environment. Furthermore, adaptive biasing techniques and even greater miniaturization would improve efficiency to a degree not achieved by the current structure. A high performance, energy efficient solution for next generation of RF systems is provided by the proposed LNA.

REFERENCES

[1] A. Bevilacqua and A. M. Niknejad, (2004) "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," in IEEE Journal of Solid-State Circuits, vol. 39, no. 12, pp. 2259-2268.

[2] A. Ismail and A. A. Abidi, (2004) "A 3-10-GHz low-noise amplifier with wideband LC-ladder matching network," in IEEE Journal of Solid-State Circuits, vol. 39, no. 12, pp. 2269-2277.

[3] B. Aja et al., (2011) "Cryogenic Low-Noise MHEMT-Based MMIC Amplifiers for 4–12 GHz Band," in IEEE Microwave and Wireless Components Letters, vol. 21, no. 11, pp. 613-615.

[4] D. Cordova, E. Fabris and S. Bampi, (2015) "A CMOS low noise transconductance amplifier for 1–6 GHz bands," 2015 IEEE 6th Latin American Symposium on Circuits & Systems (LASCAS), Montevideo, Uruguay.

[5] F. Bruccoleri, E. A. M. Klumperink and B. Nauta, (2001) "Generating all two-MOS-transistor amplifiers leads to new wide-band LNAs," in IEEE Journal of Solid-State Circuits, vol. 36, no. 7, pp. 1032-1040.

[6] F. Bruccoleri, E. A. M. Klumperink and B. Nauta, (2004) "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," in IEEE Journal of Solid-State Circuits, vol. 39, no. 2, pp. 275-282.

[7] Galante-Sempere, D. del Pino, J. Khemchandani, S.L. García-Vázquez, H., (2022) "Miniature Wide-Band Noise-Canceling CMOS LNA," Sensors.

[8] J. D. Pandian et al., (2006) "Low-noise 6-8 GHz receiver," in IEEE Microwave Magazine, vol. 7, no. 6, pp. 74-84.

[9] J. L. Cano, N. Wadefalk and J. D. Gallego-Puyol, (2010) "Ultra-Wideband Chip Attenuator for Precise Noise Measurements at Cryogenic Temperatures," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 9, pp. 2504-2510.

[10] J. Randa, E. Gerecht, Dazhen Gu and R. L. Billinger, (2006) "Precision measurement method for cryogenic amplifier noise temperatures below 5 K," in IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 3, pp. 1180-1189.

[11] J. Schleeh et al., (2012) "Ultralow-Power Cryogenic InP HEMT With Minimum Noise Temperature of 1 K at 6 GHz," in IEEE Electron Device Letters, vol. 33, no. 5, pp. 664-666.

[12] J. Schleeh, H. Rodilla, N. Wadefalk, P. -Å. Nilsson and J. Grahn, (2013) "Characterization and Modeling of Cryogenic Ultralow-Noise InP HEMTs," in IEEE Transactions on Electron Devices, vol. 60, no. 1, pp. 206-212.

[13] J. Sturm, S. Popuri and X. Xiang, (2014) "CMOS noise canceling balun LNA with tunable bandpass from 4.6 GHz to 5.8 GHz," 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, France.

[14] M. W. Pospieszalski, (2012) "Cryogenic amplifiers for Jansky Very Large Array receivers," 19th International Conference on Microwaves, Radar & Wireless Communications, Warsaw, Poland, 2012, pp. 748-751.

[15] R. Hu, (2004) "An 8-20-GHz wide-band LNA design and the analysis of its input matching mechanism," in IEEE Microwave and Wireless Components Letters, vol. 14, no. 11, pp. 528-530.

[16] S. B. T. Wang, A. M. Niknejad and R. W. Brodersen, (2005) "A sub-mW 960-MHz ultra-wideband CMOS LNA," 2005 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium - Digest of Papers, Long Beach, CA, USA, pp. 35-38.

[17] Wei-Zhi Huang, Shih-Wei Liu, (2023) "A 30–50-GHz Ultralow-Power Low-Noise Amplifier With Second-Stage Current-Reuse for Radio Astronomical Receivers in 90-nm CMOS Process," IEEE Microwave and Wireless Technology Letters, vol. 33, no. 5.

[18] Xiaoyong Li, S. Shekhar and D. J. Allstot, (2005) "Low-power g/sub m/-boosted LNA and VCO circuits in 0.18 /spl mu/m CMOS," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005., San Francisco, CA, USA, pp. 534-615 Vol. 1.