

Low Voltage High Transconductance Voltage Differencing Transconductance Amplifier and its Application in Biquad Order Filter

Kalpna Choudhary¹, Shweta Kumari² and Maneesha Gupta³

^{1,3}Netaji Subhas University of Technology/Electronics and Communication of Engineering, Delhi, India
Email: kalpna.choudhary.pg21@nsut.ac.in, maneeshapub@gmail.com

²Bharati Vidyapeeth Deemed University Netaji Subhas University of Technology/Electronics and Communication of Engineering, Delhi, India
Email: shwetagupta20009@gmail.com

Abstract—This paper proposed high performance VDTA (Voltage Differencing Transconductance Amplifier) where transconductance is enhanced by use of the NMOS cross coupling technique connected at load side. Moreover, bandwidth of proposed circuit has been improved using resistive compensation techniques. The transconductance of the proposed VDTA circuit is enhanced up to $3.56 \text{ m}\Omega^{-1}$ with 5.57MHz bandwidth at biasing current of $100\mu\text{A}$. Single input multi output biquad filter configuration using single proposed VDTA, three capacitors, and grounded resistor has been also designed and simulated to verify the proposed circuit. 180nm CMOS technology parameters with supply voltage $V_{DD}=-V_{SS}=0.4\text{V}$ has been used for simulation of proposed circuit.

Index Terms— VDTA, DTMOS, High transconductance, Positive feedback, and Biquad Filter.

I. INTRODUCTION

As technology evolved, the demand for electronics such as smartphones, portable computers, and digital gadgets increased in the past decade as it contributes to the ease of human life. However, this brings low-power devices into the picture to reduce consumption and design more reliable and power-efficient products, which motivates research in analog circuits to operate in low supply voltage levels. As move towards low power, a tradeoff arises as the analog circuits share supply voltage with digital circuits, affecting the device's performance. These are some factors that are motivating enough to carry out new research work to meet the requirements of modern electronics. Formerly in digital circuits, a reduction in supply voltage for transistors having a thin oxide area on the gate is implemented for low power consumption which also increases the density of the small area on the chip. Further decrement in channel length of transistor or threshold value below suitable level arises leakage current problems. In standard CMOS technology, analog circuits face some challenges as the leakage problem in the transistor is overcome by keeping suitably high threshold voltage levels and very low supply voltage hindered by digital circuits.

The DTMOS device is an efficient application for low voltage design to overcome the challenges of the conventional circuit in past work. It is implemented as a low-threshold device. In order to enable low power and voltage operation under 0.4V supply voltages, The DTMOS transistors has been consistently used in proposed

VDTA architecture. In this proposed circuit, four extra transistors (M18, M15 & M19, and M20) are employed as an active load for cross-coupling technique application for enhance transconductance of the device. Moreover, Resistive compensation technique is used to improve Bandwidth. This Manuscript holds for good Biquad Filter application. The offered circuit realizes three filters LP, HP, and BP.

II. DTMOS

When the DTMOS transistor is off, it exhibits a high threshold characteristic to reduce leakage, but when it is on, under a low voltage supply, it operates as a small threshold device for high current drivability. Due to respective characteristic, it is a favorable device for ultra-low-voltage analogue circuits of the present. Without requiring any further processing processes, a PMOS transistor's gate and substrate terminals can be linked, as shown in Fig. 1, and it can be made using conventional CMOS technology. In Fig. 1, the DTMOS symbol is displayed.

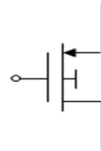


Fig.1 DTMOS Transistor symbol

Even yet, earlier dates may be traced for this setup [11-12] in-depth description of the device and explanations of its working are provided by Assederaghi et al. utilizing the relationship so the transistor threshold voltage can be dynamically altered by connecting the device's gate and body.

$$V_{TH} = V_{T0} + \gamma(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}) \quad (1)$$

Where, at zero body bias, the threshold voltage is V_{T0}

$$V_{T0} = |2\Phi_F| + V_{FB} + \sqrt{2qNA\epsilon_s/COX} \quad (2)$$

Here $\gamma = \sqrt{2qNA\epsilon_s/COX}$ (bulk threshold parameter)

V_{SB} = Source body voltage

Φ_F = Fermi Energy level

ϵ_s = Permittivity of silicon

q = Charge magnitude

NA = Acceptor ions concentration per unit volume

COX = Oxide (Gate) capacitance per unit area.

From DTMOS terminal connections, the body voltage of a DTMOS increases as the gate voltage rises. This causes V_T to fall in accordance with Eq (1), but V_{BS} must be below or equal to $2\Phi_F$ to maintain a small leakage current. When V_{BS} equals, the threshold voltage is at its lowest value. When V_{BS} equals $2\Phi_F$, the threshold voltage reaches this minimal value and given as

$$V_{min} = |2\Phi_F| + V_{FB} \quad (3)$$

This decrease in DTMOS V_t causes an increase in carrier mobility, which enhances the device's high output current and transconductance [15]. Transconductance for DTMOS may be determined to be equal to $(g_m + g_{mb})$, with g_m denoting gate transconductance and g_{mb} denoting body transconductances for conventional MOSFETs, respectively [15, 16]. Increased transconductance also results in a proportionate improvement in DTMOS's bandwidth. To maintain a minimal leakage current, the increase in V_{BS} must be constrained by the value of $|2\Phi_F|$, as was mentioned before. Additionally, triple good technology for CMOS devices based on DTMOS must be employed [17].

III. VDTA

The CDTA, whose input are currents, can be substituted with a voltage differencing transconductance amplifier (VDTA), having inputs as voltage [12], [13]. The analog signal processing circuits that are created as a result of

these voltage inputs offer new ideas to the established circuit solutions [12]. In Fig. 3, the circuit symbol is presented, and relations are displayed in a matrix according to its definition. In eq. (4).

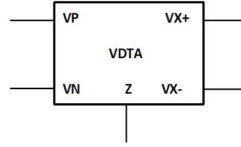


Fig.2 Circuit symbol of VDTA

The transconductance of g_{m1} is multiplied by the voltage difference between the input terminals to create the I_Z current, it creates the voltage there by flowing through the impedance at the Z terminal. The output I_X currents are then created by multiplying this voltage based on $+V_e$ and $-V_e$ g_{m2} transconductances. Two OTA circuits can be linked together in a cascaded method to produce a VDTA element.

$$\begin{pmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{pmatrix} = \begin{pmatrix} g_{m1} & g_{m2} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{pmatrix} \begin{pmatrix} V_P \\ V_N \\ V_Z \end{pmatrix} \quad (4)$$

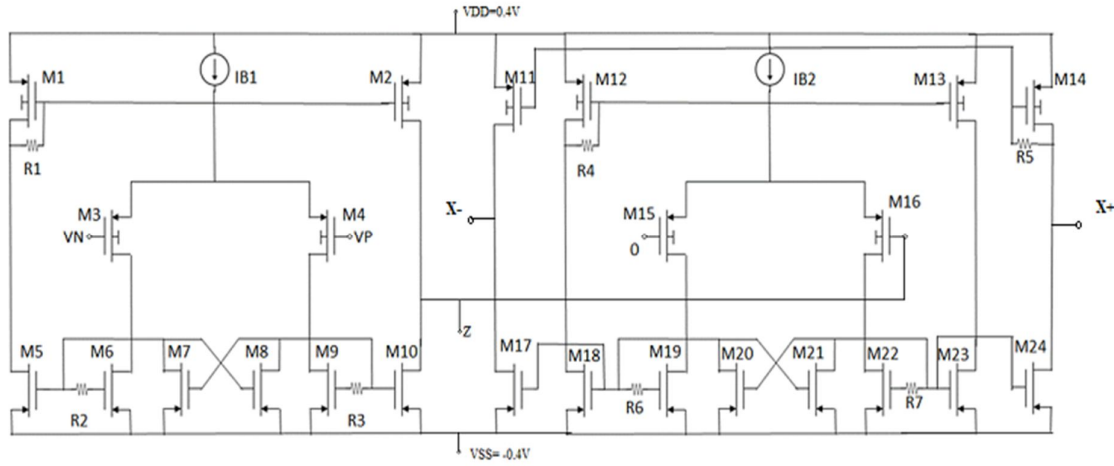


Fig. 3 The proposed VDTA circuit by using DTMOS

Fig. 3 depicts the proposed DTMOS-based low-voltage, low-power VDTA circuit. The VDTA design with two OTA, The first part of the OTA is made up of DTMOS transistors (M1, M2, M3, and M4) and correspondingly in the section-2 DTMOS transistors from M11-M16. These DTMOS transistors operate at the extremely low supply voltage (+ 0.4 V & -0.4V).

Fig. 3 depicts the design with a positive feedback loop that was employed to enhance the transconductance performance of the suggested VDTA. To produce the negative resistance, cross-coupled active load NMOS transistors are used. The NMOS M7 and M8 in the first section of OTA and M20 and M21 in the second section introduce local positive feedback loops. Furthermore, the resistive compensation technique is utilized in the suggested VDTA to increase the bandwidth of the transconductance stage.

While NMOS transistors in an n-well process share a common well and cannot construct NMOS DTMOS transistors by connecting their body terminals to their gates, in an n-well conventional CMOS process, PMOS transistors can be coupled as DTMOS transistors. Triple-well techniques utilizing deep n-wells are required to manufacture expensive NMOS transistors with their own wells. This limitation reduces the proposed circuit's overall performance because the NMOS transistors, which consume the majority of the voltage headroom, are the circuit's primary power source. Because of this, employing this circuit is not feasible for strong inversion operations or high-frequency applications. In this circuit, drain current (I_D) of MOS transistor is given by, and the transistors are therefore biased in weak inversion [3].

$$ID = IS \left(\frac{W}{L} \right) \exp \left(\frac{V_{GS} - V_{TH}}{L} \right) [1 - \exp \left(- \frac{qV_{DS}}{kT} \right)] \quad (5)$$

If $V_{DS} \gg 3kT/q$, the transistor will attain weak inversion saturation. [18].The following describes the transconductance gm :

$$gm = - \frac{qID}{nkT} \quad (6)$$

Where the Eq. (5) and (6)'s parameters have their normal meanings.

IV. SIMULATION RESULTS

The proposed VDTA with DTMOS has been simulated by the using 180nmCMOS technology parameters. Transistor dimensions are given in Table I. The supply voltage used for the proposed circuit is as $V_{DD} = -V_{SS} = 0.4$ V and bias currents of VDTA are chosen as $I_{B1} = I_{B2} = 100\mu A$. According to simulation results, this decision produces Transconductance values for VDTA as $g_{m1} = g_{m2} = 3.56mA/V$ in Fig.4 and in Fig.5 shows frequency response of transconductance stage of the proposed circuit at the different bias currents (I_B). The output stage of the proposed VDTA in Fig.6 shows DC Transfer Characteristic of I_{X+} and I_{X-} against V_z .

From Table-II we can see that our Transconductance improves by using describe techniques and bandwidth is also improved as compare to VDTA with DTMOS in past literature.

TABLE I. DIMENSIONS OF TRANSISTOR

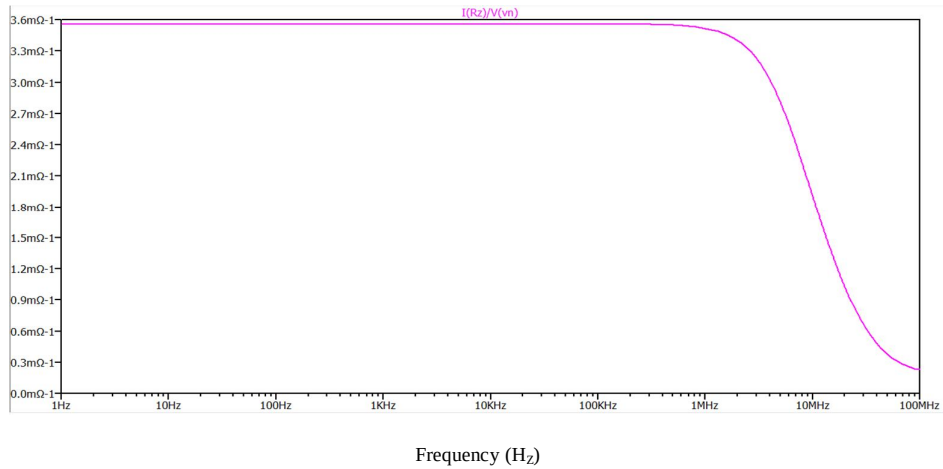
Transistors	W(μm)	L(μm)
M1, M2, M3, M5, M21, M23	2 μA	200 μA
M4, M6, M7, M9	2 μA	300 μA
M15, M18, M19, M20	5 μA	250 μA
M10, M13, M14, M17, M22, M24	5 μA	100 μA
M8, M11, M12, M16	5 μA	50 μA

TABLE II. COMPARISON TABLE

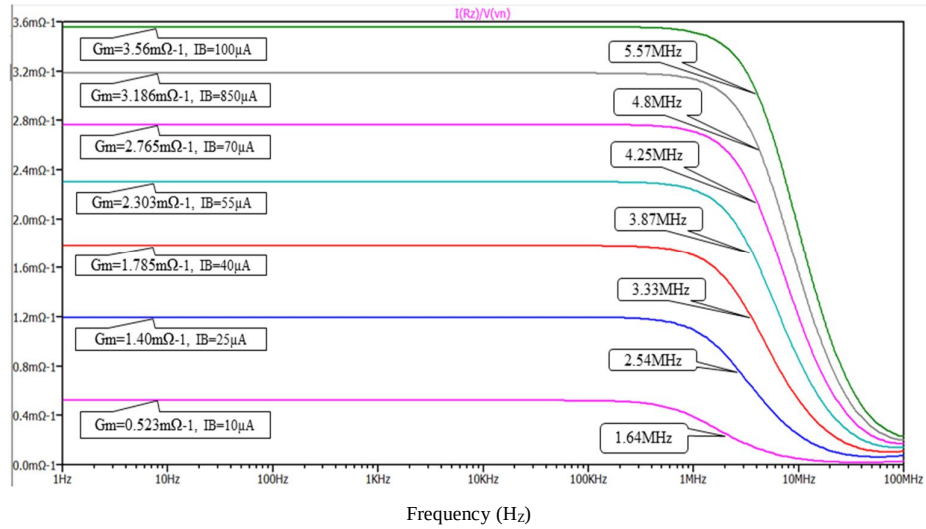
	VDTA with DTMOS	VDTA with DTMOS with Positive Feedback of NMOS	VDTA with DTMO Positive Feedback of NMOS & Resistive Compensation Technique
Technology (TSMC)	180nm	180nm	180nm
Supply Voltage (V_{DD}/V_{SS})	+ - 0.2V	+ - 0.2V	+ - 0.4V
Transconductance ($gm1=gm2$)	63nA/V	235.33 $\mu A/V$	$gm1=gm2=3.56mA/V$
Bandwidth of the VDTA	369Hz	432Hz	2.6MHz

V. VDTA BASED BIQUAD FILTER

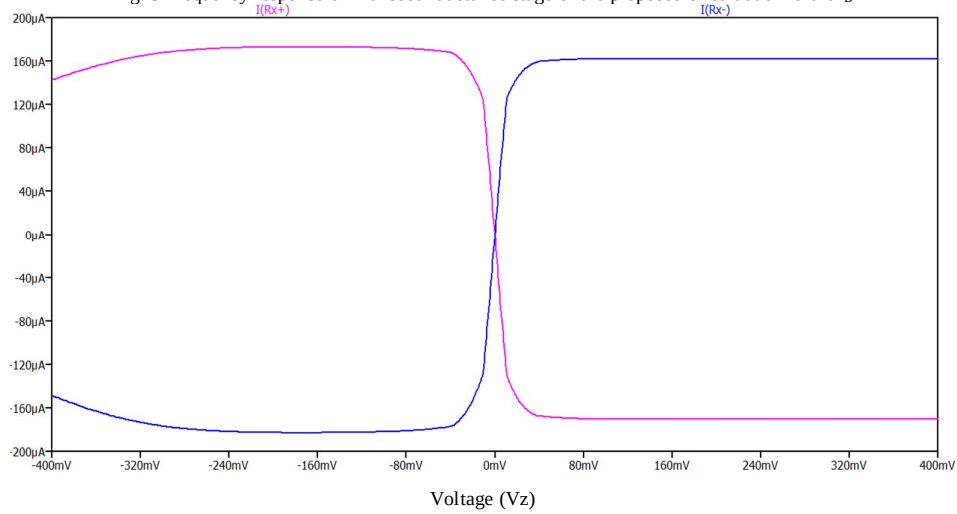
The VDTA can be easily used for realization for wide variety of mode filters. The advantage is that these circuits can be implemented without the need for external resistors because bias currents can vary the transconductance values. The implementation of a voltage-mode filter with single inputs and multi outputs is in Fig.7. This offered circuit implements LP, HP, and BP filters using three capacitors, one resistor, and a single VDTA. This suggested circuit implements LP, BP, and HP filters using just two capacitors and a single VDTA. Voltage-mode biquad transfer functions are produced through circuit analysis and are presented in (3). (6).



Frequency (Hz)
Fig. 4 Transconductance of the proposed circuit



Frequency (Hz)
Fig. 5 Frequency response of Transconductance stage of the proposed circuit at different I_B



Voltage (Vz)
Fig. 6 The DC transfer characteristic of the proposed circuit

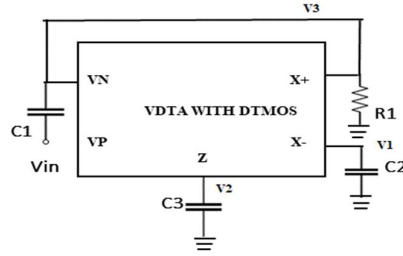


Fig.7 Application of the proposed circuit

$$\text{For LP } \left(\frac{V1}{V_{in}} \right) = \left(\frac{gm1gm2}{\Delta} \right) \quad (7)$$

$$\text{For BP } \left(\frac{V2}{V_{in}} \right) = \left(\frac{\left(\frac{gm1}{C3} \right) s}{\Delta} \right) \quad (8)$$

$$\text{For HP } \left(\frac{V3}{V_{in}} \right) = \left(\frac{s^2}{\Delta} \right) \quad (9)$$

Where

$$\Delta = (s^2 + \frac{s}{R1C1} + \frac{gm1gm2}{C1C3}) \quad (10)$$

When considering the VDTA transconductance $gm1 = gm2 = 3.73\text{mA/V}$, the provided circuit in Fig. 7 is simulated with the following passive values: $C1 = C3 = 1\text{F}$, $C2 = 1.5\text{F}$, and $R3 = 300$. The voltage mode gain frequency response simulation results for the LP, HP, and BP filters are shown in Fig. 8.

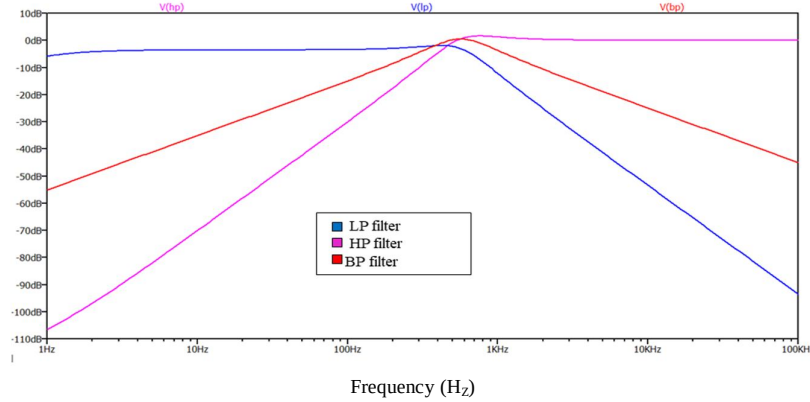


Fig. 8 Gain Frequency response of Voltage mode LP, HP, and BP signals

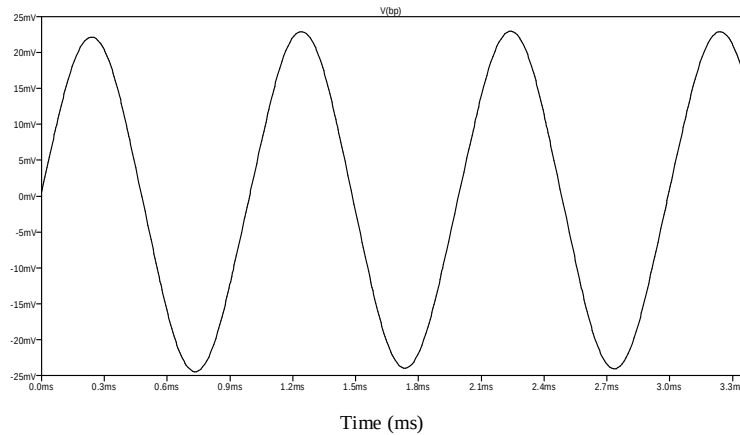


Fig. 9 Transient Response of Band pass filter at frequency 1KHZ

VI. CONCLUSIONS

This paper discusses high-performance tunable VDTA based on a strategy by use of resistive compensation and enhancing transconductance by positive feedback. It operates at a low supply voltage, improves transconductance, and employs low power as compared to other VDTA circuits in literature. The resistive compensation technique is implemented to increase the bandwidth of the circuit proposed and cross coupling techniques are implemented to increase the transconductance of the circuit proposed up to $3.56 \text{ m}\Omega^{-1}$ with bandwidth upto 5.57 MHz. The suggested VDTA circuit may therefore be beneficial for applications with mere focus on low-voltage, low-power, and high-performance analogue signal processing.

REFERENCES

- [1] Georgia Tsirimokou; Costas Psychalinos; Ahmed Elwakil "Design of CMOS Analog Integrated Fractional-Order Circuits" Springer
- [2] Yesil, A., Kacar, F. and Kuntman, H. "New Simple CMOS Realization of Voltage Differencing Transconductance Amplifier and Its RF Filter Application". Radioengineering, 2011,20, 632-637
- [3] Uygur, A. and Kuntman, H., "DTMOS-based 0.4 V ultra-low-voltage low-power VDTA design and its application to EEG data processing", 2013, Radioengineering, 22(2):458-466.
- [4] Neeta Pandey, Praveen Kumar, Sajal K. Paul (2015). "Voltage differencing transconductance amplifier based resistorless and electronically tunable wave active filter Analog Integrated Circuit Signal", 2015, Kluwer Academic Publishers United States, vol. 84, pp 107–117
- [5] Worapong Tangsrirat, Sumalee Unhavanich, "Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor", 2014, Indian Journal of Pure & Applied Physics Vol. 52, June 2014, pp. 423-428.
- [6] Jetsdaporn Satansup, Worapong Tangsrirat, "Compact VDTA based current mode electronically tunable universal filter using grounded capacitor", Microelectronics Journal 2014, vol.45, issue 6, pages 613-618.
- [7] Rajeshwari Pandey, Neeta Pandey, and Navin Singhal, "Single VDTA Based Dual Mode Single Input Multioutput Biquad Filter", Hindawi Publishing Corporation Journal of Engineering, vol.2016, ISSN2314-4904 (Print), 2314-4912 (Online).
- [8] Chandra Shankar, Sajai Vir Singh, "Single VDTA Based Multifunction Transadmittancemode Biquad Filter", International,2016, 7(6):2180-2188
- [9] Maneesha Gupta, Shweta Kumari, "New CMOS realization of high performance Voltage Differencing Inverting Buffered Amplifier and its filter application", 2017, pp 167–178
- [10] Maneesha Gupta, Shweta Kumari, "Design and Analysis of Tunable Voltage Differencing Inverting Buffered Amplifier (VDIBA) with Enhanced Performance and Its Application in Filters", Wireless Personal Communications, volume 100, pages877–894 (2018).
- [11] Parke, S. A., Bokor, J., KO, P. K., HU, C. Bipolar-FET hybrid-mode operation of quarter-micrometre SOI MOSFET's. IEEE Electronic Device Letters, 1993, vol. 14, p. 236-238.
- [12] Verdonckt-Vanderbroek, S., Wong, S., Woo, J., KO, P. High gain lateral bipolar action in a MOSFET structure. IEEE Trans. on Electron Devices, 1991, vol. 38, no. 11, p. 2487-2496.
- [13] Biolek, D. CDTA – Building block for current-mode analog signal processing. In Proceedings of the ECCTD03. Krakow (Poland), 2003, p. 397-400.
- [14] Biolek, D., Senani, R., Biolková, V., Kolka, Z. Active elements for analog signal processing: Classification, review, and new proposals. Radioengineering, 2008, vol. 17, no. 4, p. 15 – 32.
- [15] F. Assaderaghi, D. Sinitsky, S.A. Parke, J. Bokor, P.K. Ko, Dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage VLSI, IEEE Trans. Electron Devices 44 (3) (1997) 414–422.
- [16] V. Niranjana, A. Kumar, S.B. Jain, Low-voltage and high-speed flipped voltage follower using DTMOS transistor, Proceedings of the International Conference on Signal Propagation and Computer Technology (ICSPCT), 2014, pp. 145–150.
- [17] V. Niranjana, A. Kumar, S.B. Jain, Triple well subthreshold CMOS logic using body bias technique, Proceedings of the IEEE International Conference in Signal Processing, Computing and Control (ISPCC), 2013, pp. 1–6
- [18] Ferreira, H.C.L., Pimenta, C. T., Moreno, R. L. An ultralow-voltage ultra-low-power CMOS miller OTA with rail to rail input/output swing. IEEE Transactions on Circuits and Systems-II Express Briefs, 2007, vol. 54, no. 10, p. 843-847.