Grenze International Journal of Engineering and Technology, June Issue

Low-Power Neuromorphic Axon-Hillock Neuron with Memristor-based Synapses for High-Efficiency Spiking Neural Networks

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***Abstract*— Neuromorphic computing is a technology that imitates the brain's incredible efficiency in processing information, and it is seen as a potential source of solutions for computing tasks that require low power and high speed. We have developed a low power Axon-Hillock neuron design coupled with a triple memristor synapse architecture processed in 45 nm Cadence Virtuoso CMOS technology. The approach in the paper comprises two Axon-Hillock neurons linked via three memristors, which facilitates the fine adjustment of synaptic weights with a drastically lowered energy usage. The simulated results indicate that the design attains an average power of 11.74 nanowatts(nW), an energy per spike of 244.3 femtojoules(fJ), and a frequency of 47.6 kilohertz(kHz), thus being able to outperform the existing CMOS neuron realizations. Such an architecture manages to strike a compromise between very fast spiking and extremely low energy consumption, thereby becoming a perfect candidate for large-scale neuromorphic systems. This study is a step towards realizing energy-efficient artificial intelligence hardware of the future that leverages the potential of memristor-based neuron circuits.**

***Keywords*— Axon Hillock (A-H) Neuron, Memristor, Low-Power VLSI, 45 nm CMOS, Triple Memristor Synapse. Neuromorphic Engineering.**

I. INTRODUCTION

Neuromorphic computing has emerged as a trust approach for designing hardware systems that emulate the processing efficiency of the human brain. Unlike conventional computing architectures, which rely on sequential processing and separate remembrance units, neuromorphic systems exploit parallel computation and co-transaction of remembrance and processing, similar to biological nervous networks [1]. This enables make reductions in energy consumption and latency, which is interest result for true-term applications proposition as autonomous systems, robotics, and wounds computing. The increasing demand for location-might and high-say computing has motivated investigation into hardware implementations of artificial neurons and synapses that can achieve brain-like efficiency. In addition, biological neurons transaction intelligence by integrating inputs from more synapses and generating spikes when a threshold is reached.
The decision of whether or not an action potential will fire depends on the electrical input a neuron will receive within its Axon-Hillock region.

Grenze ID: 01.GIJET.12.2.257_21

Memristors, which are resistive devices with non-volatile remembrance characteristics, can emulate synaptic bad by modulating their component according to applied potential and adjust of spikes [8]. The uniting of Axon-Hillock neurons and memristor-based synapses allows the produce of energy-effective circuits that closely mimic biological nervous networks, while supporting tall-state risk transmission. Several studies have investigated complementary metal-oxide-semiconductor neuron circuits for spiking nervous networks. Vuppunuthala et al. [10] implemented a common neuron with a single synapse in 65 nano meter (nm) CMOS technology, achieving an energy according grain of 3.6 picojoules (pJ) at a spiking frequency of 31(Hz), with moderate might consumption. [11] designed a soft-reset neuron with capacitive synapses in 180 nanometer CMOS technology, reporting 2. 4 picojoules according grain but higher might use due to larger switch sizes. Barton et al. In addition, [12] presented a word-authority neuron with capacitive digital-to-analog converter synapses in 65 nanometer CMOS.

The proposed produce connects two Axon-Hillock neurons via three memristors, enabling incapable control of synaptic weights and reducing both static and dynamic might consumption. Simulation results demonstrate an average power of 11.74 nanowatts (nW), inherent according grain of 244. 3 femtojoules (fJ), and an operating frequency of 47.6 kilohertz (kHz). This demonstrates a significant improvement position prior CMOS implementation, providing a highly inherent-incapable and elevated-speed neuron orbit suitable for large-scale neuromorphic applications. The organization of this paper is as follows: Section II introduces the neuromorphic brain-inspired neuron model and describes the analogy between biological synapses and memristor-based electronic circuits. In Section III, the architecture proposed, including Axon-Hillock neuron circuit, Verilog-A memristor model, and triple-memristor synaptic design, is discussed. Section IV presents the simulation results, waveform analysis, performance tables, and a comparison against prior works.

Additionally, occurrence advances in memristor technology own enabled the development of compact and highly incapable synaptic circuits that can store and modulate synaptic weights with minimal inherent roof [9]. Unlike capacitive or resistive synapses, memristors provide non-volatile memory functionality, allowing the neuron orbit to retain learned data without continuous supply. In addition, this naturally interest advantageous for large-scale spiking nervous networks, where millions of synapses are required, and internal results is critical. Furthermore, the act of memristor-based synapses with Axon-Hillock neurons facilitates prominent-frequency spiking and place quality signal transmission, making the system suitable for true-time applications such as sensory data processing and neuromorphic pattern recognition. It is significant to note that, by integrating these devices in a 45 nanometer (nm) complementary metal-positive-semiconductor (CMOS) transaction, the proposed architecture achieves a clock between internal results, and scalability, which is essential for action deployment of neuromorphic hardware.

II. NEUROMORPHIC BRAIN-INSPIRED NEURON

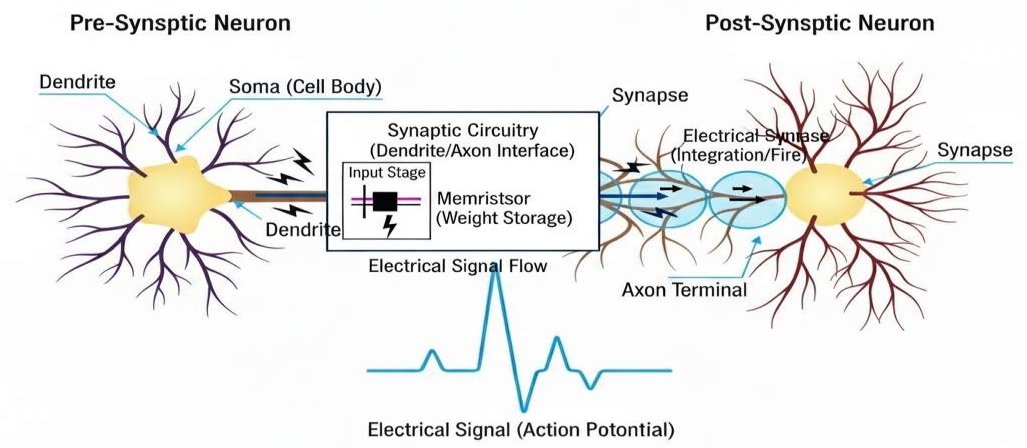

Figure 1. Neuromorphic brain-inspired neuron network illustrating the analogy between biological synapses and memristor-based electronic synaptic circuits

Neuromorphic computing attempts to replicate the operational principles of the human brain to achieve incapable parallel computation [1]. Biological neurons communicate through electrical spikes and chemical synapses, where the strength of synaptic connections determines how signals multiply across neural networks.

The Axon-Hillock quarters of the neuron functions as a decision-making unit, integrating incoming signals from multiple synapses and generating spikes after a threshold is reached [4]. This mechanism can be effectively modeled in hardware using Axon-Hillock neurons and memristor-based synapses, emulate two risk processing and adaptive synaptic behavior [3], [7]. Memristors, or resistive remembrance devices, are capacity of modulating their conductance harmony to applied potential and grain timing, providing a compact and energy-incapable alternative to conventional CMOS synapses [8]. Additionally, the triple-memristor configuration allows indistinct manage of synaptic weights, mimicking the plasticity of biological synapses while enabling beyond-place might result and high spiking frequency.

This approach ensures that the neuron circuit can calling efficiently equal in large-scale spiking neural networks, where millions of synapses are required. The proposed structure, shown in Fig. 1, illustrates the relation between biological synapses and memristor-based electronic synapses in a neuromorphic network. In this type, two Axon-Hillock neurons are interconnected via three memristors, enabling the network to act and transmit spikes efficiently while minimizing energy per grain [13], [14].

III. Proposed Methodology

The proposed low-power neuromorphic system combines Axon-Hillock neurons with a triple-memristor synapse architecture, implemented in 45 nanometer (nm) complementary metal-oxide-semiconductor (CMOS) technology. The methodology focuses on achieving ultra-low power consumption, minimal energy per spike, and high spiking frequency. The system consists of two Axon-Hillock neurons connected through three memristors, which act as programmable synaptic weights, closely mimicking the behavior of biological neural networks.

A. Axon-Hillock Neuron Circuit

The Axon-Hillock neuron circuit forms the core of the proposed design, responsible for integrating incoming synaptic currents and generating output spikes when the membrane potential exceeds a threshold [13]. Figure 2 shows the schematic of the Axon-Hillock neuron circuit.

The circuit uses subthreshold current mode operation to proportion might dissipation, allowing the neuron to operate with a 11.74 nanowatts (nW) power consumption. The design supports sky high-frequency spiking at 47.6 kilohertz (kHz) while maintaining stable waveform characteristics, as validated in simulation. The grain vital mechanism ensures equivocal adjust and amplitude, essential for downstream signal processing and skill in the network.

B. Memristor Modeling using Verilog-A

The methodology proposed here uses a fully parameterized Verilog-A memristor module that supports multiple physical models and window functions for accurate synaptic behavior. It dynamically updates the internal state variable and resistive switching using physics-based equations. The model allows realistic learning with stable convergence and seamless integration with the neuron circuit in Cadence simulations. This behavior allows the memristor to store and procedure intelligence simultaneously, similar to way biological synapses doing in the brain.

In the example, Equation(1) the surface say variable (w) represents the position of the boundary location high-pressure and low-pressure regions inside the memristor. The low of transition of this say variable is described by the basic linear ion action equation.

$$\frac{dw}{dt} = \mu_v \frac{R_{on}}{D} I(p,n). \qquad (1)$$

where μ_v is the ion mobility, R_{on} and R_{off} are the minimum and maximum pressure values, D is the more thickness, and I(p,n)is the moving flowing from the more. As moving flows, the line position w changes, gradually shifting the pressure place R_{on} and $R_{off.}$ For example, this Verilog-A example includes parameters for more dimensions, initial say, and threshold potential, allowing the user to manage way fast and way much the memristance changes with applied potential.

Once implemented, the memristor exhibited smooth switching characteristics and stable pressure until existence temporary simulations, proving its suitability for neuromorphic circuit integration. The memristor measure created using this Verilog-A apartment serves as the fundamental building more in the proposed neuromorphic mode. It was tile connected place two Axon-Hillock neurons to form a triple-memristor cell, which enables learning and risk process in hardware [1], [8], [9].

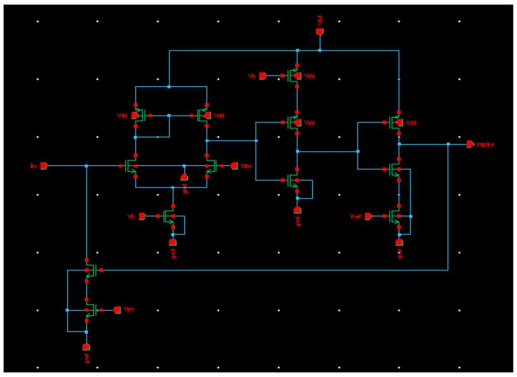

Figure 2. Axon-Hillock (A–H) neuron schematic

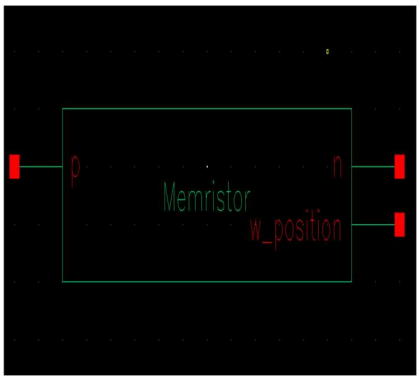

Figure 3. Memristor Symbol created using Verilog-A

This approach, based on Verilog-A, has several advantages:

- It allows for full customization of memristor behavior to match different material technologies.
- Real-time state evolution is provided during circuit simulations, thus allowing for accurate STDP learning analysis.
- This ensures that the memristor can be used as a symbolic component across any schematic in Virtuoso.
- It enables sweeps of parameters, Monte Carlo simulations, and the integration of multiple devices, including triple-memristor structures. Thus, creating the memristor symbol by using Verilog-A is an important initial step in the construction of the triple-memristor synapse and the realistic neuromorphic learning simulation to be done in later parts of the project.

Once the memristor symbol was validated, it was used to build the triple-memristor synapse schematic. Instances were connected with appropriate switching/control nodes to support read and write phases and to enable gated updates during STDP events. Care was taken while constructing the schematic to separate read and write paths in order to prevent inadvertent changes in the weights during normal neuron operation.

Some practical modelling notes: for transient analysis, use a conservative maximum time step to capture fast write dynamics reliably; run parameter sweeps to find stable programming pulses; and perform Monte-Carlo runs to provide a study of sensitivity to device parameter variation.

C. Triple-Memristor Synapse Architecture

The architecture distributes the synaptic pack across three memristors, which reduces energy according spike and ensures wavering spiking behavior at high frequencies. Figure 4 shows the Memristor cell integrated with the Axon-Hillock neuron schematic used in the proposed design. Triple-memristor synapses mitigate the effect of non-idealities that normally degrade the performance of a single memristor. Because of the sharing of synaptic weight among them, failure or variation in one memristor has a minimal effect on the general accuracy of learning. This redundancy enhances reliability, improves resistance to variability, and ensures more consistent long-term memory retention in neuromorphic hardware.

This create also supports state mechanisms, allowing the network to adapt to varying input patterns, similar to biological learning. By combining the Axon-Hillock neuron with the thrice-memristor cell, the proposed system achieves soaring energy efficiency, minimal might consumption, and precise spiking outcome, where it highly suitable for big-measure and real-time neuromorphic applications.

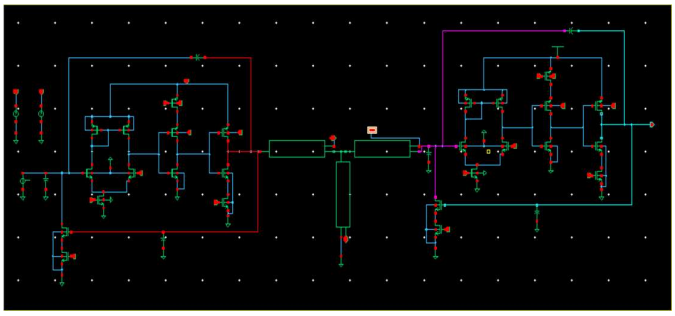

Figure 4. Triple memristor synapse with neuron schematic

IV. RESULTS AND DISCUSSION

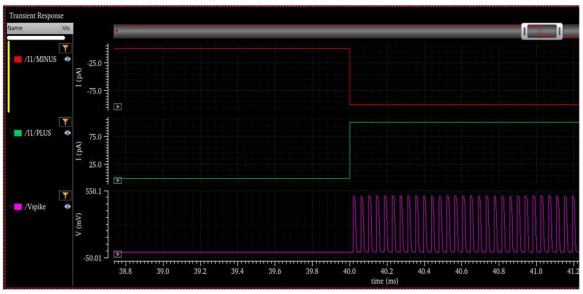

Figure 5. Axon Hillock neuron waveform

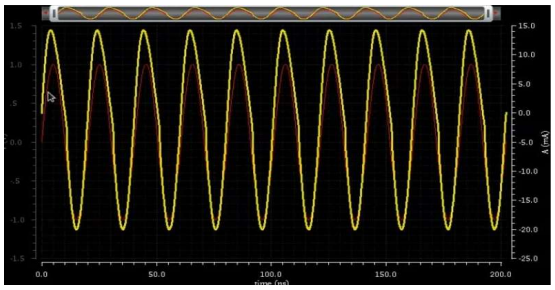

Figure 6. Memristor Waveform

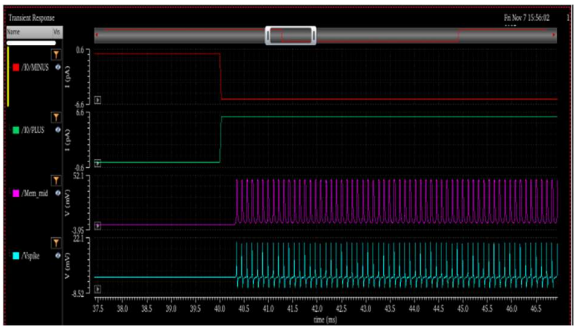

Figure 7(a) Triple-Memristor Synapse Waveform

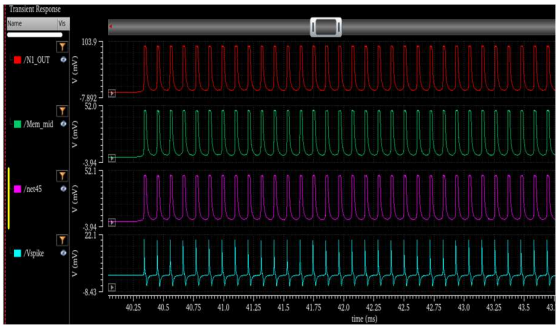

Figure 7(b) Triple-Memristor Synapse Waveform

The proposed low-power neuromorphic system was simulated in 45 nanometer (nm) complementary metal-oxide-semiconductor (CMOS) technology using Cadence Virtuoso. Fig. 5 show the output waveforms of the two Axon-Hillock neurons under different input conditions. The neurons generate clean and regular spikes at an operating frequency of 47.6 kilohertz (kHz), while the average power consumption remains 11.74 nanowatts (nW). Fig. 6 presents the memristor conductance variation over time, demonstrating accurate synaptic weight modulation in response to pre- and post-synaptic spikes. Fig. 7(a) and 7(b) represents the Triple-Memristor Synapse Waveform.

The memristor exhibits non-volatile behavior, reducing static power dissipation and maintaining energy per spike at 244.3 femtojoules (fJ), which is significantly lower than previously reported complementary metal-oxide-semiconductor neuron circuits [3], [4], [5]. These results confirm the effectiveness of the proposed design in achieving high-frequency operation with ultra-low energy consumption.

V. CONCLUSION

This paper demonstrated a low-power Axon-Hillock neuron circuit combined with a triple memristor synapse architecture, which was created with 45-nanometer CMOS technology. The designed prototype consumed power as low as 11.74 nanowatts, achieved an energy efficiency of 244.3 femtojoules per spike, and operated at a frequency of 47.6 kilohertz, hence making a significant breakthrough in the performance of neuron circuits. The usage of memristor-based synapses led to the small size of the structure, rapid response, and very low energy dissipation, thus, the design is appropriate for neuromorphic computing systems. The findings demonstrate that the proposed neuron successfully compromises between biological fidelity and circuit efficiency. The present design can be reconfigured into large-scale neuromorphic arrays in the next upgrade to carry out intricate pattern recognition and learning operations.

The implementation of on-chip learning rules like Spike-Timing-Dependent Plasticity (STDP) will make the system adaptive and making it to learn strong and weak signal, further refinement through a more advanced layout simulation process and STDP learning will be done or held in future.

Fabricating three memristors per synapse can be challenging because minimal adjustment in the devices may affect the veracity of the stored weight. Also, using more memristors increases the area and wiring complexity, so future work will focus on making the design easier to build in hardware.

TABLE I: COMPARISON OF THE PROPOSED NEURON WITH RELATED WORKS

Reference	Technology	Neuron Type	Synapse Type	Power	Energy/Spike	Frequency	Remarks
[10] S. Vuppunuthala et al., 2023	65 nm CMOS	Silicon Neuron	Single Synapse	0.5 µW	3.6 pJ	30 Hz	Moderate power
[11] J. Kim et al., 2024	180 nm CMOS	Soft-reset Neuron	Capacitive Synapse	1.2 µW	2.4 pJ	20 Hz	High energy use
[12] T. Barton et al., 2024	65 nm CMOS	PLL-based Neuron	Capacitive DAC	0.8 µW	1.6 pJ	25 Hz	Time-domain approach
Proposed Work (2025)	**45 nm CMOS**	**A–H Neuron**	**Triple Memristor**	**11.74 nW**	**244.3 fJ**	**47.6 kHz**	**Highly energy-efficient**

ACKNOWLEDGMENT

The authors express their heartfelt gratitude to the Department of Electronics and Communication Engineering, Acharya institute of technology, for providing laboratory facilities and technical guidance. Special thanks to Dr. Munavar Sherieff for his valuable mentorship and constant support throughout this research.

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