Grenze International Journal of Engineering and Technology, Jan Issue

Energy Efficient Design of Full Adder using the XOR/XNOR Gates

K.Gayathri[1] and Dr.S Poongodi[2]
[1-2]CMREC/ECE, Hyderabad, India
Email: katikalagayathri@gmail.com, dr.poongodi@cmrec.ac.in

***Abstract*—Since the past decade, the semiconductor industry has seen an explosion in advanced interactive applications integrated with electrical gadgetry. The most frequently and extensively utilised circuits in (Integrated circuit) systems are fast arithmetic calculation cells, which include adders and multipliers. XOR-XNOR circuits are fundamental building elements in a wide variety of circuits. Because of their low yield capabilities and low power consumption, the latest new FA modules are more efficient in terms of Area and the power. This article proposes a low-power full adder utilising an efficient logical method, which lowers power consumption by constructing a full adder using the EXOR-EXNOR circuit. The full-swing EXOR–EXNOR or EXOR/EXNOR gates are used in these proposed circuits. Each of the new designs has its own preferences in terms of speed, energy consumption, delay product, driving capacity, and time. Tanner/Xilinx ISE simulation tools are used to test the execution of the new structures.**

***Index Terms*— Adder, energy efficient, EXOR, XNOR, VLSI design, Tanner.**

I. INTRODUCTION

We have witnessed the integrated chip density grow dramatically in recent years. Most designs are highly integrated and chip circuits are becoming more complicated and numerous problems including interconnection, coupling effects, distortions and heating effects in turn. We have additional associated problems other than these, such as set-up time, time breaches, skew, and many more. The primary reasons for these problems are the complexity of both the systems. Why do low-power equipment play an important part in technology today. Researchers have begun to explore advances on low-powered devices, which have already been made accessible, and the rise of portable devices such as laptops, smart phones and mobile devices continues to increase. Some factors explain how successful these low-power gadgets are in your design. It also decreases the energy consumption of a circuit as well as the reduction of the surface area. .

A. Traditional Full Adder

It's a typical complete adder, as seen in the diagram. With the assistance of 14 pull up transistors (PMOS) and 14 pull down transistors, it was implanted (NMOS).. Double-pass transistor logic, swing repaired pass transistor logic, complementary pass transistor logic, transmission gate logic, and other logics were utilised to construct the complete adder shown in figure 1.
Many sophisticated designs, such as ripple carry adder, carry-look ahead adder, carry save adder, carry skip adder, and multiplier, and have been developed from full adders.

Grenze ID: 01.GIJET.8.1.505

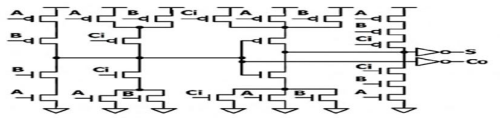

Figure 1: Conventional CMOS Full Adder

TABLE I: FULL ADDER TRUTH TABLE

A	*B*	*C*	*SUM*	*CARRY*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

B. System Description

Earlier XNOR gate designs include a 6T XNOR gate with pass transistor logic and lower power consumption. It is claimed that an 8T XNOR gate with a large output swing voltage and high driving capacity has been developed. Another 8-transistor XNOR gate with low power consumption has been discovered[11-12]. The 3T XNOR, which is based on pass transistors, is said to use less power and have limited driving capacity. A low-power XNOR gate design using FINFET technology has been described.

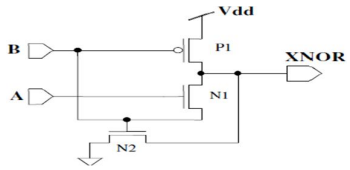

Figure 2: sample XNOR gate

As Width of N1 transistor has been increased threshold voltage of NI will become decreased

$$V_{TN} = V_{TO} + \gamma(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|})$$

VTN – threshold voltage when body bias is present VSB _ substrate to body
bias voltage
ϕF - surface potential
VTO – threshold voltage for zero substrate bias

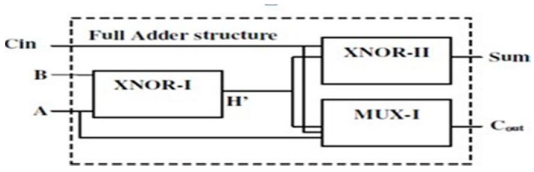

Figure 3: Structure of single bit full adder

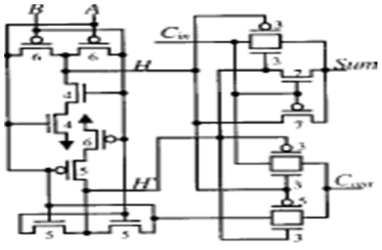

Figure 4: 16T full adder

The goal of this study was to investigate hybrid CMOS style design in order to provide low-energy operations for deep sub micrometre. This study used CMOS logic types to create an adder with the required performance. The designer may target a broad variety of applications with this adder. The suggested XOR-XNOR gate will concurrently produce full swing outputs. This adder is capable of driving and lowers buffer use between cascaded stages. .

C. Proposed method

Depicts the suggested XNOR gate design. It is made up of three transistors: one pMOS and two nMOS. All transistors have their drain linked to the Out terminal.

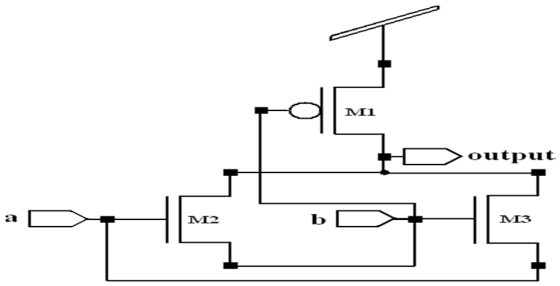

Figure 5: Proposed 3T XNOR gate

TABLE II. PERFORMANCE TABLE OF PROPOSED 3T XNOR GATE

A	b	Expected Output	Obtained Output
0	0	1	**1.00**
0	1	0	**0.00**
1	0	0	**0.15**
1	1	1	**1.00**

The suggested 8T complete adder has been built with the assistance of a 3T XNOR gate, as shown in Figure 4.2. The total output is created using a 3T XNOR gate in cascade, whereas the carry output is created with a 3T XNOR gate and a 2T multiplexer.

II. RESULTS

All schematic simulations were run using Tanner EDA tool version 2019 with a generic 250 nm technology and an input voltage range of 0 V to 2.5V in 0.1V increments. To provide a neutral testing environment, both circuits were tested on the identical input patterns, which covered all possible input stream combinations. Tanner eda 2019 was used to demonstrate that the suggested design consumes less power while providing greater performance.

Using inverted gates on the fundamental method of the construction comes out to be a significant drawback, according to this evaluation. The second disadvantage linked with the circuit is added with the mechanism with positive feedback used to payback the yield voltage range. This feedback mechanism enhances the postponement of the circuit, its output capacity and therefore its power use. In order to guarantee that these vulnerabilities are completely removed, sophisticated EXNOR gates are recommended at this point.

TABLE III: OUTPUT VALUES OF PROPOSED

Input			**output**	
CIN	**B**	**A**	**EXISTING**	**8T**
0	0	0	0.00	**0.00**
0	0	1	1.00	**1.00**
0	1	0	1.00	**1.00**
0	1	1	**0.21**	**0.00**
1	0	0	**0.55**	**0.98**
1	0	1	0.17	**0.46**
1	1	0	**0.28**	**0.21**
1	**1**	1	**0.51**	**1.00**

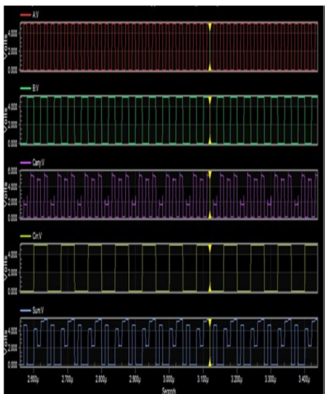

Figure 6: It shows the simulated output of proposed method

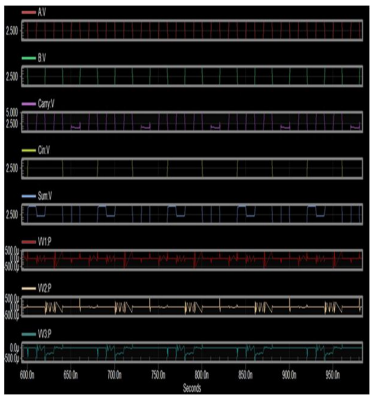

Figure 7: It shows the power consumption

III. CONCLUSIONS

The proposed 8T adder was developed and simulated using Tanner EDA tool version 2019. The suggested 8T 1-bit full adder outperforms the current 8T full adder in terms of performance. At different input voltages and frequencies, it was shown to have superior temperature sustainability and substantially reduced power and power-delay product. It improves threshold loss by 82 percent over the current 8T full adder. According to simulation findings, the suggested XNOR gate does not fulfil certain of the inputs when compared to a standard XNOR gate, but it has superior performance in terms of power consumption, latency, and area. The suggested XNOR and complete adder have a greater future scope in terms of performance and latency. These may be used in low-power applications, and the suggested XNOR gate can be used in parity checkers, comparator, compression, defect and flaw codes, phase detectors, and code converters. Digital signal processors and microprocessor designs utilise full adders.

REFERENCES

[1] Malini, P., Balaji, G.N., Boopathiraja, K., Gautami, A., Shanmugavadivu, P. and Pandian, S.C., 2019, March. Design of swing dependent XOR-XNOR gates based hybrid full adder. In *2019 5th International Conference on Advanced Computing & Communication Systems (ICACCS)* (pp. 1164-1170). IEEE.

[2] Neeraj Kumar Singh, Purnima Kumari Sharma, "A Novel 4T XOR based 1 Bit Full Adder Design," International Conference for Convergence of Technology – 2014.

[3] R.N.Nivethitha, S.Divya, "Performance analysis of low power full adder using 8transistor", International Conference on Engineering Trends and Science & Humanities (ICETSH-2015)

[4] JAYACHITHRA, P. and KUMAR, S., Design And Analysis Of Low Power High Performance Single Bit Full Adder.

[5] Bhavani Prasad Y, Harish Babu, N. Ramana Reddy K.V., Dhanabal R, "Comparative Performance Analysis of XOR-XNOR Function Based High-Speed CMOS Full Adder Circuits" international journal of engineering development and research | IJEDR, ISSN: 2321-9939. 18.

[6] Vahid Foroutan and Keivan Navi, "Low Power Dynamic CMOS Full-Adder Cell" (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 6 (3) , 2015, 3198- 3201.

[7] Krishna Chandra, Rajeev Kumar, Shashank Uniyal, Vishal Ramola, " A new design 6T Full Adder Circuit using Novel 2T XNOR Gates" IOSR Journal of VLSI and Signal Processing (IOSR- JVSP) Volume 5, Issue 3, Ver. I (May - Jun. 2015), PP 63-68 e-ISSN: 2319 – 4200, p-ISSN No. 2319 – 4197.

[8] Sugandha Chauhan, Tripti Sharma,"Full Adder Circuits using Static Cmos Logic Style: A Review" International Journal of Computer Applications (0975 – 8887) National Conference on Latest Initiatives& Innovations in Communication and Electronics (IICE 2016).

[9] S. Selvi*, S. Pradeep, " 6 Transistor Full Adder Circuit Using Pass Transistor Logic," Journal of Chemical and Pharmaceutical Sciences, ISSN: 0974-2115, February 2017.

[10] Anurag kothari, Achint chugh, "Less Power Consumption based low delay based 9-transistors based full adder," ijo science. volume III, issue v, June 2017.

[11] Hasan, M., Hussain, M.S., Hossain, M., Hasan, M., Zaman, H.U. and Islam, S., 2021. A high-speed and scalable XOR-XNOR-based hybrid full adder design. *Computers & Electrical Engineering*, *93*, p.107200.

[12] Kumar, S.S. and Rakesh, S., 2020. A Novel high-speed low power 9T full adder. *Materials Today: Proceedings*, *24*, pp.1882-1889.

[13] JYOTHI, K. and PUSHPALATHA, M., Implementation Of ALU sing Low Power Full Adder.
[14] Kuo, P.Y., Sheu, M.H., Tsai, C.M., Tsai, M.Y. and Lin, J.F., 2021. A Novel Cross-Latch Shift Register Scheme for Low Power Applications. *Applied Sciences*, *11*(1), p.129.
[15] Rostami, D., Eshghi, M. and Mehrabani, Y.S., 2020. Low-power and high-speed approximate 4: 2 compressors for image multiplication applications in CNFETs. *International Journal of Electronics*, pp.1-21.