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An Accurate Low-Power Power-on-Reset Circuit in 45-nm CMOS Technology

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***Abstract*— In this short paper, we introduce a new power-on-re-set circuit that uses very little power and works accurately. To achieve a precise trip voltage with minimal extra cost, we designed a low-pow-er system that uses a current reference and a current comparator. The reference current in this design comes mainly from the subthreshold current of several native NMOS transistors. By changing how many of these transistors are used, we can get a stable hysteresis window. When tested using a45nm CMOS process, the circuit uses just 418pW of power at0. 5V supply voltage. The measured trip voltage is0. 45V, and it changes by 227µV per degree Celsius with temperature. Since the circuit uses only10 transistors, its size is very small, just 67. 5µm².**

***Index Terms*— Power-on-reset, low-voltage, low- power, high accuracy, area efficient.**

I. INTRODUCTION

With the fast growth of Internet of Things (IoT) applications has made reducing energy use a key goal in designing integrated circuits. One of the best ways to cut power use is by using low voltage techniques, which are commonly used in low-power systems. In digital systems, it's important to set memory elements to a specific state when the power is first turned on. To make sure the system works properly at low voltage, an accurate low-voltage power-on reset (POR) circuit is needed. Also, the POR circuit stays active after the reset signal is turned off, so its static power use should be as low as possible to meet low-power needs. To prevent problems from short voltage drops, the POR circuit must have a brown-out detection (BOD) function. This function resets the system when the voltage falls below a set trip voltage. To avoid repeated resets from small voltage fluctuations, the BOD trip voltage is usually a little lower than the POR trip voltage. The difference between these two voltages is called hysteresis. this makes the circuit less stable under PVT changes. Many low-power POR circuits use delay elements to create the reset signal, which reduces power use compared to band-gap designs. But delay elements are very sensitive to PVT variations, making the trip voltage less reliable. Also, most of these POR circuits don't work properly at low voltages, which limits their use in low-voltage systems. In this paper, we introduce an accurate and low-power power-on-reset circuit. By using a low-power design based on current reference and current comparator, the circuit provides precise power-on reset with minimal power use. This paper builds on work from [14].

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We also present experimental results to confirm the effectiveness of the proposed circuit. Additionally, we show a variation of the circuit that can create POR circuits with different trip voltages, expanding its possible uses.

II. Literature Survey

The Power-On-Reset (POR) circuit is an essential block in digital and mixed-signal integrated systems. It ensures that all logic circuits start in a defined state when the power supply is turned on, thus guaranteeing reliable operation of the system. Several POR circuits have been proposed over the years, focusing on improving accuracy, reducing power consumption, and maintaining functionality over a wide range of process, voltage, and temperature (PVT) variations. In traditional designs, bandgap reference-based POR circuits were widely used because they provide a stable and accurate reference voltage that is nearly independent of temperature and supply variations. However, bandgap references typically consume higher power and occupy more area, which makes them less suitable for ultra-low-power applications and advanced CMOS technologies. To address the limitations of bandgap-based designs, researchers have developed comparator-based and current-comparison-based POR circuits. Comparator-based de-signs use voltage or current references to detect when the supply voltage crosses a predetermined threshold. These circuits offer faster response and lower static current but can suffer from offset errors and process dependency, especially in deep submicron technologies like 45 nm. Current-comparison-based PORs, on the other hand, use matched transistor pairs to compare currents derived from the supply voltage. They are known for their low quiescent current and compact size, but their accuracy is affected by transistor mismatch and temperature variation. Some designs use trimming or calibration techniques to correct these errors, though this increases circuit complexity. Recent research has introduced resistorless and subthreshold-operating POR circuits to achieve ultra-low power consumption. These designs operate with quiescent currents in the nanoampere range, making them suitable for IoT and battery-powered systems. However, working in the subthreshold region introduces challenges such as temperature sensitivity and slower response time. Another design approach involves the use of forced-stack transistor configurations, which effectively reduce leakage currents in 45-nm technology while maintaining detection reliability. Such architectures provide.

III. Proposed Methodology

In this, we look at the design of the 10-transistor POR circuit and its different version in detail. The design of the 10-transistor POR circuit is shown in figure. The reference current in the 10-transistor POR circuit comes from the sub-threshold current of the transistors NM2a and NM2b.Transistors NM3, NM4, PM2, and PM1 act as current mirrors to copy this reference current. The detailed operation of the 10-transistor POR circuit is shown in Fig. 3. As shown in Fig. 3, the 10-transistor POR circuit works as follows. When the power supply starts to ramp up, the current of the current reference and transistor NM1 rises gradually. Since NM2a, NM2b, NM3 and NM1 are in sub- threshold region. The gate of transistor NM1 is directly connected to the power supply voltage VDD, so the current through NM1 shows what the power supply voltage is. The voltage at node V2 is determined by the reference current and the current through NM1. When the reference current is stronger than the current through NM1, node V2 charges up to a high level through PM1. When the reference current is weaker, node V2 discharges to a low level through NM1. Transistors PM4 and NM6 act like an inverter and produce the reset signal RSTN. The detailed operation of the 10-transistor POR circuit is shown. The 10-transistor POR circuit works like this. When the power supply starts to rise, the reference current and the current through NM1 also increase gradually. Since NM2a, NM2b, NM3, and NM1 are in the sub-threshold region.

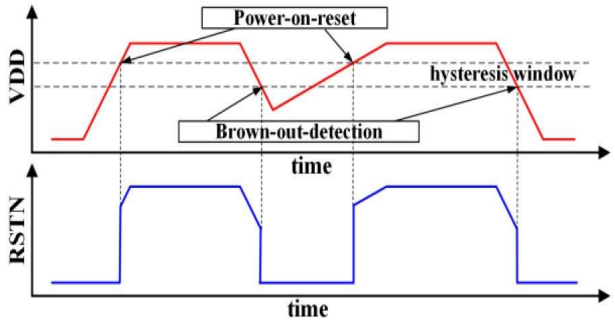

Fig. 1. Transient waveform of the proposed 10-transistor POR circuit

It can be seen that when the supply voltage is not very high, the reference current increases as the sup-ply voltage goes up. When the supply voltage gets higher (VDS is much greater than the threshold voltage VT), the reference current stays the same. Also, the current through NM1 increases quickly as the supply voltage goes up. Because the threshold voltage of NM2a and NM2b is much lower than that of NM1, Figure 3. The changing pattern of the 10-transistor POR circuit. The reference current is high-er than the current through NM1 when the supply voltage is low, and node V2 goes high. As the supply voltage increases, the current through NM1 goes up until it is higher than the reference current, then node V2 goes low and the reset signal RSTN becomes high. When the reset signal RSTN is high, the current through NM2a is cut off completely by transistor PM3, and the reference current goes down. When RSTN is no longer high, the current through NM1 is just a little more than the reference current so that node V2 stays low and RSTN remains high. When the power supply starts to decrease, the cur-rent through NM1 decreases slowly. When the current through NM1 drops below the reference current, node V2 goes high and the reset signal RSTN becomes low. Since the reference current is higher when RSTN is low (PM3 is on), the POR trip voltage (VPOR) is higher than the BOD trip voltage (VBOD), creat-ing a hysteresis window. The parameters labelled with a 1 are the parameters of NM1, the ones with a 2 are the pa-rameters of NM2a (NM2b), and the ones with a 3 are the parameters of NM3. Parameter N represents the number of active NMOS transistors. When RSTN is low, N equals 2, and the trip-voltage is the POR trip voltage. When RSTN is high, the current through NM2a is fully blocked by PM3, N equals 1, and the trip-voltage is the BOD trip voltage. Because the threshold voltage Vth changes with temperature and VT also changes with temperature, the temperature effects of the first two terms in equation (2) can be made to balance each other by adjusting the size of the transistors.

IV. Design Considerations

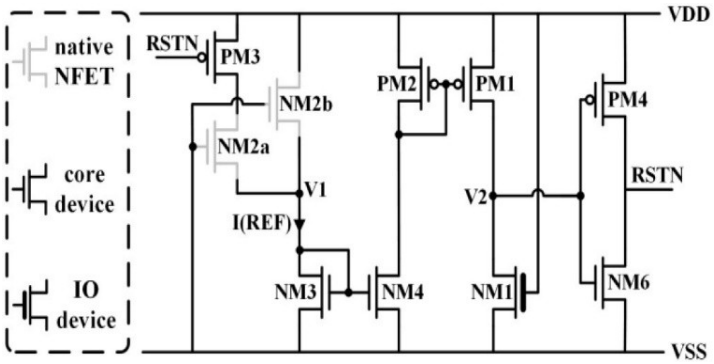

Fig 2

A. Software Considerations

For designing the proposed Power-On-Reset (POR) circuit in 45-nm CMOS technology, simulation tools like Ca-dence Virtuoso is used. These tools help in schematic design, transient analysis, and performance verification of the circuit parameters such as trip voltage, reset delay, and power consumption. Using BSIM4 transistor models, the circuit is tested under different process corners and temperature conditions to ensure stability and accuracy. Post-layout simulations are performed to validate the design. Additional tools like may be used for waveform analysis and data plotting. Overall, these software tools ensure the circuit meets low-power and high-accuracy requirements be-fore fabrication.

V. Result and Discussion

As the technology node scales down (from 90nm to 45nm), the power consumption decreases significantly. This is due to smaller transistors, lower supply voltages, and reduced parasitic capacitances. The 45nm tech-nology shows the lowest power consumption (418 pW). Such ultra-low power is highly desirable for low-power and battery-operated devices, IoT, and wearable electronics. The power consumption of 90nm is 4.2 µW which is Suitable for older systems, higher power budgets,65nm is 2.6 µW Improved power efficien-cy,55nm is 32 nW A huge drop in power (by almost 2 orders of magnitude) and 45nm is 418 pW Extremely low, shows excellent power optimization.

TABLE I: PERFORMANCE COMPARISON OF VARIOUS POR CIRCUITS

Technologies	Power
90nm	4.2 µW
70nm	3.6 µW
65nm	2.6 µW
55nm	32nW
45nm	418pW

The power values in the table clearly demonstrate the advantage of advanced CMOS nodes like 45nm in achieving ultra-low power operation in POR circuits. The 418 pW value at 45nm indicates a highly optimized design achieved likely through: Efficient current references, Low-leakage transistors. Compares the proposed POR circuit with other POR circuits. As shown in Table IV, the trip-voltage of the proposed POR circuit is 0. 45V, making it suitable for low-voltage applications. The circuit works properly across a wide temperature range from −40◦C to 125◦C, with a temperature coefficient of 227µV/◦C, which is similar to that of band-gap based POR circuits. The static power consumption of the proposed POR circuit is only 418pW, which is much lower than that of band-gap based POR circuits. Additionally, since the circuit uses only 10 transistors, its area is very small—just 67 5µm2—which shows excellent area efficiency compared to other POR circuits.

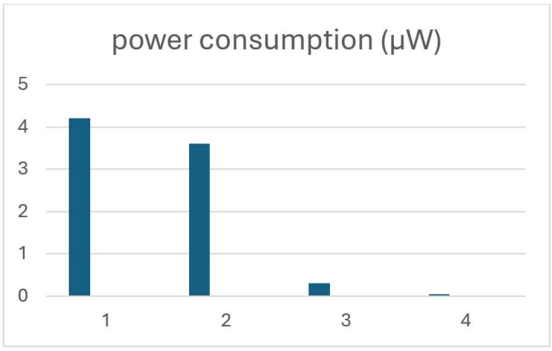

Fig. 3. Bar graph of power of different Technologies

This bar graph shows power consumption (in microwatts, µW) of different technologies used in a Power-On Reset (PoR) circuit. Technology 1 consumes the highest power (~4.2 µW). This could be a conventional design or older CMOS method. Technology 2 consumes slightly less power (~3.5 µW), maybe a partially optimized or newer ver-sion. Technology 3 shows significantly lower power (~0.3 µW), likely an optimized low-power design. Technology 4 has negligible power consumption, possibly the proposed ultra-low-power design in the paper. The graph shows that power consumption decreases from Technology 1 to 4, demonstrating improvements in circuit design techniques. The aim is to reduce power for efficient performance, especially important in battery-operated or compact systems.

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