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Optimized Design of a Double Tail Dynamic Comparator using 18nm FinFET Technology

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***Abstract*— The research work presented in this paper focuses on the optimized design of a dual-tail dynamic comparator using 18 nm FinFET technology, aimed at achieving high-speed decision-making with significantly reduced power consumption. The primary objectives are to enhance comparator accuracy, minimize delay, reduce leakage, and ensure stable operation at low supply voltages. To achieve these goals, a dual-tail dynamic architecture is adopted, separating the pre-amplifier and latch stages to improve gain, reduce input referred offset, and minimize kickback noise. The circuit is implemented at the schematic level in Cadence Virtuoso, utilizing FinFET devices with optimized fin count and threshold voltage selection to achieve an optimal power–performance trade-off. The evaluation procedure includes DC operating-point analysis, transient simulations, delay characterization under differential input sweeps, and power measurement through current probing at the supply node. The results demonstrate substantial reductions in power consumption compared to the initial design, along with improved regeneration speed and reduced offset. The architecture maintains stable decision-making even at reduced supply voltages, highlighting the advantages of FinFET-based comparator implementations in nanoscale nodes. The optimized comparator is suitable for several high-performance applications, including high-speed and low-power ADCs, precision sensor front-ends, portable medical electronics, and next-generation mixed-signal integrated circuits. Future work may explore skewed-clock techniques, subthreshold operation for ultra-low-power designs, and process-corner optimization to further enhance performance in advanced VLSI systems.**

***Index Terms*— Dynamic Comparator, Dual-Tail Architecture, FinFET Technology, Low-Power Design, Analog-to Digital Converters (ADCs)..**

I. INTRODUCTION

The rapid evolution of modern electronic systems has significantly increased the demand for high-performance analog and mixed-signal building blocks capable of operating reliably at reduced power and supply voltage levels. Among these blocks, comparators play a central role in analog-to-digital converters (ADCs), memory readout circuits, sensor interfaces, and high-speed data acquisition systems.

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With the continued downscaling of semiconductor technologies into deep nanoscale regimes, traditional comparator architectures suffer from major performance degradations, including increased leakage current, limited voltage headroom, and severe short channel effects. These limitations impose significant challenges on maintaining high-speed operation and accuracy [1].

Dynamic comparators—especially those based on the double-tail architecture—have gained widespread attention due to their low static power consumption, high decision speed, and ability to function efficiently under low supply voltages. However, as planar CMOS reaches its physical limits, device-level enhancements become essential to sustain comparator performance. FinFET technology, with its superior electrostatic control, reduced leakage, and enhanced drive strength, emerges as a promising solution for enabling robust circuits at sub-20 nm technology nodes [2].

This project presents a systematic design and optimization of a Dual-Tail Dynamic Comparator (DTDC) implemented in 18 nm FinFET technology, targeting substantial improvements in delay, power consumption, and accuracy. The work encompasses architectural refinement, transistor-level optimization, and detailed simulation-based characterization using Cadence Virtuoso. The goal is to develop a comparator design that is scalable, energy-efficient, and suitable for next-generation VLSI systems [3].

II. Design Implementation

A. Block Diagram & Conventional Designs

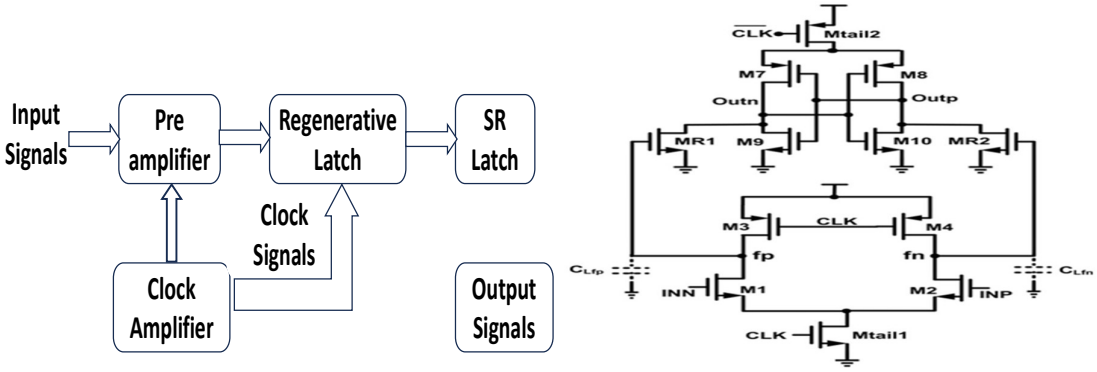

Fig. 1. Overall block diagram of the proposed system Cascode Circuit diagram of a basic Double Tail Comparator

III. Proposed Design

A. Blocks Designed

The comparator consists of a cross-coupled preamp and a clocked latch. The preamp uses differential input pairs with a tail transistor to amplify small input differences during the evaluation phase. A double-tail configuration reduces stacking, enabling low-voltage operation. The latch employs cross-coupled inverters that regenerate the preamp output into a full-swing digital signal. Clock gating ensures both stages operate only when needed, minimizing static power and improving energy efficiency in 18nm FinFET technology [4].

The design also includes a local clock generator block to generate and drive the clock signals into the cascaded pre-amplifier block as well as the cross coupled regenerative latch stage. This allows us to skew the clock signals generated according to the needs and drive those clock signals into the comparator. The design uses an SR Latch to improve the readability of the comparator output waveforms making it easier to understand the outputs generated by the comparator. The figure 8 shows the complete design of the optimized double tail comparator [5].

B. Inputs Driven

The differential inputs (V1, V2) are analog voltages whose relative magnitude determines the digital output. They are applied to the gates of input transistors in the preamp. VDD and GND serve as power and reference rails, with supply voltage scaled for 18nm FinFET (e.g., 1.0 V). The clock signal synchronizes operation: during reset (CLK = 0), output nodes are pre-charged; during evaluation (CLK = 1), amplification and latching occur. Proper clock timing prevents metastability and reduces kickback noise [6].

C. Preamplifier

The cross-coupled preamp is clock-gated to operate only during the evaluation phase, where the tail transistor enables current flow when the clock is high, allowing differential amplification of the input signal. Clocked input switches or isolation transistors prevent DC path during reset, while the cross-coupled PMOS pair enhances gain and speeds up output node divergence, improving initial voltage swing for the latch and reducing sensitivity to kickback noise [7].

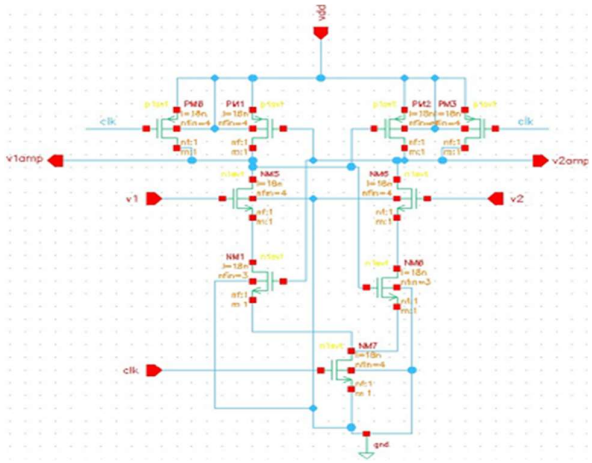

Fig. 2. Pre-amplified differential voltage sensing pulldown component of the DTDC

D. SR Latch Block

The addition of an SR latch at the output of the double tail comparator's internal latch enhances output stability and readability by acting as a storage and buffering element. After the internal clocked latch regenerates the differential signal during the evaluation phase, the resulting digital outputs (out1 and out2) may still be susceptible to noise or transient glitches, especially during switching or near decision thresholds. The external SR latch captures and holds these final logic states when enabled, providing a clean, stable output that does not fluctuate [8].

This improves signal integrity, especially in noisy environments or when driving large capacitive loads, and ensures that downstream digital circuits receive a well-defined logic level. Furthermore, the SR latch can help mitigate metastability effects by synchronizing the comparator output with system timing, thereby increasing overall reliability [9].

After passing through the SR latch the outputs undergo lesser switching operations which is helpful in reducing the amount dynamic power being consumed when there is a transition between logic ‘0’ to logic ‘1’ and vice versa [10].

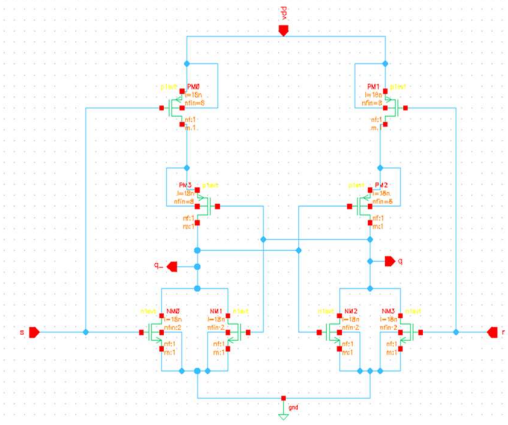

Fig. 3. Schematic diagram of the SR Latch designed

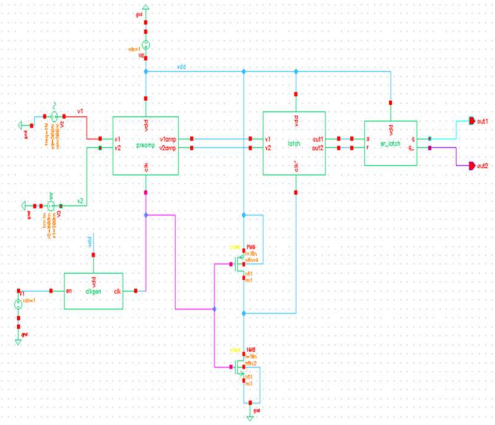

Fig.4: Complete design of the optimized double tail Dynamic latch comparator

IV. SIMULATION RESULTS

Transient simulations show sub-nanosecond delay and fast regeneration, confirming high-speed operation. Power analysis reveals low dynamic consumption due to clock gating and FinFET advantages. Overall, the comparator achieves high speed, low power, and good noise immunity suitable for advanced ADC applications [11].

In the transient analysis of the double tail comparator with clock-gated preamplifier, latch, and output SR latch, the simulation demonstrates faster regeneration of the differential outputs (out1 and out2) during the evaluation phase (clk = high), with minimal delay and clean transitions to rail voltages .The SR latch ensures that the final logic state is captured and held stably, reducing glitches and improving readability, especially under low overdrive or noisy conditions [12].

For power analysis, the design shows significantly reduced power consumption due to clock gating of both preamplifier and latch stages only drawing dynamic current during active phases. There is a stable static power of around 124 nW being consumed by the circuit during the operating phases like the evaluation phase and the pre-charge phase (also referred to as the reset phase for the latch stage) for a supply voltage of 1.0V. Transient power peaks will align with clock edges, confirming activity only during evaluation, while the SR latch adds negligible overhead due to its simple static structure

A. Performance Analysis

Key metrics include propagation delay, power consumption , offset voltage , and kickback noise. Delay is measured from input transition to valid output; power is analyzed dynamically and statically using Cadence ADE. Offset is evaluated via DC simulations to account for mismatch. Kickback noise is assessed by observing disturbances at the input nodes during regeneration. PV (process, voltage) variations are simulated to ensure robustness across operating conditions.

Using 18nm FinFET technology for a double tail comparator design offers several significant advantages over traditional CMOS approaches. The 18nm FinFET node enables highly advanced and compact integrated circuits due to its nominal feature size of 18 nanometres, which supports improved scalability and performance.

In the figure 5, the first waveform (in the colour red) represents the out2 signal which corresponds to the input voltage v2. The second waveform (in the colour green) represents the out1 signal which corresponds to the input voltage v1. The input voltages v1 and v2 are the purple and light blue signals, respectively, that are overlapped on top of each other where the signal v1 is a sinusoidal signal of time period 1us (frequency of 1MHz) and the signal v2 is a simple pulse or square wave of time period 0.5 us (frequency of 2MHz).

As seen in the diagram, when the v1 voltage is higher than the v2 voltage the out1 voltage is pulled up to logic '1' and subsequently the out2 voltage is pulled down to logic '0', and when the v2 voltage is higher than the v1 voltage the out2 voltage is pulled up to logic '1' and subsequently the out1 voltage is pulled down to logic '0'. The output signals show how the evaluation happens only when the clock signal goes to logic '1' and hence is referred to as the "evaluation phase". The output also shows that when the clock signal goes to logic '0' the outputs irrespective of what logic they currently display gets pulled to ground, indicating that the output is being reset

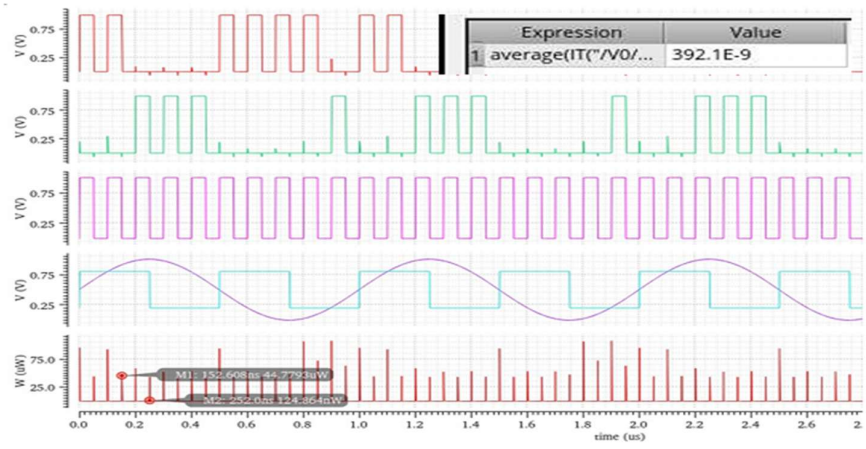

Fig. 5: Functional output with power analysis for a differential input pair of a square pulse wave and a sinusoidal wave

B. Improves Readability

The SR latch captures and holds the comparator's output state at a precise moment (typically on a clock edge), ensuring a clean, stable digital output. Without it, the comparator output may exhibit metastability or transient glitches during decision-making, especially under small input differences. The latch provides definite logic levels (0 or 1), enhancing signal clarity for downstream digital circuits.

The way how this works is that the truth table of an SR Latch shows that when the two inputs are complimentary the outputs are the same as the inputs and when the inputs are both logic '0' then the output retains its previous value (in case of a SR Latch created by cascading two NOR gates). This is because if the SR Latch was made by cascading two NAND gates then the outputs would have to be pre-charged instead of reset during the logic '0' phase of the clock cycle

V. CONCLUSIONS

The proposed double tail comparator, implemented in 18nm FinFET technology and enhanced with an SR latch and local clock generator, achieves high speed, low power consumption, and excellent noise immunity. The SR latch ensures stable output levels and suppresses metastability, while the local clock generator enables precise timing control, reducing power through optimized pre-charge and evaluation phases. Together, these components enhance reliability and performance in high-speed mixed-signal systems. The results obtained shows a power consumption as low as 124.86 nW during the normal operation and an average power of 392.1 nW when the circuit operates at frequency of 2 GHz and with a supply voltage of 1.0V.

The usage of sinusoidal signals along with a square wave of different frequencies as the input signal was to ensure proper representation of a real-life scenario of the input signal sequence when it is used in analogous applications such as ADCs, RF based systems, etc. In conclusion, further improvements in terms of power consumption can be achieved by power scaling, skewing the clock signals that are generated from the local clock generator block. This design plays a significant role in a large number of applications revolving around analog devices such as transceivers, RF (radio frequency) devices, audio based systems, sensors and IOT based networks, etc.

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