

Comparative Analysis of Ternary Logic Gates using CMOS and CNFET

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Abstract— The limitations inherent in traditional binary logic systems, particularly regarding interconnect complexity and energy efficiency, have spurred increased interest in multi-valued logic (MVL), with a specific focus on ternary logic due to its capacity for enhanced information density and computational efficiency. The paper presents a comparative analysis of fundamental ternary logic gates by using unbalanced ternary logic (0, 1, 2) Using multi-threshold in both conventional CMOS and innovative Carbon Nanotube Field-Effect Transistor (CNFET) technology. Utilizing the Cadence Virtuoso design tool, various ternary gates, including the ternary inverter, NAND, NOR gate were designed and simulated. Key performance metrics such as power dissipation and delay were Calculated.

Index Terms— Ternary, multi-valued logic (MVL), CMOS, CNFET, Cadence.

I. INTRODUCTION

With the expanding utilization of artificial intelligence (AI), the Internet of Things (IoT) and autopilot technologies, a substantial volume of data is being generated that necessitates processing. Projections indicate that the total data produced annually will increase from 64.2 zettabytes (1021) in 2020 to over 180 zettabytes by 2025. Consequently, there is a significant demand for computers with enhanced data density to fulfil future data processing requirements. [1] As Moore's Law decelerates, enhancing chip performance through mere reduction of transistor feature size becomes increasingly challenging. Binary circuits are characterized by high energy consumption.[2] In recent decades, the significance of Si-MOSFET (Silicon Metal-Oxide Semiconductor Field-Effect Transistor) technology has grown. Si-MOSFETs have been described as an alternative for integrated circuits in various technical domains. Due to scaling, Si-MOSFET-based devices encounter limitations such as static current and short channel effects.[3] Carbon Nanotube Field Effect Transistors(CNFETs) are employed to address the limitations of Si-MOSFET. CNFET technology provides a high ON-state current, minimal power dissipation, and enhanced thermal stability. The unique capability of CNFETs to adjust the Threshold Voltage(V_{th}) by altering carbon nanotubes diameter (DCNT).[4] Multi-valued logic (MVL) circuits enhance data density by partitioning the operating voltage into more than two intervals. Recently, MVL circuits have been investigated to address the limitations inherent in CMOS-based binary logic circuits. MVL circuits are anticipated to improve power, performance, and area characteristics, as they require fewer logic gates and interconnects than binary logic for equivalent functions by computing multiple values within a single logic gate.[5] Ternary logic is a numerical system with one logical value more than binary logic. Namely there are two kinds of ternary logic: balanced ternary logic, which uses '−1, 0, 1' and unbalanced ternary logic, which uses '0, 1, 2' Each value corresponds to '−V_{dd}, 0, V_{dd}' and '0', V_{dd}/2, V_{dd}' respectively.[6]

Table 1 illustrates the representation of Decimal numbers in both binary and ternary logic (Balanced and Unbalanced).

If we consider a number (50)₁₀ in the number of bits required to represent the number in binary is 6 bits (110010)₂ . where as in ternary it requires 4 trit (1212)₃.

TABLE I: REPRESENTATION OF DECIMAL NUMBER IN BINARY BALANCED AND UNBALANCED TERNARY CODE

Decimal	Binary code	Balanced ternary Code	Unbalanced ternary Code
5	0101	1-1-1	012
2	0010	01-1	002
0	0000	000	000
7	0111	1-11	021
9	1001	100	100

II. LITERATURE REVIEW

The article by G. Thrishala discusses the application of ternary logic to design digital circuits performance is better compared to the conventional binary approach. The authors discuss a number of combinational implemented using CMOS 90 nm technology. In general, the work highlights the increasing significance of multiple-valued logic in promoting digital design methodologies. [7]

The author Abhiman Kumar describes an algorithm for function minimization in multivalued logic systems and specifically ternary logic with radix 3. The method introduced is ternary Karnaugh map-based. With an increase in radix, the logic minimization complexity also increases, and hence such tools become vital for efficient circuit design.

The output logic is expressed in Sum-of-Product (SOP) form with separate treatment of levels 1 and 2. The correctness of the algorithm is established by comparing its output with ternary half adder and full adder truth tables for correct minimization, optimized for ternary digital architectures [8]

The article by Furqan Zahoor presents a detailed survey of ternary logic systems with special focus on their ability to go beyond binary in VLSI design. It points out that ternary logic can minimize chip area and interconnects by as much as 50%, and save power by about 36.9% over binary logic. The authors compare different technologies such as CMOS, CNFET, GNRNFT, RRAM, and FinFET for ternary gate and arithmetic circuit implementation.

CNTFET-based ternary circuits exhibit greater energy efficiency and scalability, with improved ON/OFF current ratios being offered by GNRNFTs. Simulation outcomes illustrate ternary designs consuming up to 40% reduced PDP (Power-Delay Product) with immensely lower transistor counts. [9]

According to S.V. Ratan Kumar pseudo NCNFT is an effective method of designing ternary arithmetic circuits. The authors design ternary logic gates (inverter, AND, OR) with just pseudo-NCNFTs and design full-adder and full-subtractor circuits at the trit level. Designed in 32 nm technology through HSPICE simulation, the designed circuits show substantial improvement in performance showing up to 65.82% power delay product (PDP) [10]

The author Chetan Vudadha [11] presents a multiplexer-based design method for designing ternary logic circuits with CNFETs in order to reduce complexity and enhance energy efficiency. A ternary multiplexer is first designed as a basic building block that is used to design a 1-bit comparator and half adder. SPICE. The results indicate the proposed half adder reduces delay by 27% and power-delay product by 23%, validating the advantage of the multiplexer-based CNFET design.

III. METHODOLOGY

A. Multi-Threshold Voltage in CMOS logic

TABLE II: SWITCHING OF CMOS TRANSISTOR.

MOSFET	PMOS		NMOS	
				
INPUT =0 (0V)	ON	ON	OFF	OFF
INPUT =1 (V _{dd} /2)	ON	OFF	ON	OFF
INPUT =2 (V _{dd})	OFF	OFF	ON	ON



Low V_{th}
MOSFET



High V_{th}
MOSFET

Multi-threshold voltage technique employs transistors of varying threshold voltages in a design to improve power and performance. High-Vt transistors minimize leakage power but are slower, whereas Low-Vt transistors provide faster switching at the expense of increased leakage. Table 2 shows the switching of CMOS transistor, when the input logic is '0' ($V_{in} = 0V$) both lvt (low threshold) and hvt (high threshold) pMOS are turn ON. When the input logic is '1' ($V_{in} = V_{dd}/2$) lvt of both pMOS and nMOS are turn on. When the input logic is '2' ($V_{in} = V_{dd}$) lvt and hvt of both nMOS is turned ON.

B. Multi-Threshold Voltage in CNFET logic

The Stanford CNFET model employs Semi-conducting single walled carbon nanotube (CNT) as channel for conduction; the highest current drive is 35uA when the supply voltage is Vdd. The arrangement of atoms along the tube in a single-walled CNT is described by the chirality vector. The diameter of CNFET is given by equation 1.

$$D_{cnt} = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + nm} . \quad (1)$$

a_0 represent the inter-atomic distance between each carbon atom and neighbouring atom and the integer pair (n,m) denotes the chirality vector.[12]. Equation 2 demonstrates that threshold voltage(V_{th}) is inversely proportional to the CNT diameter.

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{a\pi}{D_{cnt}} . \quad (2)$$

TABLE III: RELATION BETWEEN CNT DIAMETER, CHIRALITY AND THRESHOLD VOLTAGE.

chirality	CNT diameter	Threshold Voltage (V_{th})	
		N-CNFET	P-CNFET
(19,0) hvt	1.487nm	0.289V	-0.289V
(13,0) svt	1.018nm	0.428V	-0.428V
(10,0) lvt	0.783nm	0.559V	-0.559V

The above table 3 represent the relationship between CNT diameter, Chirality and V_{th} . For the chirality's of (19,0), (13,0) and (10,0) the CNFET is operated as hvt, svt and lvt respectively.

C. Ternary Inverter

In general, there are three types of inverters namely negative ternary inverter (NTI), standard ternary inverter (STI) and positive ternary inverter (PTI) as show in fig 1,

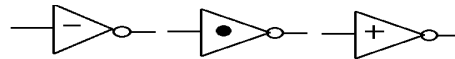


Figure 1: Symbols of (a) NTI, (b) STI and PTI.

TABLE IV: FUNCTIONAL TABLE OF TERNARY INVERTER

Input	NTI	STI	PTI
0	2	2	2
1	0	1	2
2	0	0	0

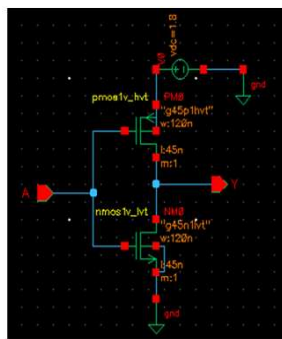


Figure 2: Schematic of NTI.

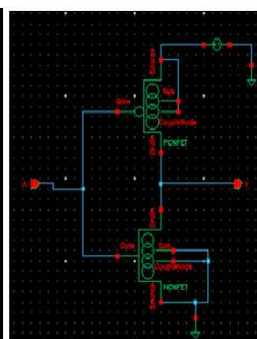


Figure 3: Schematic of PTI

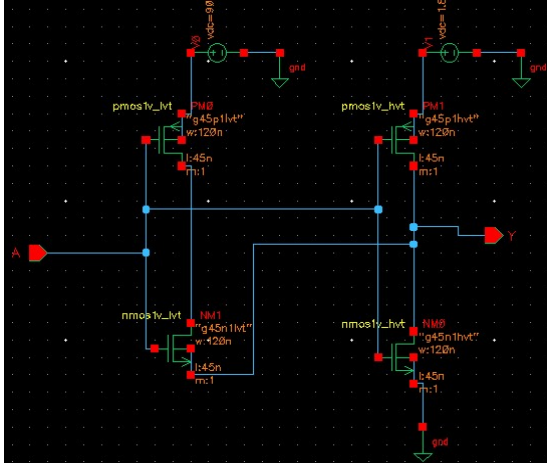


Figure 4 (a): The schematic of STI using CMOS.

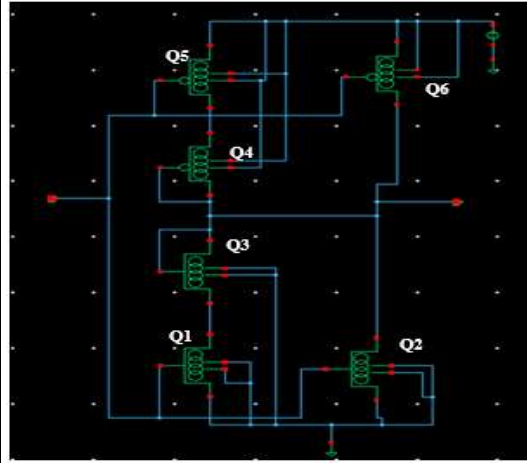


Figure 4 (b): The schematic of STI using CNFET

The schematic NTI is as shown in the figure 2. For pMOS hvt cell is made used and nMOS is of lvt hvt cell is made used. So that when the input is at logic '0' pMOS is ON and nMOS is OFF make the output to reach Vdd (logic 2). When input is logic '1' and '2' the output at logic '0' make the pMOS to OFF and nMOS to ON.

The figure 3(a) and 3(b) shows the implementation of STI using CMOS and CNFET respectively. CNFET transistor Q1, Q5 has chirality of (10,0) Q2, Q6 has chirality of (19,0) and Q3, Q4 has chirality of (13,0). when the input is logic '0' Q5, Q6 are ON and Q1, Q2 are OFF output is logic '2'. when the input is logic '1' Q5, Q1 are ON and Q6, Q2 are OFF, Q4 is ON making the output is logic '1'. when the input is logic '2' Q1, Q2 are ON and Q5, Q6 are OFF output is logic '0'.

The schematic of PTI is as shown in the figure 2. For pMOS (pCNFET) lvt cell is made used and nMOS (nCNFET) is of hvt cell is made used. So that when the input is at logic '0' and '1' pMOS (pCNFET) is ON and nMOS (n CNFET) is OFF make the output to reach Vdd (logic 2). When input is logic '2' the output at logic '0' make the pMOS (pCNFET) to OFF and nMOS (nCNFET) to ON.

D. Ternary Logic Gate

In unbalanced ternary logic, where the logic levels are typically 0, 1, and 2, the ternary AND gate produce the minimum of the inputs, and the OR gate produces the maximum. Generalizing even more, the ternary NAND gate produces the inverted minimum of the inputs, and the ternary NOR gate produces the inverted maximum.

TABLE V: FUNCTIONAL TABLE OF TERNARY LOGIC GATES

A	B	AND	OR	NAND	NOR
0	0	0	0	2	2
0	1	0	1	2	1
0	2	0	2	2	0
1	0	0	1	2	1
1	1	1	1	1	1
1	2	1	2	1	0
2	0	0	2	2	0
2	1	1	2	1	0
2	2	2	2	0	0

$$\text{AND: } a.b = \min(a, b). \quad (3)$$

$$\text{OR: } a+b = \max(a, b). \quad (4)$$

$$\text{NAND: } \sim(a.b) = \sim\min(a, b). \quad (5)$$

$$\text{NOR: } \sim(a+b) = \sim\max(a, b). \quad (6)$$

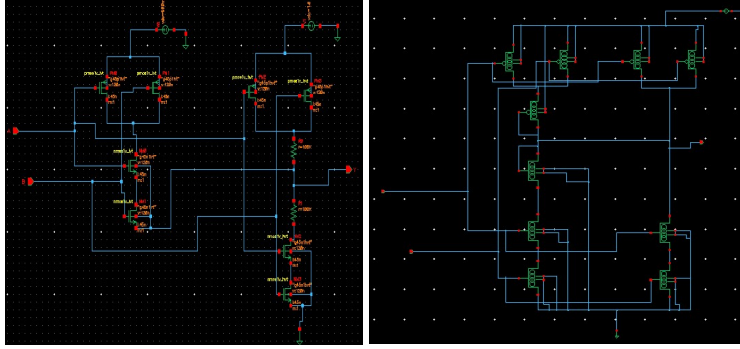


Figure 5(a): Schematic of TNAND using CMOS Figure 5(b): Schematic of TNAND using CNFET.

The figure 5(a), 5(b) shows the implementation of ternary NAND gate using CMOS and CNFET respectively. The output of gate is given in the equation (5).

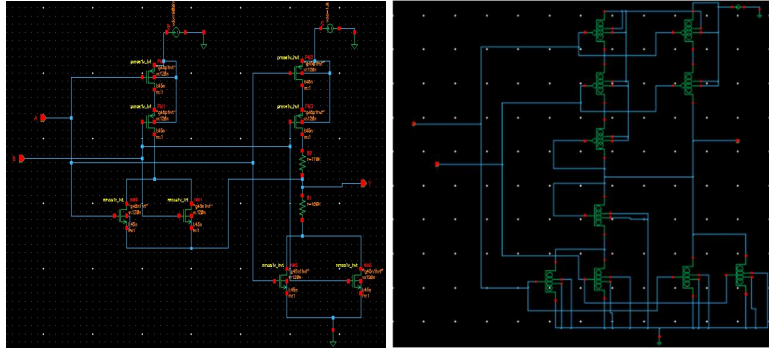


Figure 6(a): Schematic of TNOR using CMOS. Figure 6(b): Schematic of TNOR using CNFET.

The figure 6(a), 6(b) shows the implementation of TNOR gate using CMOS and CNFET respectively. The output of gate is given in the equation (6).

IV. RESULT

The transient response of the Ternary logic gates is shown in the below figures the logic value is (0, 1 and 2) are 0V, 0.9V and 1.8V for CMOS and 0V, 0.45V and 0.9V for CNFET respectively.

A. Ternary Inverters

Figure 7, 8(a) (b) shows the transient response of STI, PTI and NTI respectively. The wave form is verified using the Table 4.

B. Ternary NAND and NOR

Figure 9 and 10 shows the transient response of Ternary NAND and NOR respectively and the output matches with the equation (5) and (6) respectively.

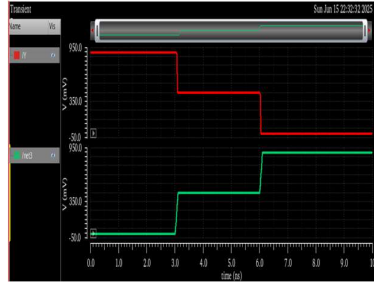


Figure 7: Output of STI

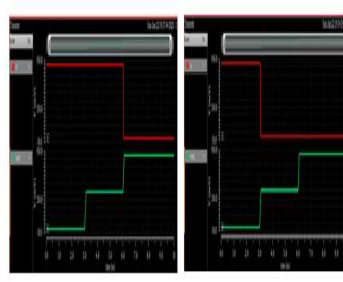


Figure 8: Output of PTI (a) and NTI (b)

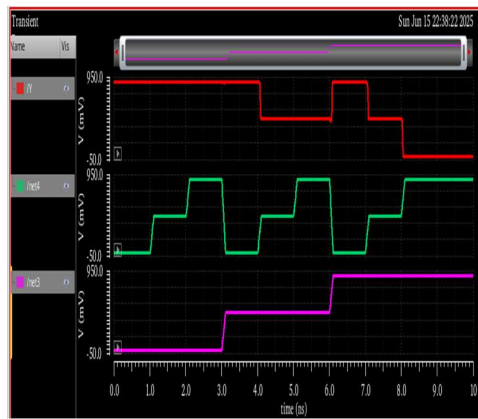


Figure 9: Output of TNAND gate.



Figure 10: Output of TNOR gate.

V. CONCLUSION

The comparative study of STI, NAND, and NOR logic gates based on CMOS and CNFET technologies, one can see that CNFET circuits have tremendous power savings as well as speed improvements. Power wise, CNFET gates use much less power compared to CMOS. As an illustration, the power of the NAND gate drops by about 70% (from 0.62 μ W to 185 nW), while the NOR gate experiences a 98.9% drop (from 4.67 μ W to 49 nW). In terms of delay, CNFET circuits exhibit dramatic reductions: the STI gate experiences a 99.9% reduction in delay, the NAND gate 99.8% reduction, and the NOR gate experiences a 98.7% improvement. These findings strongly suggest the use of CNFET technology in future VLSI circuits, where ultra-low power consumption and high-speed operation are essential.

REFERENCE

- [1] G. Zhao et al., "Efficient Ternary Logic Circuits Optimized by Ternary Arithmetic Algorithms," in IEEE Transactions on Emerging Topics in Computing, vol. 12, no. 3, pp. 826-839, July-Sept. 2024.
- [2] J. M. Aljaam, R. A. Jaber and S. A. Al-Maadeed, "Novel Ternary Adder and Multiplier Designs Without Using Decoders or Encoders," in IEEE Access, vol. 9, pp. 56726-56735, 2021.
- [3] Katyayani Chauhan and Deepika Bansal "Low power CNFET based ternary multiplier for digital signal processing applications" Engineering Research Express 6 February 2024.
- [4] R. A. Jaber, J. M. Aljaam, B. N. Owaydat, S. A. Al-Maadeed, A. Kassem and A. M. Haidar, "Ultra-Low Energy CNFET-Based Ternary Combinational Circuits Designs," in IEEE Access, vol. 9, pp. 115951-115961, 2021.
- [5] J. Yoon, S. Baek, S. Kim and S. Kang, "Optimizing Ternary Multiplier Design With Fast Ternary Adder," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 2, pp. 766-770, Feb. 2023.
- [6] S. Kim, S. -Y. Lee, S. Park, K. R. Kim and S. Kang, "A Logic Synthesis Methodology for Low-Power Ternary Logic Circuits," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 9, pp. 3138-3151, Sept. 2020.
- [7] G. Thrishala, K. Ragini, "Design and Implementation of Ternary Logic Circuits for VLSI Applications" International Journal of Innovative Technology and Exploring Engineering ISSN: 2278-3075, Volume-9 Issue-4, February 2020
- [8] Abhiman Kumar, Anurag Sah, Dhanesh Prakash Gupta, Dr. Asima Adak "Ternary Logic Applications in Basic Combinational Circuits" International Journal of creative research Thoughts Volume 11, Issue 5 May 2023 | ISSN: 2320-2882-2023
- [9] Furqan Zahoor, Ramzi A. Jabber, Usman Bature Isyakuc, Trapti Sharma, Faisal Bashira, Haider Abbas, Ali S. Alzahrana, Shagun Gupta, Mehwish Hanif "Design implementations of ternary logic systems: A critical review" Results in Engineering 23 August 2024
- [10] SV Ratan Kumar, L. Koteswara Rao, M. Kiran Kumar. "Design of ternary full-adder and full-subtractor using pseudo NCNTFETs" e-Prime - Advances in Electrical Engineering, Electronics and Energy - 18 September 2023.
- [11] Chetan Vudadha, Sreehari V, M. B. Srinivas "Multiplexer Based Design for Ternary Logic Circuits". Analog and Mixed Signal III - 2012.
- [12] Ramzi a. Jaber, Abdallah Kassem, Amadei-Hajj, Lina. El-Nimri, and Ali Massoud Haidar "High-Performance and Energy-Efficient CNFET-Based Designs for Ternary Logic Circuits" - 30 July 2019.