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Multilevel Cascaded Inverters having Improved Output Level with Reduced Power Switches - A Novel Approach

Sanjiba Kumar Bisoyi[1], Parveen.P.Terang[2], Sampath Kumar.V[3] and Veerendra Kumar A.N[4]
[1-4]JSS Academy of Technical Education, Noida
Email address: -sanjibabisoyi.eed@jssaten.ac.in, ppterang.eed@jssaten.ac.in, sampath.kumarjss@jssaten.ac.in, veerendrakumar@jssaten.ac.in

***Abstract*—Off late, multilevel inverter (MLI) technology has emerged significantly in medium voltage applications especially those requiring high power. This has proved to be an important option for domestic and industrial applications. Multilevel inverters having many voltage levels could generate improved voltage waveforms for these applications. The main disadvantage of any topology of MLI is the requirement of power supplies of a large number as well as semiconductor components to get the desired multistep output voltage waveforms. This paper has attempted to focus on diminishing the number of power supplies and reducing the semiconductors for a certain number of output levels. A new scheme is proposed to get an increased number of levels for an output voltage with a decrease in the number of switches, components and gate driver circuits. Using this proposed method, the size as well as the power consumption in the gate driver circuits has been reduced to a great extent. The proposed methodology discussed in this paper, presents an 81-level Hybrid Multilevel Inverter for applications suitable to medium and high voltage and this design works by optimizing the number of power switches for a given output level. The results have been presented, highlighting the obtained output waveform seen to be nearly sinusoidal. With an output close to a sinusoid, the benefits of reduced losses are observed in terms of significantly good power quality or low total harmonic distortion (THD) as compared to other conventional topologies. The benefits of the proposed circuit configuration is its simplicity and ease of control. The working principle and output waveforms obtained have been analyzed and presented using MATLAB /Simulink.**

***Index Terms*— DER, Hybrid multilevel inverter, multilevel inverter, MLI, modulation index, power quality, PWM, switching angle, THD, voltage source inverter.**

I. INTRODUCTION

With the high penetration of renewables into the power system, to meet the ever-growing demand of energy, the variability of the distributed energy resources (DER) is a concern for all. In addition to the variability is the subsequent penetration of power electronics (PE) devices into the power system. This is contradictory to the search for a sustainable solution of energy, as these power electronic interfaces affect the grid performance and reliability. PE devices include systems having a dynamic behaviour and pertaining to protection and control. The dynamic behaviour makes the PE devices very complex when compared to the classical power system devices

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and have an undesirable impact on the performance and stability of AC networks.
Multilevel converters have the advantage of reducing voltage or current stress of the PE interfaces in applications requiring high power and high voltage. Fig. 1 shows the evolution of these ML topologies. In recent times, the Hybrid topology is gaining prominence due to the significant decrease in equipment. With the need to use Renewable energy resources as an alternative to conventional resources, the PE interfaces devised were two-level and three level inverters [1,2,3]. For different levels of inverters, Fig. 2 shows the basic switching cells which have evolved.

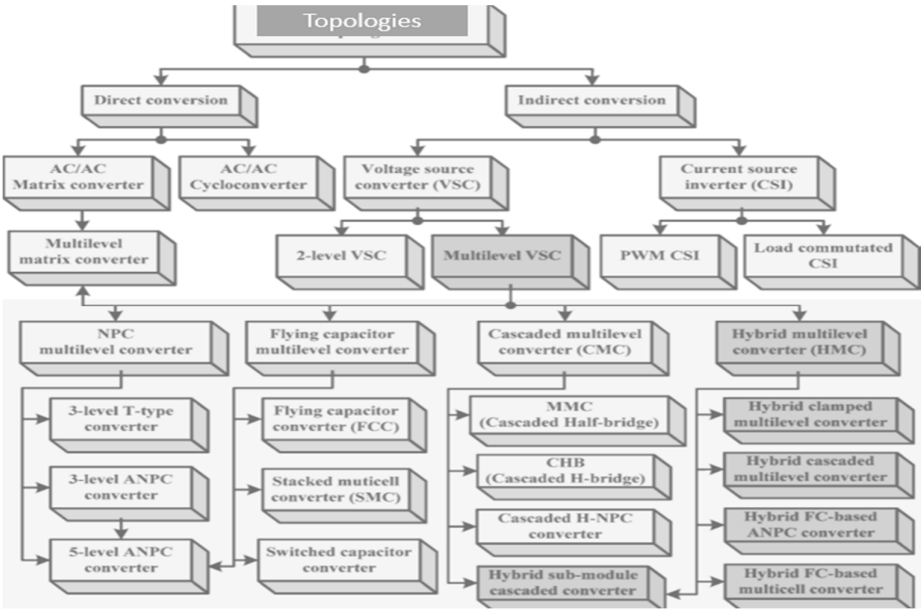


Fig.1 ML Converters- Various Topologies

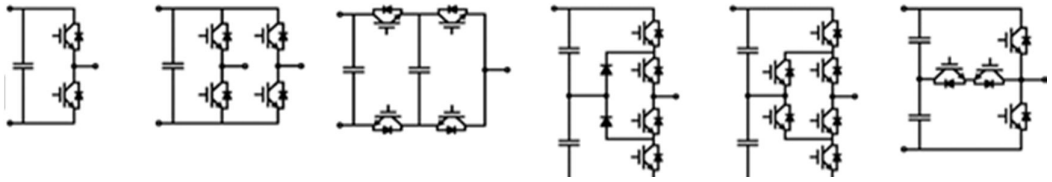


Fig. 2. Basic switching cells. (a) 2Level cell, (b) 3 Level HB cell, (c) 3 Level FC cell, (d) 3 Level NPC cell, (e) 3 Level ANPC cell, (f) 3 Level T-type cell

While the multilevel inverter (MLI) is advantageous and works well to give high power with low harmonic content, the dynamics change with an increase in output voltage. Any increased output voltage leads to increase in the semiconductor devices. The loss incurred due to this addition is difficult to estimate, as each semiconductor device is different [4]. The challenge, therefore, is to compute the switching and conduction loss. [5] presents a simple and accurate methodology of estimating this loss in an and has validated the result for a 3 & 4 level diode clamped inverter system. With the attractive features of MLI, the conventional configuration with more number of switches is a great limitation for all types of applications [6,7]. As understood in [8] levels of a large number having a desired output further enhanced with reduced number of switches and driver circuits lead to an impact on the size, complexity and power consumption. The proposed use of a 7 level MLI for renewable energy applications [9] with just 5 unidirectional switches ensures decrease in size, loss and installation cost.
For a grid connected PV system, the arrangement of panels are in multiple strings to get desired power output.[10] proposes the modulation of a converter, by controlling gates of the switches used internally in each converter while another topology proposed is the asymmetric multilevel inverter [11,12] where more output levels are obtained with the use of the same number of voltage sources. The proposed topology has the added advantage of reduced THD along with low voltage stress.

The number of steps in a MLI gives good quality waveforms which have the capacity to follow a reference with accuracy. The modulation of the voltage waveform can be done in amplitude instead of the pulse-width. The focus moves particularly to minimizing semiconductors and power supplies. The optimization process showing the increase in the power transistors used with increase in levels along with the various combinations and topologies is reported in [13]. The increase in output voltage levels with switches which are lesser in number helped to obtain reduced losses and cost as reported in [14]. Proposed methodology of further decreasing the switches [15] of an MLI with enhanced performance has also been reported.

With the advancement towards better and more effective PE devices the research of MLI has moved towards balancing the voltage between various levels all the while reducing the cost and simplicity of control and maintaining good power quality. The highlight of this proposed strategy therefore, is an increase in output level number with decrease in quantity of output switches, while still keeping the power circuit simple. The significance of the research work is improvement in power quality and a higher output voltage. To meet the demands of the present power scenario, the scheme reduces the switching devices thereby incurring less loss. The efficiency of this topology has been compared to the existing conventional topology and is recommended for its simplicity. Section II gives the proposed topology which includes the circuit diagram, the switching pattern used and the modulation technique. Results and comparison of the conventional topology to the proposed topology has been given in the Sections III and Section IV respectively.

II. Proposed Topology

The structure introduced here is a multilevel inverter which is cascaded and asymmetrical. The number of DC sources that have been used are unequal. The circuit diagram of the proposed scheme is given in Fig. 3. This structure maintains number of full bridge units while increasing the output levels of voltage. At a higher frequency of modulation, higher voltage levels are attained making this topology very useful for high power applications. In addition, the reliability increases as the quantity of switches employed are significantly decreased. Further, increased steps ensure high resolution of the output voltage. This type of configuration will be of significant importance in adjustable speed drive applications as well as in AC power supplies.

The number of switches in the H Bridge being used in the topology is only two. The switches are bidirectional in nature and are required to conduct current in both directions as well as block the voltage. Since the switches perform both functions, the total number of switches are reduced by half, this reduction includes the gate driver circuits. Reduction in the number of switches therefore simplifies the circuit, decreases the losses and allows easy control. It also serves to be more economical.

A. Circuit Diagram

To understand the changes in the circuit diagram, the proposed circuit diagram has been shown alongside the conventional one in Fig. 4.

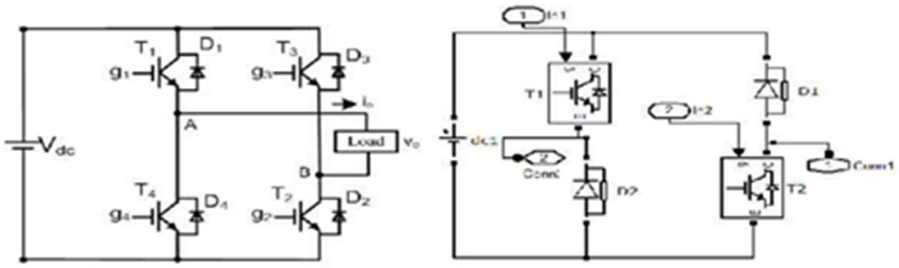


Fig.3 Circuit Diagram a) Conventional b) Proposed

B. Switching Pattern

The switching scheme used is illustrated in Table 2. and highlights the difference between the conventional and proposed topology, when both are compared in terms of output voltage. Looking at the output voltage levels of the conventional topology it is seen that when switching T1 & T2 if ON, an output voltage of +Vdc occurs but requires switching T3 & T4 to be switched ON to obtain the output voltage of -Vdc. The same output voltage level +Vdc is obtained when T1& T2 is in the ON position. Reaching the output voltage level -Vdc , however, can simply be achieved by setting T1 & T2 being switched OFF. The only additional feature in the proposed topology is ensuring that the diodes D1 & D2 are connected at a higher voltage.

TABLE I. CIRCUIT PARAMETERS OF PROPOSED TOPOLOGY

S.NO	Parameters, Unit	Circuit Symbol	Value
1	Resistance, Ω	Ron	0.001
2	Inductance, H	Lon	0
3	Voltage (Forward), V	Vf	1
4	10% fall time in Current, s	Tf	1*10-6
5	Tail time (Current), s	Tt	2*10-6
6	Current (Initial), A	Ic	0
7	Snubber resistance, Ω	Rs	1e-5
8	Snubber Capacitance, F	Cs	inf

TABLE II. SWITCHING PATTERN

Conventional Switching Pattern	T1T2	T3T4	V0
	1	0	+Vdc
	0	1	-Vdc
Proposed Switching Pattern	T1	T2	V0
	1	0	+Vdc
	0	1	-Vdc

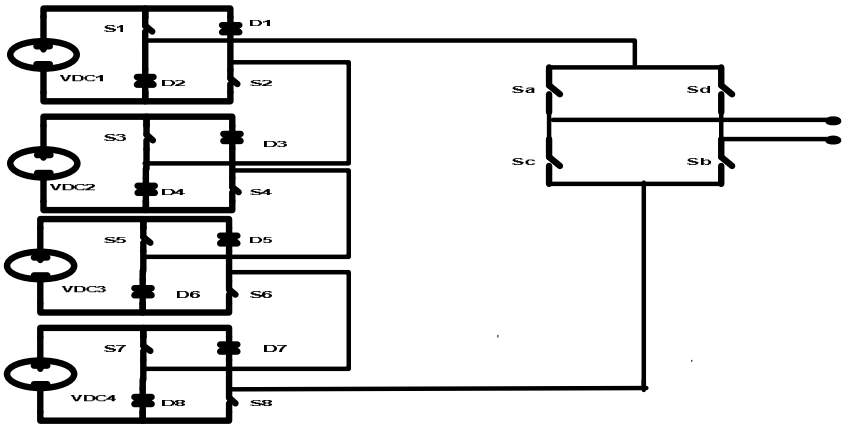


Fig 4. Proposed topology for 81 levels MLI

To understand the structure of the 81 level MLI with the switches, Fig. 4 illustrates the scheme of switches. And Table 2 gives the steps at various instants.

The scheme to generate voltage levels (output) is shown in Fig.4, where, for the generation of a nine level fundamental output voltage, the lower inverter is used. Addition and subtraction of each level from the wave (fundamental) is managed by the upper inverters. This synthesizes the stepped waves. With the use of VDC, 3 VDC, 9VDC and 27VDC, the synthesis of the 81 levels of the output is given between -40VDC to 40 VDC. To summarize the scheme: trinary DC voltages progressions of unequal DC sources have been considered. Preference has been given to the DC voltages having an amplitude in the ratio of 1:3:9:27; 81....3N where the

voltage progression is unequal and ((3N-1)/2 Vdc is the output attained. The Asymmetric Cascade H-Bridge (ACHB) is made up of 4-bridges, having the ability to achieve an 81 level output for the DC Sources of 27:9:3:1 ratio. The output waveforms at 81 levels are between -40VDC to 41VDC, ensuring a trinary distribution pattern of the DC voltage sources. The various steps of the DC sources are calculated as seen in Table III:

TABLE III. STEP CALCULATION

DC Sources	Step N for n=1,2,3,4…
Equal	2n +1
Binary	2(n+1) – 1
Trinary	3n

Working sequence of the circuit is as follows:
i) Zero to π (pi) for positive cycle and π (pi) to 2π period for negative cycle will work. However the common H-Bridge will determine positive and negative sequences.
ii) There will be two references (positive and negative) that are taken each for 40 levels.
iii) For each π duration, the 40 levels will be generated. And with the help of the common H-Bridge negative cycle is produced when tuned.
iv) Here the output frequency is 50Hz. So the time period will be 20ms.
v) For the sake of convenience, it is multiplied with 1000 and taken as 20 in function programming. To produce levels for each π duration, 10 is taken
vi) Here sinusoidal is taken as reference with 1 V. 40 levels will be compared with this 1V reference. So each level will be 1/40.g) Different levels may be termed as 1/40, 2/40, 3/40……..39/40, 40/40. The same for next 40 levels in other half cycle.
vii) Then to produce the first level among 40, the instant 1/40 should be taken. To produce the voltage at this instant, it should be turned ON before and maintain up to next level i.e. 2/40
viii) So first level starts from 0.5/40 to 1.5/40 i.e. 0.125 to 0.0375 whose average will decide.

C. Modulation Technique

The modulation technique which has been used in the proposed system is multi-carrier based. The Multi-carrier-PWM (MCPWM) is known for its switching simplicity and is preferred by many for the MLI. Information in the PWM technique is carried on a train of pulses. Width of each pulse carries the encoded information and helps maintain a constant voltage. The carrier requirement is for each level of a phase in the carrier-based multilevel modulation technique. This technique is advantageous as it improves the quality of the output voltage. There are two categories of carrier- based modulation schemes. They are a) level-shifted (LSPWM) and b) phase-shifted (PSPWM).
The difference between these schemes lie in the allocation of carrier modules with respect to each other. Level shifted modulation technique has an improved output when assessed against the phase shifted technique and the same has been applied in the proposed system with the Hybrid asymmetric cascaded multilevel inverter. This choice was to ensure a better harmonic spectrum with efficient utilization of voltage. The results in the proposed topology using Level shifting modulation has been presented in further sections of this paper.
For multi level voltage source converters, the common conclusion is that the increased number of switches will create a complex PWM switching scheme. This notion was debunked with demonstrations of the straight forward nature of the ML-PWM. In the level-shifted PWM methods, for a selected range of 10kHz to 100kHz, carrier signal frequency varies inversely to the switching period of the device. On the other hand values of the reference voltage, can have values in the range of –M.Vdc and M.Vdc. To ensure that the entire voltage range is covered, the carriers are the triangular waves of same phase and peak to peak amplitude, arranged vertically. The first module carrier covers a range 0 - Vdc, while the second covers a range Vdc - 2Vdc. The last module covers voltage (M−1) Vdc- M Vdc. Since the outcome is reduced THD, these methods are generally used in a MLI which is in cascade configuration. Thus, an n-level inverter is an inverter with M-modules in series and the number of levels is calculated by the relation; **n = 2M + 1.**
The basic three schemes of level shifting in Multi-carrier modulation are:
1. In phase disposition (IPD): All carriers in phase.

2. Alternative phase opposition disposition (APOD): Opposite disposition of alternative carriers
3. Phase opposition disposition (POD): All carriers above zero reference are in phase and all carriers below zero reference are in opposition.
For calculating steps, first step i.e. at 1/40 instant: when S1 and S2 of common H-Bridge are ON
1/40 == 0.025
0.025= 25ms
1/25 = 0.04
And for the second step:
3/25 = 0.12

TABLE IV, SHOWS THE STEP VALUES OF THE PROPOSED TOPOLOGY

Step	**Values**	**Switches Conducting for particular instant**	**Vo**
1st	0.04	S7, S5, S3 and S1	0
2nd	0.12	S7, S5, S3, S2 and S1	1
3rd	0.20	S7, S5, S4 and S3	2
4th	0.28	S7, S5, S4, S3 and S1	3
5th	0.36	S7, S5, S4, S3, S2 and S1	4
6th	0.44	S7, S6 and S5	5
7th	0.52	S7,S6, S5 and S1	6
..			
40th	4.50	S8, S7, S6, S5, S4, S3 and S1	39
..			
78th	9.80	S7, S5, S4, S3 and S1	-3
79th	9.88	S7, S5, S4 and S3	-2
80th	9.96	S7, S5, S3, S2 and S1	-1

The patterns given in Table 5 are used to develop the switching states for negative, zero and positive voltages. The output obtained is by giving the gate pulses to the switches based on the pattern in Table V.

TABLE V. PROPOSED TOPOLOGY SWITCHING PATTERN

Switch S8	Switch S7	Switch S6	Switch S5	Switch S4	Switch S3	Switch S2	Switch S1	V0 *
0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	1	1	1
0	1	0	1	1	1	0	0	2
. .								
1	1	0	0	0	0	0	1	15
1	1	0	0	0	0	1	1	16

1	1	0	0	0	1	0	0	17
. .								. .
1	1	1	1	1	1	0	0	38
1	1	1	1	1	1	0	1	39
1	1	1	1	1	1	1	1	40

III. Simulation Results

A. Simplot Results

The topology which has been proposed is simulated and the circuit diagram is as given in Fig. 7. The simulation of single phase 81 level output with 4 DC sources and 4 switches has been carried out for 0.1 seconds. The circuit parameter details are shown in Table 1, Triggered Pulses to Common H-bridge Inverter (S3-S4 and S1-S2) are shown in Fig.7 and the output waveform across 10Ω load is shown in Fig. 8. The output voltage levels can clearly be seen in Fig. 9.

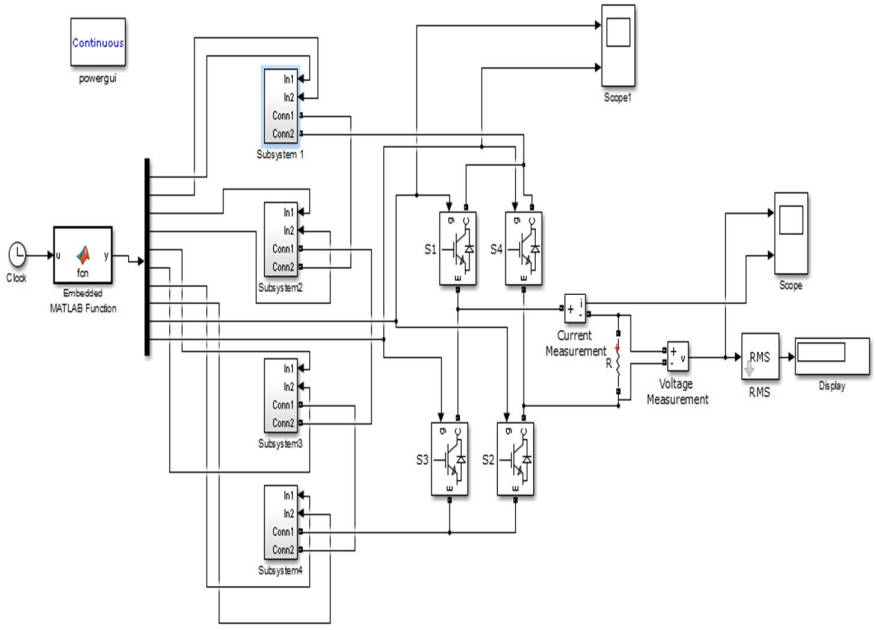
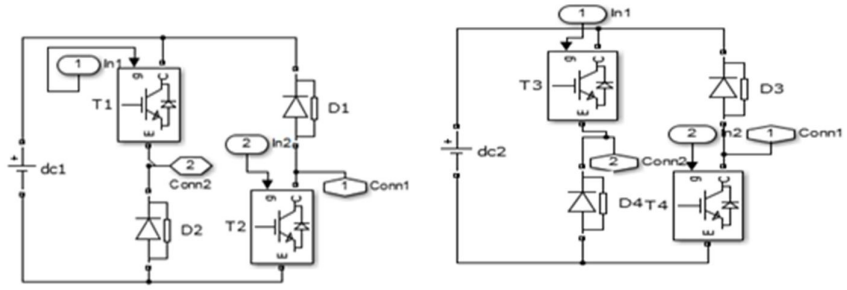
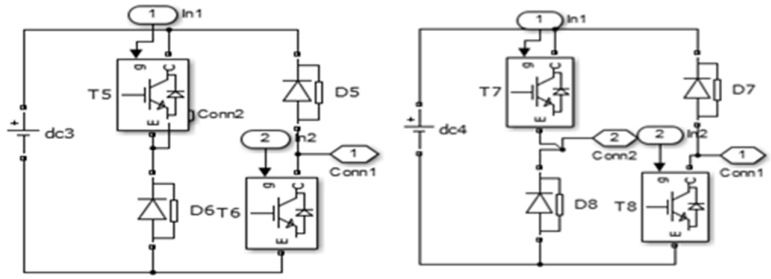


Fig. 5. Complete Simulated Circuit Diagram



(a) Subsystem 1 (b) Subsystem



(c) Subsystem 3 (d) Subsystem 4

Fig. 6 Subsystems for generating Gate Pulses (a) Subsystem 1 (b) Subsystem 2 (c) Subsystem 3 (d) Subsystem 4

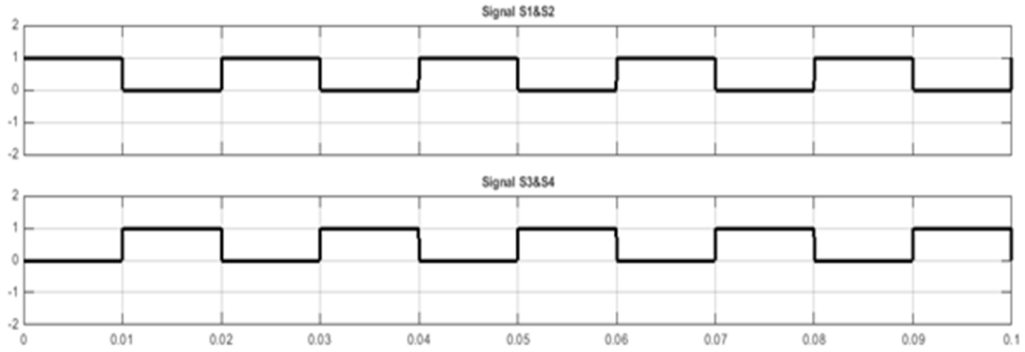


Fig. 7. Triggered Pulses to Common H-bridge Inverter(S3-S4 and S1-S2)

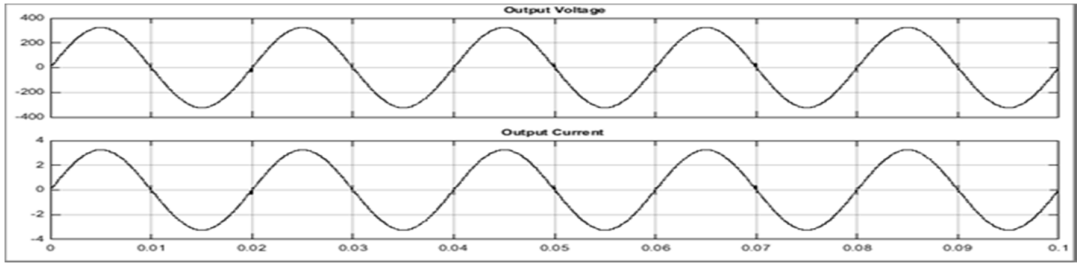


Fig. 8. Output Voltage and Current of Simulated 81 Level proposed MLI (With Resistive Load: R=10Ω)

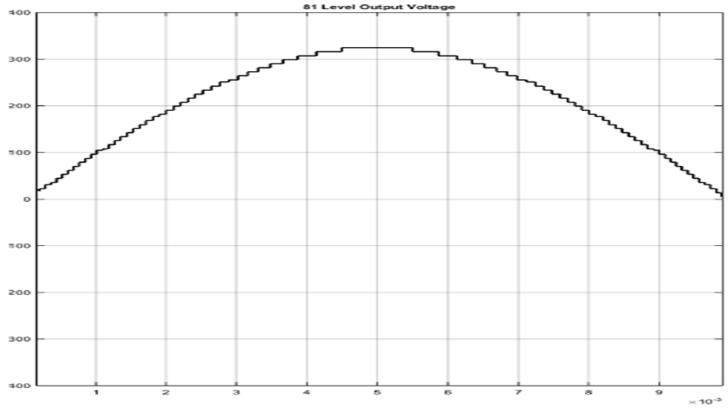


Fig. 9. Zoomed output showing Levels in voltage for Simulated 81 Level proposed MLI

B. FFT Analysis

To test the proposed topology, the load used was : R=10Ω. The steady state voltage & current output FFT are seen in Fig. 10.

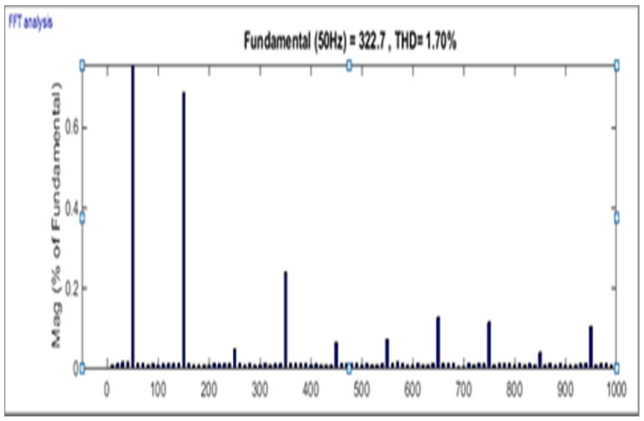


Fig. 10 THD of Output Voltage with Simulated 81 Level proposed MLI (With Resistive Load: R=10Ω)

IV. Comparison Of Existing and Proposed Model

The work attempted and reported in this paper differs from the other mentioned topologies where each module of H-bridge needs two switches and levels of voltage that can be added are only those which distribute the input voltage equally or in a binary pattern. The proposed method attempts to overcome this shortcoming by using trinary DC source distribution with dc voltage sources scaled by a factor of three. It has been seen that in this configuration maximum number of voltage levels are attained with a constant number of IGBTs. Using this scheme, addition or subtraction of the voltage level can be carried out allowing the input voltage to be distributed either equally, binary or in trinary pattern. Keeping the number of bridge units fixed, the levels of the output voltage levels can be increased while using the Asymmetric cascaded -inverter. The proposed technique employs the ACMLI with unequal DC sources with cascaded inverters. Low harmonic distortion is the outcome of the compounding voltage levels of the inverters which are in cascade configuration. The number of switches used are two and this topology avoids isolated voltage sources ensuring economic viability. The connection of the AC outputs of each level of the H bridge is done in series to enable synthesis of the multilevel waveform. This waveform is the result of the inverter outputs. Details of the circuit parameters are shown in Table 3 To highlight the differences in the proposed model, Table 5 compares the different topologies using no of switches, no of output voltage levels and no. of DC sources as a means of comparison.

Table V. Comparison of Topologies for output voltage levels

Topology	DC sources Distribution	No. of DC source	No. of switch	Output Voltage levels
Conventional Method	Trinary	n	4n	3^n
Existing Methodology	Binary (Trinary Not Possible)	n	2n+4	$2^{(n+1)}-1$
Proposed Method	Trinary	n	2n+4	3^n

The proposed topology shows a marked increase in the level of the voltage (output) even though number of DC sources are the same. This is a step towards getting a waveform close to a sinusoid, with decreased harmonic content.

V. CONCLUSION

The analysis of a large number of levels in a MLI has been done. In this work, the focus has been on decreasing the power transistors used for high levels (here 81 levels) coming up with a novel multilevel scheme for the multilevel Inverter. The topology suggested is a combination of ML modules and full-bridge converters. By increasing the number of levels of the voltage a marked improvement in the quality of the output voltage (low harmonic content) has been achieved. To highlight the benefits of this topology, it has been compared at every step while describing the methodology. The proposed topology can be optimally used to fulfil various objectives due to its design flexibility It has been seen that the circuit, consisting of MLMs with two switches, has a significant reduction in the number of switches for a fixed number of voltage levels. It has also been seen that the suggested topology gives 81 levels on the output voltage using 12 IGBT making it a good solution for high power quality applications or those that have a considerable number of dc voltage sources. The operation and performance of the proposed scheme has been done through MATLAB/Simulink and the harmonic spectrum has been shown in the FFT window. Merits of the proposed topology can be shortlisted as follows:

1) Use of Trinary sources (input) leading to an economically sound circuit configuration,
2) Ease of control in terms of voltage and power output due to the characteristic of modularity,
3) Suitability for high voltage applications as loss of switches are minimal due to low switching frequency and decreased EMI.

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