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Optimised DFT Architecture through Scan based Design

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***Abstract*—In this paper, an Optimized DFT architecture through Scan based design is proposed, where an efficient Low Power test pattern generator is used to verify any real time Design Under Test (DUT) module using Functional and Structural testing. The MUX based parallel data input Linear Shift Feedback Register along with gray code converter architecture reduces the initial latency in turn increasing the speed of architecture. Further, the generation of test patterns using characteristic equation optimizes the memory required and also minimizes the complexity of overall verification techniques in terms of hardware utilizations. The intended LFSR saves power by 14 % which is generated through SAIF file using synopsis tool and Tessent tool .DFT flow is adopted to do Scan insertion and ATPG and able to achieve fault coverage by 97% for one of the design chosen .it is compared withprevailing techniques to prove the efficiency in terms of Power utilizations and Fault Coverage.**

***Index Terms*— LPLFSR, Wallace tree Multiplier, DFT, ATPG, SAIF, Scan insertion, Stuck at fault.**

I. INTRODUCTION

Design for testability in VLSI is a design technique that makes testing a chip possible. In VLSI ,it is an extra hardware, where it is applied in the normal design, during the design process, which helps in its post-production testing.

The Built-In-Self Test (BIST) is one of the DFT approach, present within the chip itself . The random sequence test pattern, often known as LFSR, generates the test vectors. The LFSR is referred to the sequential logic circuits that were used to generate simulated binary numbers. A LFSR circuitry is made of n registers and response taps, defines state arrangement during most LFSR transitions. The taps for feedback are a modulo-2 polynomial can be used to explain it. A primitive polynomial is a polynomial that has no roots and generates the longest m-sequence possible, where the LFSR before repeating sequences, goes through the 2n-1 state.[1]. Here LFSR design is analysed through functional testing.

Functional testing focusses on testing all possible functional states, given the complexity of VLSI designs this is almost impossible because of the infinite possible combinations. Test vectors for functional testing focus on the entire system as a black box, without giving any consideration to the internal structure .Structural test makes no direct attempt to determine if theoverall functionality of the circuit is correct. Instead, it tries to make sure that the circuit has been assembled correctly from some low-level building blocks as specified in a structural netlist. The idea is that if the netlist is correct, and structural testing has confirmed the correct assembly of the circuit elements, then the circuit should be functioning correctly. Here Structural testing is adopted for Scan based design.

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Scan based technique, which modifies the internal sequential circuitry of the design . The goal of scan design is to make a difficult-to-test sequential circuit behave (during the testing process) like an easier-to-test combinational circuit. For ATPG,deterministic generation of patterns are used to cover stuck at faults.[3].

II. LITERATURE SURVEY

A. Previous BIST techniques

Mr.P.Moorthy, Ms.S.Saranya Bharathy[1] proposed an Efficient Test Pattern Generator for High Fault Coverage in Built-In- Self-Test Applications In this paper, a novel test pattern generator (TPG) for built-in-self-test is presented to attain the target fault coverage without increasing test length sequences. This proposed TPG method generates multiple patterns with single input change i.e., all vector applied to a scan chain is a single input change (SIC) vector.

Adeboye Stephen oyeniran et al., [4] were proposed concurrent mock-exhaustive testing of array multipliers with data- controlled segmentation. So this paper gives brief introduction of a new method for pseudo-exhaustive testing of standard array multipliers using a unique methodology of the data-controlled segmentation. The consistent structure of the test permits effective implementation of the method as both software based self-test (SBST) and hardware based BIST.

Shyamala et al., [10] proposed low power testable reversible combinational circuits. This paper affords information about low power revocable BIST test pattern producer which affords test vectors to condense switching activity for minimization of power through testing. A gated clock scheme is one of the low power BIST procedures was used to create the test patterns. So several fault models such as physical, stuck-at and missing gate faults are used to regulate the fault coverage. Higher fault coverage has realized for the circuits with gated clock scheme.

An analysis based on pertinence was proposed by Arbab alamgir et al., [6] in BTST application domain in which LFSR was streamed for hardware proficiency and elevated imperfection coverage. This paper presents modest, even and scalable parallel concatenation of LFSR to produce architecture for BIST applications. Accordingly aforementioned method condenses the bulky utilization of storage essentials in LFSR and the intended test design formation can be swapped over deterministic designs post satisfactory high error scope will be accomplished towards the primary levels of testing.

Akhila et al., [7] proposed design and accomplishment of performance efficiency in terms of power, logic BIST with high error scope by deploying Verilog. The authors designed and implemented performance efficient and high error scope BIST to check combinational logic. Therefore, the suggested LBIST pattern used to check combinational circuits accomplishes minor energy consumption reduction and complete error coverage. Maryam Rajabalipanah et al., [8] proposed contraction DFT hardware elevated by the use of a check micro-program in a micro-programmed hardware accelerator. This paper designates mechanism of testing micro-programmed accelerators of an embedded system. The consumption of the accelerator microinstruction to the test the data path and controller to projected process is called iMPAC. The outcomes showed that the structural level experiment is intended to test all conceivable paths of the data path, adding showed an online checking process for micro-program storage.

Jhanvi Ravi et al., [9] proposed trial logic infusion for optimization of testing frameworks on lower technology node. The structure DFT methodologies like examine approach, BIST, MBIST were implemented. In the recent days, DFT independently confront serious experiment as a result of node grading and it influences the compactness of the fabricated chip. Hence, manuscript hosts enhance the parameters on the 28nm technology node, like test time, test coverage and power dissipation. The results shows that the test points inclusion and ECO logic are used to get and enhanced data value of test parameter.

Hadi Jahanirad and Hanieh Karam [11] proposed BIST-based online test approach for SRAM-based FPGAs. Among the various test techniques, the BIST based approach has shown better performance. This paper briefly explains an effective online and non-concurrent technique has anticipated testing and identifying fault in FPGA. Trials showed that the test of SRAM cells has been done concurrently but the path testing has been done serially. The area overhead of the connected hardware has almost 50% but test process has been done very fast and without the need for reconfiguration of FPGA.

Jamuna Set al., [12] proposed design and implementation of BIST logic for ALU and FPGA. So this paper illustrates the reconfigurable BIST logic which perceives faults across the ALU block mapped on the FPGA. So basically BIST is a fault uncovering procedure that allows a circuit to test itself. The design is carried out using

VHDL and implementation on the ZED board with the help of Xilinx vivado. The design has tested for its functionality and code coverage using Questasim simulation.
Siyun chen et al., [13] proposed BISTlock: efficient IP piracy protection using BIST. So this work comprises a logic- locking method that operates BIST to isolate practical inputs when the circuit is locked. Also a set of security metrics and use the projected metrics to quantify BISTlock's security strength for an open-source AES core. Trials showed that BISTlock quantifiably secure impressive nominal overhead. Most importantly, BISTlock looks afar the prevailing logic-locking standard and opens up a new direction for logic locking for input isolation. Yousuke Miyake et al., [14] proposed on-chip delay measurement for in-field test of FPGAs. The proposed work comprises several timing generation using an embedded PLL, BIST-based interruption measurement and correction of the measured interruption with reflecting temperature modification in field. The projected method infers that an alteration of the performance during VLSI operation can be perceived by iterative interruption measurement. Further the trials inveterate that an effect of temperature for the measured interruption can be corrected by merging with temperature measurement.
G. Bhavani, K. Jamal and B.Veera Reddy [15] proposed weighted pseudorandom based deterministic BIST for fault testing and self-healing. The projected work comprises self-healing method of scan design that is performed among two stageclocks for vital scan cell test way and faulty scan cell way to pseudorandom pattern generation and deterministic BIST application to upsurge the fault coverage. The trials showed that the projected method has two clocking stages to synchronize error originated data with error corrected data. Author Dr.Sabir [23] proposed low power multiplexer lfsr design for IOT devices and analysed results in terms area,power and time parameters.

A. Existing Scan logic and ATPG methods

Seongmoon Wang[2] proposed an generation of Low Power Dissipation and High Fault Coverage Patterns for Scan-BasedBIST The proposed BIST decreases the number of transitions that occur at scan inputs during scan shift operations and hence decreases switching activity during BIST. The proposed BIST is comprised of two TPGs: LT-RTPG and 3-weight WRBIST TPG .
Authors have et al., [3] implemented scan logic on RTL design peed analysis, difficulties and remedies for 56 Gbps as well 112 Gbps PAM4 SerDes. Consequently, developing DFT for greater performance in terms of speed edge of a appliance familiarizes the age-old difficult of performance degradation due to addition of extra circuitry.
Capture-per-clock hybrid assay detail was proposed by Elham Moghaddam et al., [5] in which logic of BIST was discussed. Here, in this paper detail description of composite examine point knowledge designed to condense deterministic pattern counts and to advance fault recognition probability by means of the similar nominal set of test points. Hence, recent structure corresponds to the mixture of assumed arbitrary trial patterns brought in a test-per-clock fashion through conservative scan chains and per-cycle-driven hybrid remark test points that capture faulty things every shift cycle into enthusiastic scan chains. So by detecting trials on the proposed scheme, industrial designs confirm practicability were reported.

III. MOTIVATION

Firstly, it is difficult to ensure the durability, dependability, and testability of multi-million transistor based VLSI designs.Secondly, In volume production of ICs, faulty chips leads to huge financial losses. This motivated to take up this work.

IV. PROBLEM STATEMENT

The existing techniques used for different types of functional testing and structural testing for fault detection are not very effective in terms of different parameters such as Power, Fault coverage with reduced patterns, which are needed to address for proper working of digital integrated circuits. In this paper, these issues are addressed.

V. PROPOSED ARCHITECTURE

The Proposed optimized BIST architecture is shown in Figure 1, in which the advanced multiplier architecture and 16 bit shift register are used as Design Under Test (DUT).

In the Proposed system, the low power LFSR block is used to generate pseudo random number based on some predefined polynomial equation along with gray code converter , which are then fed as input to the DUT block. As an example, Wallace tree Multiplier is chosen as DUT block. The DUT block performs multiplication of the two input numbers and mainly the non-equal inputs (a≠b) are stored in the ROM block and accessed through the counter output. Finally both the output sequences of multiplier block and stored ROM data are compared in the compare block.

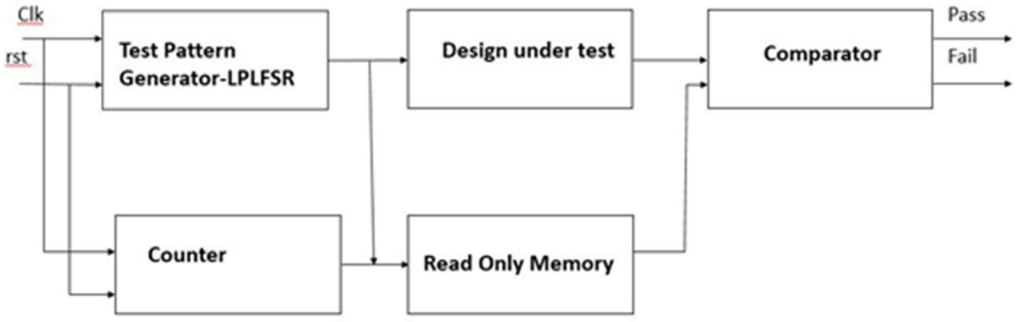

Figure 1: Proposed DFT Architecture

A. Test Pattern Generator

The test pattern generator block produces test vectors which will be used to test the circuit by serving the essential test vector to the design. Generally, PRSG or LFSR is used in this instance which produces pseudo-random patterns based on the feedback polynomial. So, it is the sub-module of the shift register where the particular bits are known as taps which are XORed to make the feedback polynomial later this will be provided to LFSR for LSB of the flip-flop. Galois filed is used as the basic model for LFSR. Modulo 2 is the basic arithmetic procedure for LFSR where the multiplication corresponds to an operation and addition is corresponds to the XOR operation. Bits shifting from one flip-flop to another flip-flop created pseudo-random patterns in the PRSG. Figure 2 shows the proposed architecture of Low power LFSR.

The characteristic polynomial is described by the n-bit LFSR's internal structure by using a characteristic polynomial of the degree n above GF(2) is given by

$$y(x).=1+x^5+x^9+x^{10}+x^{15} \qquad ($$

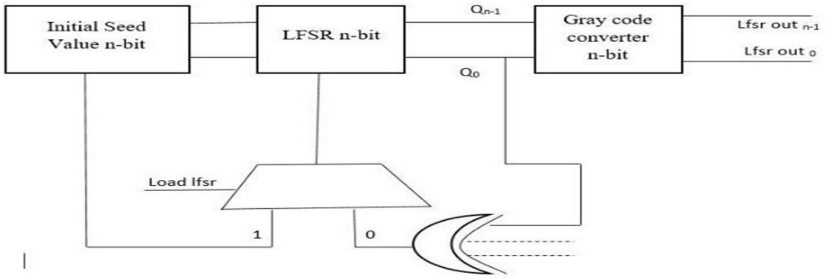

Figure 2. Proposed Low power LFSR

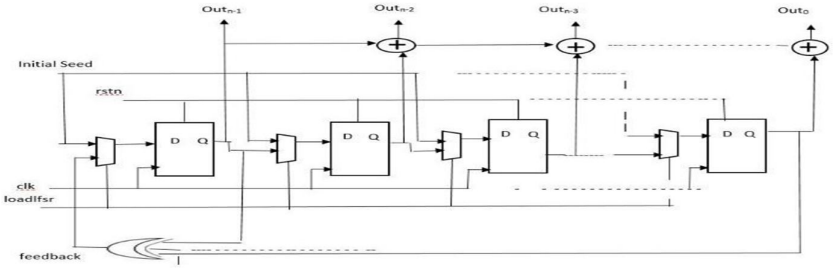

Figure 3. Internal structure of Low power LFSR

The polynomials are considered primitive polynomials if the polynomials cover the extreme length. The proposed PRSG is developed by using polynomials which are realized by using Galois to minimize the delay of the critical path for 16- bits as shown in equation (1). The tapped bits are denoted as powers of the x terms and input to the first flip-flop will be denoted as term one. So these created polynomials are served to the projected LFSR at logic BIST request. Fibonacci kind LFSR has a large critical delay because of external feedback. Galois LFSR has been used in our design which helps to reduce the critical path delay because of internal feedback. The flip-flop output is fed to gray code converter to reduce the number of transitions inturn switching activity is reduced, which is fed as LFSR outputs ,then these outputs are separated into two parts which are used as input to the Design Under Test block.

B. Design Under Test

The low power LFSR patterns are applied for combinational and sequential design. The Wallace tree multiplier and 16 bit shift register designs are taken as combinational and sequential circuit designs under test to check the performance of theproposed test method.

C. ROM

It is a memory module used to store all the probable input of the predicted signature of the appropriately designed circuit under test. These values are pre-calculated by the simulations. The test results of the architecture will be developed based on these signature values. Basically, for testing purposes golden signature is used. Meanwhile, this is hardware-level testing, so in any situation, the data that exists in the memory should not be obligated or altered. As a result, the ROM architecture is used. The ROM array is used to store the appropriate signature. The ROM array is read by the address created by the counter block to get values of the appropriate signature.To reduce the ROM, the redundant of input signals are eliminated by MUX block.

D. Comparator

It is used to compare the ROM and Design Under Test block's output depending on whether the particular number is equal, larger, or smaller. The golden signature is kept in the ROM and the result and signature from Design Under Test block will becompared. The progress of the circuit is finalized depending on the result. The circuit will be considered fault-free if the both golden signature and created signature by the Design Under Test block are equivalent or else the circuit will be considered as faulty. The Counter architecture is used as Comparator in this case.

VI. RESULTS AND DISCUSSIONS

A. Implementation

1.Functional Testing

Here low power LFSR patterns are applied for DUT As an example Wallace tree multiplier and 16 bit shift register designs are chosen ,then the outputs of DUT is compared with golden patterns stored in ROM .All patterns are passed as it is done forfault free design through functional simulation.

1.1.Steps to compute power for LFSR pattern generation

1.Firstly from RTL design, VCD file is generated, it is an ascii based format for dump files generated by EDA tool2.VCD is converted into SAIF file which gives switching activity using synopsis tool.

3.Synthesis is done in synopsis tool by reading SAIF file to generate power report and where power is reduced to 14%compared to normal 16 bit LFSR which is tabulated below.

TABLE I. POWER UTILIZATION

Parameters	Power(mw)
Normal LFSR	0.3707
Proposed LP LFSR	0.3174
Proposed OptimisedDFT architecture	0.70

2.Structural Testing

To inject stuck at faults Structural testing is adopted. The flow for structural testing using tessent tool is shown in fig. 4.

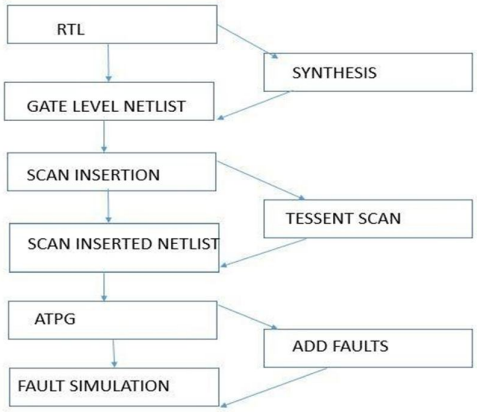

Figure.4 Tessent tool DFT flow

RTL Design is synthesized using synopsis tool with 28nm technology to get gate level netlist. Then netlist is taken as input for scan insertion for one of the proposed design with 5 scan chains using tessent tool. The scan inserted netlist which is obtained as output has 26 scan cells in scan chains with 31 memory elements and longest scan chain has 6 scan cells .Then ATPG is done which reports stuck at faults and generates serial and parallel patterns .The fault statistics is reported in the table.

RTL of proposed architecture and low power LFSR design is shown in fig 5 and 6,which gives internal structure of thedesign.

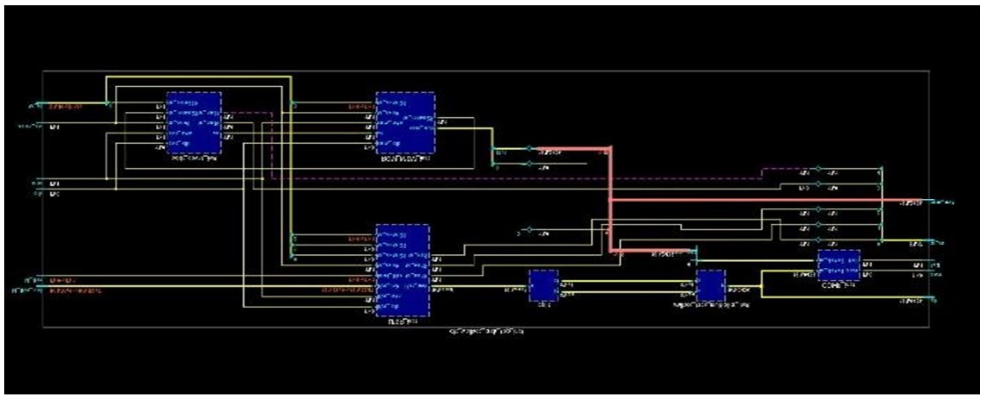

Figure 5. RTL Schematic of Scan inserted Proposed DFT Architecture

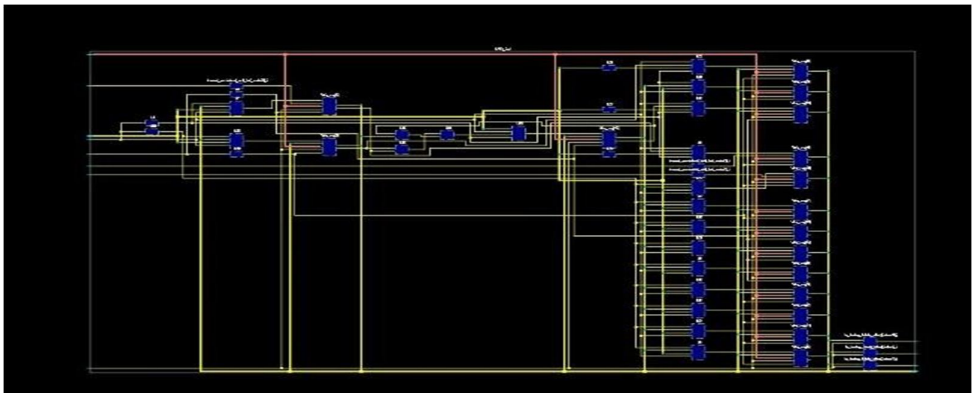

Figure 6.RTL schematic of Scan inserted Proposed LFSR

B. Simulation Results

Figure 7 shows the fault simulation result of the Proposed architecture. As 5 scan chains are inserted ,there are 5 scan inputsand 5 scan scan outputs which is depicted in figure.Here Serial pattern simulation is done to detect stuck at faults.

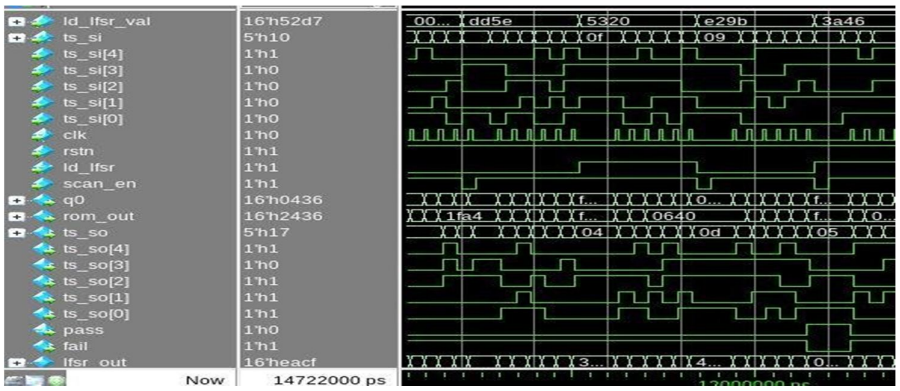

Figure 7.Fault simulation for proposed Architecture

Figure .8 Low power LFSR patterns

Figure 9 shows the cycle count and Pattern count simulation. Here 368 cycles and 44 test patterns are appliedto the design. Internal scan uses two states for Internal modification of the design circuitry to increase testability. The two states are shift and launch when scan enable is low, data is launched into scan cells. When scan enable is high, scan chain is loaded and shifting of the data happens. This is depicted in the figure.9 below.

Figure.9 Cycle count and Pattern count simulation

Figure 10 shows the statistics report of faults, where Formula for Calculating Test coverage and Faults coverage is given below

a) Test coverage = Detectable faults/total number of testable faults
b) Faults Coverage = Detectable Faults/total of faults in the design
c) Total number of testable faults = Total number of faults − (RE + UU+ BL + TI)

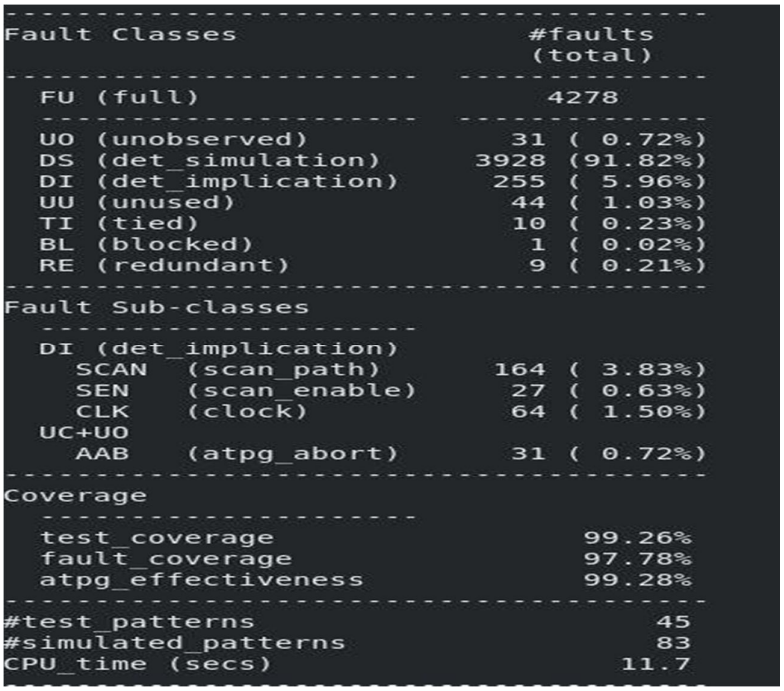

Figure 10. Statistics report of stuck at faults

Fault coverage Report table for DUTs

TABLE II. FAULT COVERAGE REPORT

Sl.No	Design under test	Fault Coverage
1	16bit shift Register	80%
2	Wallace Tree Multiplier	97%

TABLE III. COMPARISON TABLE

Sl.no	Parameters	[1]TPG	[23]LPLFSR	Proposed LPLFSR
1	Power	33.64mW	107mW	0.3174mW
2.	Fault Coverage	70%	-	97%

C. Comparison and Justification of the results

From Comparison Table .3, the proposed method is able reduce power by 33.32 % using functional testing and increase fault coverage by 27% using structural testing compared to reference [1]. Hence it is justified as Efficient Lowpower DFT architecture through scan based design.

VII. CONCLUSION

In this paper, it's been able to design low power test pattern generator for any design under test. The proposed Low power patterns are applied for optimized design and performed functional testing, in which the Wallace tree multiplier, 16 bit shift register are used as test case. The parallel implementation of the low power LFSR block reduces switching activity in turn reduces power by 14 % and the MUX based test case reduction technique reduces the overall decision time and Structural testing is performed to inject stuck at faults through Scan based

design to achieve high fault coverage. In future, Scan Compression Techniques can be evolved in proposed architecture to reduce scan chain count and test time.

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