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A Study of Approximate Arithmetic Circuit Designs for Digital Signal Processing Systems

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***Abstract*—Approximate computing has gained significant attention as a promising strategy for digital signal and image processing applications. This article reviews the relevant research aimed at development of approximate arithmetic circuits and provides an overview of their performance in digital signal processing systems. The incessantly growing demand for compactness and speed in portable multimedia devices and embedded systems, continues to drive the need for novel approximation techniques. This review research paper is aimed at serving as a guideline for further research on inexact computing.**

***Index Terms*— Approximate circuits, energy efficiency, compactness, delay reduction, multipliers, inexact adders.**

I. INTRODUCTION

An increase in the role of multimedia devices in daily lives has made improvement in: energy-efficiency, compactness and faster computation; a key objective in VLSI research. Integrated circuit advancement through technology scaling has shown significant performance gains through continuously shrinking the size of CMOS. However, CMOS shrinking has doubled the number of transistors on a chip (driving Moore's law to its limit), leading to increased complexity in nanoscale technology along with an increase in process-voltage–temperature (PVT) variations, and poor threshold voltage scaling.

Fortunately, major application domains of embedded electronic devices, for example, digital signal processing (DSP), data analytics, and data mining are inherently tolerant to a certain degree of noise. Leveraging the inherent error tolerance, approximate computing induces an acceptable amount of error in exchange for a simpler circuit and lower power dissipation.

Approximate computing is applicable at different levels of abstraction from the hardware level to algorithm synthesis at the software level. In this paper, we have discussed various approximation techniques that optimize the hardware level of abstraction. The probabilistic CMOS (PCMOS) was one of the first approaches to trade-off computation for power efficiency [1], it proved to be applicable only when the power supply voltage is reduced to the noise level.

Another potential approximation technique is voltage over-scaling (VOS), requires additional hardware e.g., error recovery circuitry and additional voltage domains, approaches that modify the functionality of the circuit to implement approximation were introduced, wherein arithmetic units e.g., adders and multipliers (most power-

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consuming units in DSP systems for image and video processing) proved to be the best targets.
The most commonly used techniques for the development of approximate arithmetic circuits include bit width truncation, circuit simplification through truth table alteration [2], partial product approximation [3], and integration of new number representation formats in the implementation of arithmetic circuits [4].
Approximate circuits can be assessed based on the figures of merit discussed in [5] and peak signal-to-noise ratio (PSNR: measures output quality of decoded image) generated on application of the circuits, to get a better understanding of probabilistic circuit performance.

II. Reviews of the Techniques Discussed

A. Approximate Radix-8 Booth Technique

Jiang et al. [6] reduced the computation time of an accurate radix-8 booth multiplier by employing a novel 2-bit adder to calculate least significant bits (LSBs) of a recoding adder, eliminating the carry propagation in calculation of a triple multiplicand.
A novel recoding adder is designed for 16-bit booth multiplier. Fig. 1 shows the circuit for the proposed approximate recoding adder, constructed using 4 proposed 2-bit adders and a 7-bit exact adder.
The pass rate of the proposed approximate adder is 31.64%.
ABM1 and ABM2 are the two proposed signed 16 x 16-bit approximation radix booth multipliers. They show 20% and 44% lower computation time compared to an exact radix-8 booth multiplier. The approximation multiplier is 31% quicker and occupies 43% less circuit space.

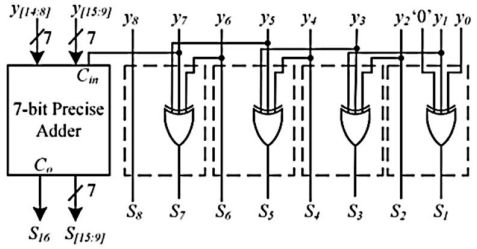

Figure 1. Approximate recoding adder with 8 approximate bits [6]

B. Novel Approximate Compressor-Based Multipliers

Reference [7] proposes an approximate compressor design for design of energy efficient inexact multipliers. Performance testing indicated that their manufactured circuits outperform the prior suggested approximation multipliers in terms of error electrical performance.
The proposed approximate compressors (depicted in Fig. 2) contain j inputs p_0, p_1, and p_{j-1} and assess [j/2] outputs through a novel approach, with the goal of lowering the chance of inaccuracy and the mean error. Adaptive filter using approximate compressor provide 4% and 24% system level power saving respectively. The suggested approach outperforms earlier approaches which used simplifying of partial product matrix using 2x2 multipliers.

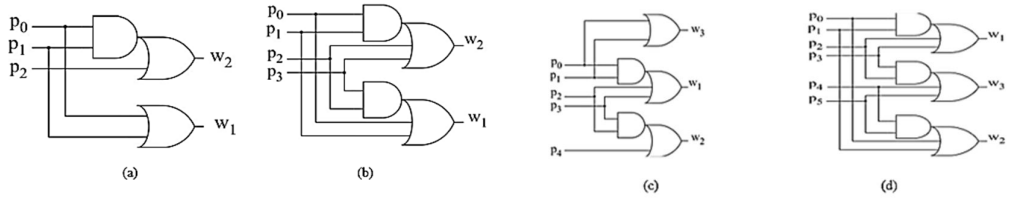

Figure 2. Schematic of proposed approximate (a) 3/2 compressor (b) 4/2 compressor (c) 5/3 compressor (d) 6/3 compressor [7]

C. Approximate Hybrid High Radix Encoding Method

The suggested approach [8] encapsulates the multiplicand's most important bits (MSBs) using radix-4 encoding, while the k LSBs with radix-2k (having $k > 4$). However, to reduce the extra intricacy prompted by composite computing, a circuit enabling partial products is approximated.

Suggested method is adaptable to any multiplier design and may be reconfigured. Compared to an accurate Multiplier, the suggested approach saves up to 50% energy and reduces area by 0.93%. It outperforms in terms of energy usage and inaccuracy.
Eventually, its effect on inexact 16-bit hardware multipliers is specified, and a qualitative study is performed to estimate possible area benefits.

D. Hierarchical Seeding Approach for Design of Energy Efficient Approximate Circuits

Reference [9] presents two major concepts, the first of which is a hierarchical Seeding Approach for creating fundamental population development without the need of pre-evolutionary procedures. To simplify matters, the following concept is statistical and relates to offline pre-evolution forecasts.
The goal of recurrent approximate design is to lessen ambiguity in the design. Minimizing a system's chip size is a crucial factor for small and embedded system design. These systems are anticipated to make the most of their multimedia tacks' varied algorithms and designs.

E. Novel Reverse Carry Propagate Full Adder (RCPFA)

Reference [10] presents 3 novel designs of reverse carry propagate full adder (RCPFA) each having different accuracy level, power consumption, and delay. Pashaeifar et al. proposes a hybrid adder with tunable accuracy designed using an accurate carry adder and the proposed inexact RCPFA cells.
The first proposed architecture is a blended design adder, which has 2 distinct sections, accurate MSB and LSBs. The issue seems to be in exact most significant bit segment's carry input and simulation in the LSB segment for high-performance DSPs.
Fig. 3 shows the difference in quality of JPEG compression image outputs for discrete cosine transform (DCT) circuits constructed using: exact adder cells, RCPFA proposed adder cells, approximate mirror adder (AMA-I) (proposed by Gupta et al.), transmission gate based approximate adders (TGA-I) (proposed by Yang et al.), and lower-part OR adders (LOA), respectively.
In the least desirable situation, the carry propagation adder's delay is: $n \times t_{CP}$, where 'n' is the bit width of the adder. A little delay violation results in a large error beholding error phenomenon on summing MSBs.
Concepts of RCPFAs are employed in hybrid adders with RCPFA-based general n-bit structures. Results show that approximation FAs save 60 percent and 39 percent of energy in DCT of JPEG and FIR further applications, respectively.

Figure 3. Output images for DCT circuits using different FAs [10]

F. TOSAM Truncation Technique

An approximation approach [11] is designed to decrease the partial products. The input values are trimmed to '*t*' and '*h*' bits in proposed approximation method depending on the location of the leading to one bit. The suggested multiplier involves less complicated calculations and spends less energy than the precise multiplier. Fig. 4 depicts the proposed signed approximation multiplier's block diagram.

TABLE I. MARE AND VARE OF SUGGESTED MULTIPLIERS WITH VARYING WIDTHS AND 'H' AND 'T' VALUES [11]

TOSAM Architecture (*h*, *t*)	8 – bit		16-bit		32-bit	
	MARE (%)	VARE (%)	MARE (%)	VARE (%)	MARE (%)	VARE (%)
(0,2)	10.12	43.73	10.91	46.55	10.9	46.63
(0,3)	7.66	28.23	7.6	28.78	7.61	28.81
(1,5)	4.06	8.38	3.95	7.61	3.95	7.6
(2,6)	2.11	2.29	2.06	2	2.06	2
(3,7)	1.12	0.65	1.05	0.51	1.05	0.52
(4,8)	0.62	0.2	0.53	0.13	0.53	0.13
(5,9)	0.37	0.06	0.26	0.03	0.27	0.03

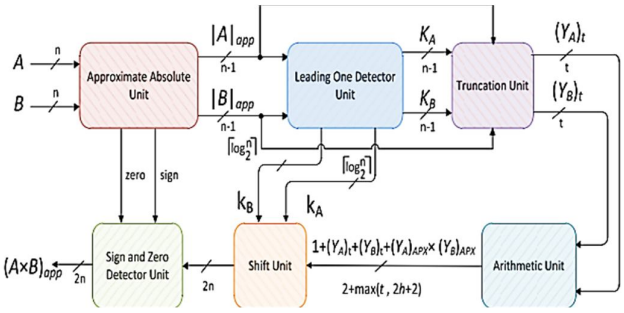

Figure 4. Proposed signed multiplier as a block diagram [11]

As shown in the Table I, the arithmetic units of 8-bit, 16-bit, and 32-bit TOSAM structures have stable '*h*' and '*t*' with almost equal Mean Absolute Relative Error (MARE) and Variance Absolute Relative Error (VARE). On average, the proposed 32-bit multiplier reduced energy consumption by 95% as compared to the identical Wallace multiplier and took up 85% less space. The suggested multiplier outperforms in classification applications as well as image processing due to its high accuracy.

G. Truncation Based Inexact Multiplier: LETAM

Vahdat et al. designed LETAM: Low Energy Truncation-based Approximate Multiplier. LETAM maintains a fixed core, independent of input bit width, by scaling down n-bit addition and multiplication operations by truncating the intermediate results to smaller bit length, before using them in final output calculation.
Fig. 5 illustrates the block diagram of the proposed architecture.
Reference [12] also designed an adjustable output quality multiplier (AQ-LETAM), that utilizes reconfigurable units (quality selectors/ decoders), allowing the user to tune the approximation level according to precision requirements and input characteristics.
Study of error distributions for different truncation lengths (LETAM (*t*=4, 6, 8, 10)); reveal that the relative error of the proposed design is almost always less than 5%. The proposed multiplier has 58.2% lower average relative error (ARE) compared to Dynamic Segment Method (DSM) of approximate multiplication.
Compared to the Wallace Tree multiplier, LETAM reduces the EDP, delay and area, on an average by 11.98%,74.77%, and 89.44% respectively. LETAM outperforms DSM and DRUM (dynamic range unbiased multiplier) architectures at higher accuracy levels (*t*=6,8,10). The best and worst outputs for power reduction in LETAM are 87.9% and 78.8% respectively, compared to exact techniques [12].
Due to additional enable/ disable logics for quality selection, AQ-LETAM has a higher delay than the LETAM. LETAM and AQ-LETAM are superior to the precise Baugh-Wooley multiplier, at all accuracy levels. The AQ-LETAM and LETAM offer 84% lesser energy consumption and 85% smaller EDP than the Baugh-Wooley multiplier. Compared to exact architecture, JPEG encoder made using LETAM observed a maximum 0.15 dB decrease in PSNR, with some cases showing PSNR reduction.

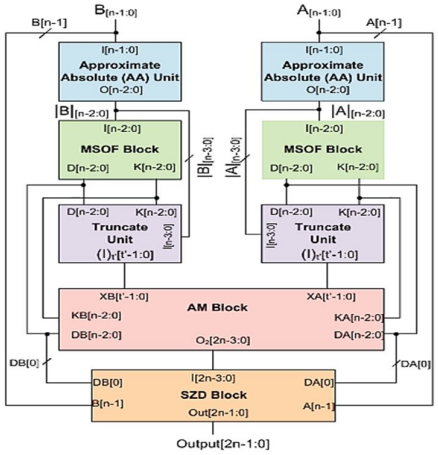

Figure 5. LETAM architecture [12]

H. Energy-Efficient Image Processing Using CNFET-Based Imprecise Ternary Adders

Panahi et. al. [13] proposed two inexact CNFET- based approximate ternary adder cells that require fewer transistors, tested to exhibit reduced delay and power consumption, improved noise immunity, and reduced sensitivity to process compared to precise adders. The proposed designs use switching theory for implementation of ternary logic and leverage the unique properties of CNFETs. The proposed adder

The designs constitute an exact C_{out} generator, using CNT pass transistors as shown in Fig. 6, while the Sum output is chosen to trade off accuracy for power consumption.

The first design of the proposed imprecise Sum trit generator circuit (Fig. 7), constitutes 2 cascaded ternary half adders and generates six false results in the output. Design 1 has higher propagation delay and power consumption compared to Sum generated from a full adder. The second proposed design (Fig. 8) outputs a false Sum for seven input combinations. The PSNR values for DSP systems designed using these designs range between 36dB and 40dB, which is an acceptable accuracy in most image processing applications.

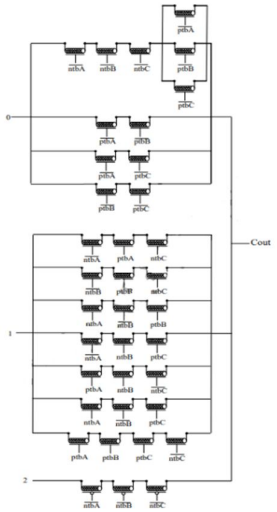

Figure 6. Ternary C_{out} generator circuit for both proposed designs [13]

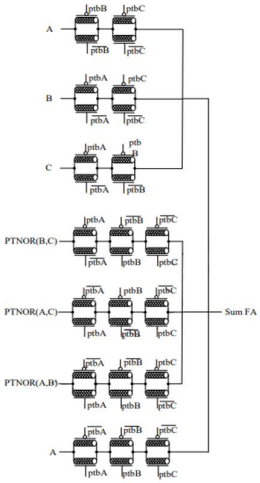

Figure 7. Sum trit generator circuitry for Design 1 a) block diagram b) transistor level scheme [13]

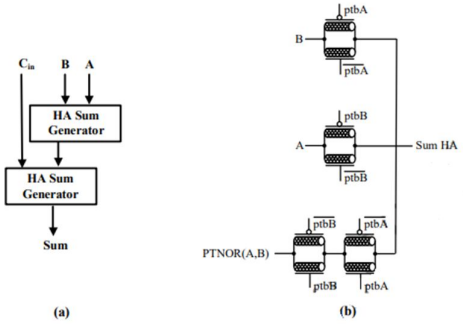

Figure 8. Sum generator circuit for Design 2 [13]

I. Majority Technique for Efficient Approximate Image Multiplication

Sabetzah et al. designed an inexact 4:2 compressor using a single majority gate, and applied it in the architecture of an 8-bit Dadda multiplier, to reduce density and complexity of nano scale digital circuits.

All circuits in [14] are designed using FinFETs. The proposed 4:2 compressor design (Fig.9) has only 12 transistors; none of the generated false outputs have greater than 1 error distance.

Application of majority logic in partial product reduction allows the multiplier circuit to be reduced into simple AND, OR, XNOR, and NOT logic gates, with lesser transistors leading to reduced circuit complexity and lower delay.

The proposed architecture requires smaller area, reduces the number of transistors by 31% (compared to other compressor-based designs), maintains acceptable PSNR values, and improves delay, power consumption and PDP. The proposed structure has the added advantage of being the perfect fit for majority friendly emerging technologies like Quantum dot Cellular Automata (QCA) and Single Electron Transistor (SET).

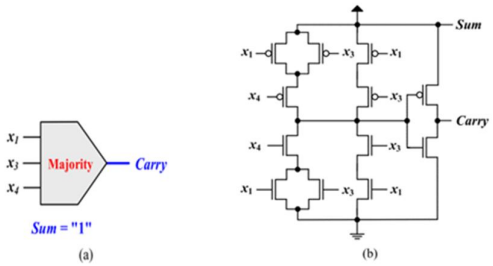

Figure 9. Proposed inexact 4:2 compressor a) Majority Gate b) Circuit design [14]

J. Approximate Adder Circuits for Low-Power Digital Signal Processing

Gupta et al. [15] explored the possibility of reducing complexity at the transistor level, and designed 5 approximate Full Adder (FA) circuits (as shown in Fig. 10-13) that tested up to 69% power savings compared to accurate adders. The proposed mirror adder (MA) has lower dynamic power dissipation and lower area (max. proposed area in approximation 1= 29.31μm2) compared to conventional FA cell(40.66μm2) due to reduced number of transistors. Use of approximate FA cells to create ripple carry adders (RCAs) in a multilevel adder tree, lead to reduction in load capacitance, reduced propagation delay, and lower operating voltage, compared to conventional RCA adder tree.

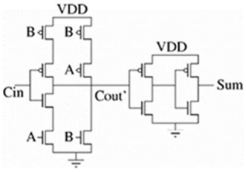

Figure 10. Approximation 3 [15]

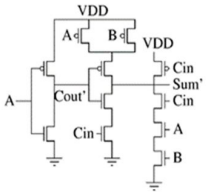

Figure 11. Approximation 4 [15]

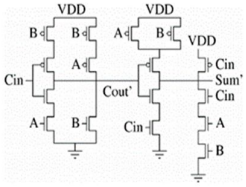

Figure 12. Approximation 1 [15].

Performance analysis of image compression systems employing the inexact cells for 7-9LSBs revealed that truncation offers better power savings (61%) compared to the proposed technique at the cost of huge PSNR value (25.46 dB), while approximation 5 provides the best PSNR (13.87 dB) and power savings (60%) amongst all proposed approximations.

MPEG encoder architecture employing the proposed technique revealed to fare better than truncation-based MPEG as the number of approximate LSBs was increased. The proposed approximation has lower probability of error compared to truncation, as the number of approximate LSBs is increased.

The proposed imprecise adder can be used along with other existing low-power technologies, such as significance-driven calculation (SDC) and algorithm noise tolerance (ANT), to extract multi-fold benefits with a very minimal loss in output quality [15].

K. Use of Adiabatic Logic to Design Energy Efficient Approximate Multipliers

Giridhar Reddy et al. [16] attempted to further reduce power consumption in approximate circuits by employing ECRL adiabatic logic instead of CMOS logic, to the imprecise multiplier circuit.

8-bit accurate array multipliers designed using CMOS, and ECRL logic were compared to approximate array multipliers designed using CMOS, and ECRL adiabatic logic. Results revealed that the ECRL logic offered 58.79% power savings compared to CMOS in approximate multipliers and 58.84% power savings when applied to accurate multipliers. The proposed architecture is ideal for applications in portable devices where power savings are a significant factor.

L. Imprecise Multiplier Design for Power and Area Efficiency

Venkatachalam et al. reduced power consumption in multipliers by applying approximation in the partial product stage of binary multiplication operation.

The proposed approximation technique alters and then reduces the partial product (PP) matrix in an 8-bit inexact multiplier using, OR gates, and the proposed inexact half adder (HA), full adder (FA), and 4:2 compressor.
Reference [17] proposes 2 models of multipliers using the proposed approximation. Multiplier 1 (approximation in all columns of a n-bit multiplier's PP matrix) offers 87% area power product (APP) savings and Multiplier 2 (approximation in n-1 lease significant columns of a n-bit multiplier's PP matrix) offers 58% APP savings, compared to an exact Dadda multiplier.
Reference [17] compared the proposed multiplier designs with an exact Dadda multiplier, Momeni's approximate compressor-based multipliers (ACM1 and ACM2), multiplier based on static segment method of approximation (SSM), partial product perforation technique of approximation (PPP), and under designed multiplier (UDM) by Kulkarni et al. Analysis revealed that Multiplier 1 is suitable for providing ideal power savings but requires high error tolerance, while Multiplier 2 offers the best accuracy along with moderate energy efficiency.

M. Probabilistic Prediction of Partial Products for Design of Fixed Width Booth Multipliers (FWBM)

Yajuan He et al. proposed a FWBM design. Similar to all FWBMs, the proposed technique modifies the PP array through dedicated partitioning, but the proposed method further partitions the truncated part of the PP array as illustrated in Fig. 14.
The proposed FWBM architecture (Fig. 15) comprises: Booth encoder and partial product generator (BEPPG block), a compression tree system, and a carry propagation adder (CPA) for final product generation [18].
The method reduces the area-energy-delay-error product by 27% compared to other booth multipliers (including: post truncated BM, direct truncated BM, multilevel conditional probability-based BM, probabilistic estimation bias-based BM, Jou et al.'s BM, sign-digit-based conditional probability estimation BM), at different operand lengths.
In DCT applications, compared to the direct truncation method, the proposed multiplier showed a 16.76 dB gain in PSNR, while the area loss is only 15%. Reference [18] reduces the area cost by 30% and lowers power consumption by 28% with a 3.61 dB precision loss compared to post truncation technique.

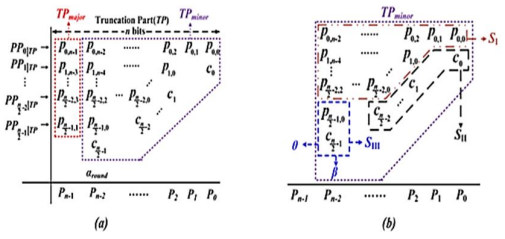

Figure 13. Truncation Part (TP) array partitioning [18]

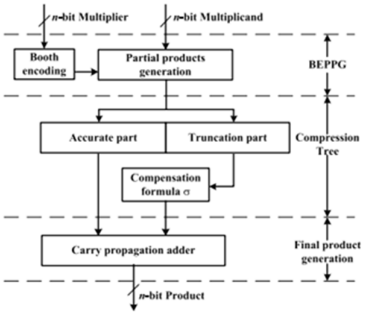

Figure 14. Block diagram for proposed FWBM [18]

N. Carry Skip Technique Using Neuromorphic Computing

Kim et al. employed a carry prediction technique that uses information from the least significant bits to implement parallel carry speculation. Fig. 16 shows design for the proposed adder using carry technique. Fig.17 illustrates the block diagram for the n-bit approximate comparator designed by implementing subtraction using the proposed scheme.
The proposed adder is 2.4 times faster than the traditional adder and increases energy efficiency by 43%. The proposed comparator offers up to 71% energy savings compared to the traditional adder. The imprecise units proposed by Kim et al. are ideal for neuromorphic computing since they are 3.11 times more energy efficient than the exact adders and comparators in performing leaky integrate-and-fire operation with scaled up voltages [19].

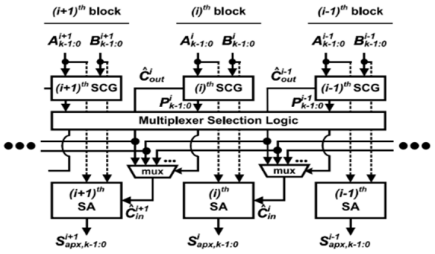

Figure 15. Proposed inexact comparator block diagram [19]

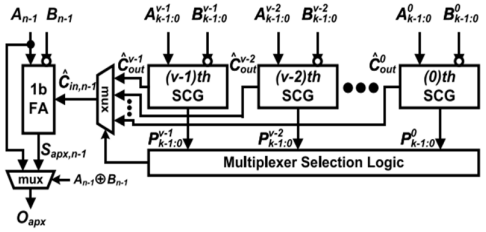

Figure 16. Proposed inexact adder block diagram [19]

O. Truncation Algorithm Based Adders and Multipliers

The proposed adder design [20] involves splitting the input operands into accurate (designed using RCA, carry-skip adder (CSK), carry-select adder (CSL), or carry-look-ahead adder (CLA)) and inaccurate (carry-free addition and control blocks) parts.

As the carry propagation can consume an unwanted part of power consumption, it can be excluded from addition of inaccurate parts. Hence, a large part of both energy efficiency and power consumption can be improved. The PDP of ETA is noted to be 66.29%, 77.44%, 83.70% and 75.21% better than RCA, CSK, CLA, and CSL, respectively.

P. Rounding Based Approximate Multipliers

R. Zendegami et al. [21] proposed a rounding-based high-speed approximate multiplier for both signed (Fig. 18) and unsigned multiplications. The multiplier was based particularly on characterized rounding of the input in the form of 2*n*. Three approximate multipliers' hardware implementation were conferred in this paper. Upon comparing them with some accurate and approximate multipliers, it was exhibited that the proposed architectures were more efficient than the approximate multipliers.

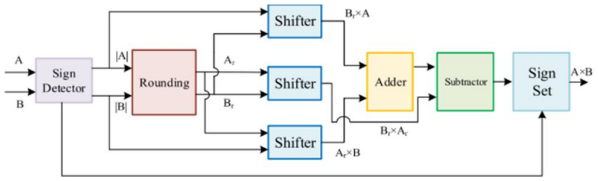

Figure 17. Architecture of proposed multiplier [21]

For efficacy, two image processing applications (sharpening and smoothing) were taken into account. The results showed same image qualities of all multipliers.

The multiplier used in this paper by the author was based particularly on characterized rounding of the input in the form of 2*n*.

Q. Two Staged Operand Trimming Approximate Logarithmic Multiplier

In [22] TL16-8/4 approximate logarithmic multiplier is used to reduce area utilization and energy consumption while maintaining acceptable accuracy compared to other approximate logarithmic multipliers.

The input operands are split into two parts of which the parts. Logic circuitry at the multiplier input selects the upper part of the split operand if it contains even a single ON bit, else the lower part is input. Thus, bit width gets reduced, leading to reduced complexity.

Further a mantissa extractor has been proposed which trims the mantissas of logarithmic operands.

The proposed 16-bit inexact logarithmic trimming multiplier utilized 40-50% lower area and 25-40% lower energy compared to an exact radix-4 multiplier. More than 90% of products generated by the proposed design were found to have less than 12.5% relative error.

R. Inexact Adders Design Methodology for Image and Video Processing Accelerators

Soares et al. [23] developed an algorithm for design of energy efficient add-and-shift accelerators for image and video processing. The proposed design methodology is based on fast search heuristics to configure less power consuming inexact adders.

The hybrid approximate adders successfully reduced the power consumption up to 73.2% and area reduction up to 73.8%. Improved quality testing of average results and variability is attained from parallel prefix adder (PPA) topologies and VOS estimation.

III. Conclusions

Approximate circuits trade the accuracy of the system for power savings in the device.
In this review we have presented various models proposed by previous studies that make use of traditional approximation techniques including: truncation, partial product approximation, and rounding off, to create novel algorithms.
The circuits and algorithms for adders and multipliers proposed in the studies have successfully reduced the delay and area of arithmetic circuits used in DSP applications, without much loss in PSNR quality of the output.
TOSAM [11] and LETAM [12] truncation models outperform rounding based approximate multipliers [21] and traditional truncation, providing higher accuracy, and reduced delay, area and power consumption.
Partial product approximation using radix encoding [6], [8] surpasses probabilistic approximation [18] and alteration of partial products [17], in terms of power consumption.
Inexact compressor, based multiplier architectures [7], [14] outperform all other reviewed multipliers in terms of power efficiency.
Reviewed approximate adder cells have notably reduced the transistor count in the circuit, thus reducing circuit complexity.
For the purpose of optimizing speed and power efficiency in DSP applications, this review serves as a guide for further research and development in approximate circuit design.

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