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Design and Simulation of an Optimized 8-Bit Hybrid Adder using Xilinx Vivado

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***Abstract*— Efficient arithmetic units are crucial components of a digital system, particularly Digital Signal Processors (DSPs) and also digital circuits that require optimized use of power, area and other performance parameters. This paper presents the design and simulation of architectures of pipelined and non-pipelined 8-bit hybrid adders using Xilinx Vivado Design Suite. The proposed architectures combine the speed of a Carry Select Adder (CSLA), and the area efficiency of a Carry Skip Adder (CSKA) to achieve an optimal balance in the performance parameters of both the standalone adders. The design is modeled using Verilog HDL and verified through functional simulation and post-RTL synthesis. The results demonstrate that the hybrid developed achieves a significant improvement in performance parameters such as power consumption, utilization and timing analysis, compared to each individual adders, making it a suitable design for energy efficient and high-speed circuit.**

***Index Terms*— Digital Signal Processors (DSP), Pipelined architecture, Hybrid Adder, Carry Select Adder (CSLA), Carry Skip Adder (CSKA), Verilog HDL, performance parameters, RTL synthesis.**

I. INTRODUCTION

In digital systems, adders are essential arithmetic units responsible for processing images, signals, audio, and video data. They directly impact overall system performance and support several higher-level mathematical operations such as multiplication, accumulation, and division. Since addition lies at the core of these computations, the primary performance limitation often arises from carry propagation delay, making high-speed adder design a critical requirement in real-time digital applications.

Adders also play an important role in various domains depending on the application. For example, multipliers in microprocessors and controllers repeatedly use addition operations and hence the efficiency of multipliers is strongly dependent on the speed and performance of adder circuits [1]. As the complexity of digital signal processing modules, such as OFDM, MIMO, image blending, etc., continues to grow, there is a demand for arithmetic units that offer high speed, low power consumption, and reduced area overhead [2]-[3].

The traditional adder design like Ripple Carry Adder (RCA) is quite simple but faces a problem of substantial carry propagation time. In this context, many fast adder designs have been introduced, including Carry Look-Ahead Adders (CLA), Carry Select Adders (CSLA), and Carry Skip Adders (CSKA).

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Although CSLA is very fast because of its parallel sum computation, this design also faces some drawbacks related to area and power because it consists of replicated RCA units for computing outputs for both cases of carry input [3], [4]. Like this, CSKA adders face performance limitations based on blocks.

To overcome these drawbacks, several researchers have explored different hybrid adder architectures that combine the strengths of more than one type of adder. Hybrid adders and multipliers have demonstrated improvement in energy efficiency and reduction in time-delay in DSP-based systems [5]. FPGA-based hybrid adder units provide further advantages in flexibility and high-speed implementation [6]. Besides integrating different architectures, another popular method to enhance arithmetic processing in DSP applications is pipelining. Pipelined hybrid has shown reduction in the critical-path delay and enhancement in the throughput. This makes them ideal for deep-learning accelerators and real-time DSP applications [7]-[10].

With these requirements in mind, a new hybrid adder design is proposed, integrating Carry Skip and Carry Select concepts and also with a 2-stage pipelined approach that reduces both delay time and enhances the throughput rate in DSP-related applications. Unlike previously proposed CSLA-CSKA architectures that focus exclusively on ASIC technology, this new design takes an advantage of the rapid bypassing of carry signal in CSKA, along with the simultaneous processing advantage of CSLA, further reduced by pipelining in order to avoid delay in critical paths, allowing it to run quickly at higher clock speeds. The design focuses on FPGA optimization, where CSKA is selectively used in the lower bits and CSLA in the higher bits, incurring less hardware costs.

II. Literature Survey

Research on improving adder performance has centered on hybrid architectures, optimized logic techniques, and pipelined computation structures to support the increasingly rapid data processing (DSP) and process area expansion of modern FPGA-based systems. Hybrid adding, optimised carry-generation methods, and pipelined arithmetic units are common areas analyzed in works [1, 2] to design efficient computation blocks.

Dinesh Kumar and Ganesh Babu [11] introduced a hybrid parallel-prefix adder to handle high-velocity AI and deep-learning arithmetic nodes. By designing the corresponding Binary-to-Excess-1 Converter and applying Cin=1 as the carry-select, their method minimized gates, switching, and power requirements for its design as compared to CSEL-BEC, CSEL-RCA, and KS-RCA architectures. In the 90 nm technology, based on the proposed adder, the delay improvements were 76.39%, 70.86%, and 3.27% and power saving was achieved up to 28.92%, suggesting a good match for low power, high frequency arithmetic circuits.

Likewise, Thamizharasan and Kasthuri [12] proposed a Hybrid Carry-Select Adder of a Han-Carlson prefix stage and a BEC-based hybrid stage. After performing all 4-bit subblocks in parallel with zero redundant carry computations, the design resulted in significant delay upgrades of 49.06 % over RCA, 52.61 % over CBL-CSLA and up to 71.59 % over Ling-based CSLA on a Virtex-6 FPGA. They showed how strong hybrid structures were of both SoC and FPGA-based arithmetic units requiring high speed and area efficiency.

Vallabhuni et al. [13] evaluated Ripple-Carry, Carry-Select and Carry-Skip adders for VLSI implementations. In this study, adder performance is emphasized as important features within DSP processors. We are sure that even though CSA provides highest performance, CSKA provides a trade-off between speed and area, thus making it relatively attractive for optimized data path designs. By simulation on Xilinx Vivado each architecture's practical performance in the face of different design constraints was checked.

Swetha et al. [14] provided two tailor-made Carry Select adder designs. D-Latch-based and MUX-based, for DSP FIR filter fabrication. Based on 32 nm technology synthesized in Synopsys tools, the architecture can achieve significant delays reduction of 60–75% as well as 22–56% of power saving against conventional CSLAs. This higher delay–power product, despite the minor overhead on the area, confirmed how well CSLA improvements apply to low-power DSP environments.

Mukherjee [15] presented CCGDI-based hybrid full adder for low power MAC modules for portable/IoT devices. The design was equipped with a 12-transistor XOR–XNOR core with an effective latency of 34.23 ps and total power consumption of 9.48 μW, resulting in PDP better than CMOS and traditional GDI adders. This architecture greatly reduces switching activity and is appropriate for battery-operated, power-efficient arithmetic systems.

Upendra Raju et al. [16] used a pipelined multiplier with a high accuracy 4-2 compressor, which has the reduced critical path delay as well as a trade-off between accuracy and performance.

Similarly, Mysura Reddy et al. [17] developed a pipelined FFT architecture which substantially enhances the throughput and decreases latency in real-time DSP applications while also maintaining low hardware utilization. Despite the complexity that comes with pipelining, the design is a bit more convoluted, but is very effective in performance in contemporary digital systems.

III. PROPOSED SYSTEM METHODOLOGY

This project deals with the development of an 8-bit hybrid adder using two standalone adders with two types of architectures. An 8-bit data length is selected as the evaluation case to enable clear analysis of power, performance and area. This architecture is modular to 16 and 32-bit data length by modifying the input-output bus width and scaling the adder blocks appropriately. The first method studied upon is using non – pipelined technique, followed by a comparative study of a 2-stage pipelined architecture. The design employs the speed of CSLA and the area efficiency of CSKA to achieve an optimal balance in the performance parameters. CSLA is used for the upper bits and CSKA is used for the lower bits.

The decision to use these as the standalone adders was due to the following reasons:

CSLA is well-known for its fast carry propagation due to precomputing sum values for both possible carry inputs. However, this advantage comes at the cost of increased hardware area and higher power consumption, as it requires duplicate adder circuits for every group of bits. In a full-width implementation, this can lead to inefficient silicon utilization and unnecessary resource usage. In the hybrid design, use of CSLA for the upper bits is done. This is because the carry computation delay has a greater impact on overall speed. This significantly reduces the number of duplicate adder blocks, lowered area and power while also achieving fast computation for the most significant bits (MSBs). CSKA improves speed by allowing carry to bypass groups of bits through skip logic. This is often faster than a simple ripple-carry adder. Despite this, CSKA performance degrades for higher-order bits. Therefore, its speed improvement is less pronounced in larger bit-widths. By assigning CSKA to the lower bits, the hybrid adder can efficiently bypass carries for least significant bits (LSBs), enhancing the performance without the area consumption of a full CSLA implementation.

A. Phase 1: Design of Non – Pipelined architecture

The first implementation uses simple combinational adder without using any registers or flip-flops. This helps reduce the overall power consumption and area utilization, making this architecture suitable for applications where low power and compact sizes are critical. But due to its combinational nature, the speed limitation due to sequential processing makes it unsuitable for high-frequency computations required by modern processors.

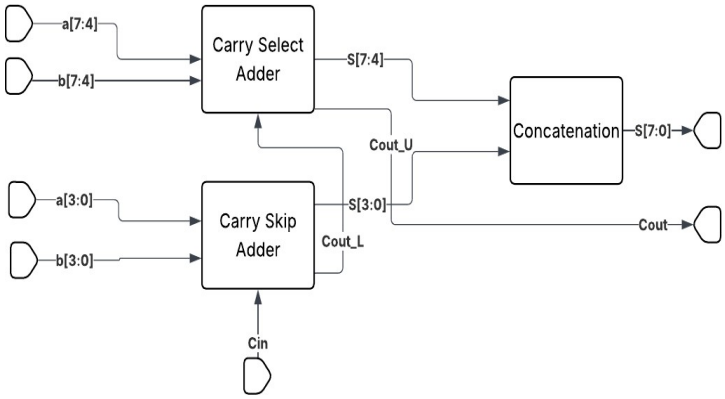

Figure 1. Block diagram for Non-Pipelined architecture

B. Phase 2: Design of Two – Stage Pipelined architecture

To improve the speed performance, pipelining is applied to divide the adder into two balanced stages with registers placed between them. The two-stage pipeline was selected as an optimal trade-off between performance improvement and implementation overhead. A single stage adder suffers from long propagation delay, whereas a multistage pipeline is inefficient for smaller data width such as 8-bit. The overhead of pipeline registers would outweigh the advantages due to pipelining. Therefore, splitting the adder into 4-bit partial stages gives the most optimal results.

In the proposed design, the partial sum results will be stored in registers between the stages, which reduces the critical path delay and improves the maximum operating frequency. The implementation is referred to as 2-stage pipelined hybrid adder. The area utilization increases due to the adder pipeline registers and control elements. However, the dynamic power consumption also rises, making the device less suitable for low-power applications.

Despite these drawbacks, the throughput of the system significantly improves due to pipelined processing.

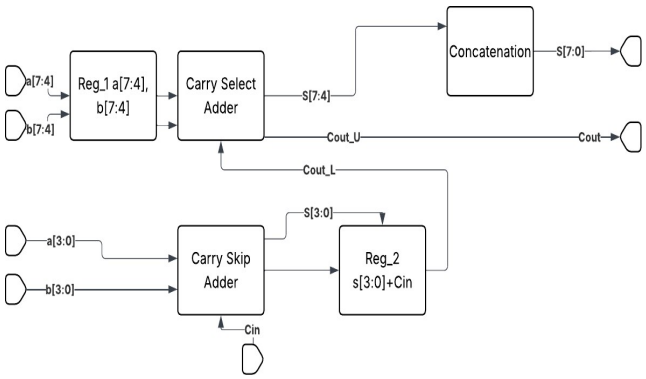

Figure 2. Block diagram of Pipelined architecture

IV. Experimental Results

The project was developed using Verilog HDL to describe and implement the design of the individual and the hybrid adder. Xilinx Vivado was utilized as the primary tool for simulation, synthesis and the analysis of power, performance and area utilization (PPA analysis).

The proposed hybrid architectures were implemented on Artix-7 FPGA family, (XC7A100T324-1) using Vivado Design Suite. Both the non-pipelined and the pipelined architectures were analyzed using the same performance matrices to ensure fair comparison. The performance parameters include total delay, total on chip power, and resource utilization. By analysing these results, the efficiency of pipelining strategy in improving speed and performance is demonstrated.

The power consumption of this design, was found to be 12% lesser than its pipelined design counterpart. The delay of this design was found to be 30.7% less than its non – pipelined counterpart. This makes the design highly suitable for applications demanding high – speed computation.

A. Results for non – pipelined architecture.

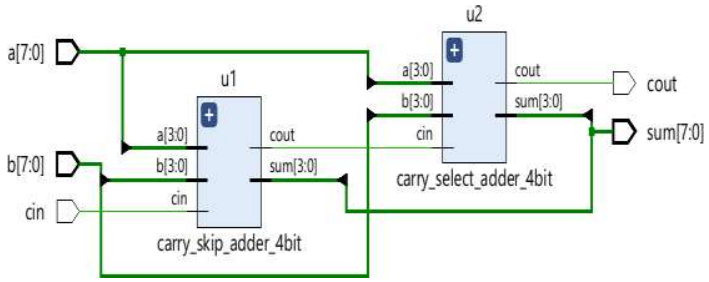

Figure 3. RTL design of non-pipelined hybrid adder

As per the proposed architecture, the RTL design of the 8-bit hybrid structure with non – pipelined architecture was simulated in Xilinx Vivado. The RTL design clearly shows the usage of the standalone adders individually performing the addition of bit-groups. The lower bits are being operated with the help of CSKA and upper bits with CSLA. the resulting Cout from CSKA is fed to the CSLA block as Cin, which precomputes the results for both possible carries, therefore speeding up the final result calculation process.

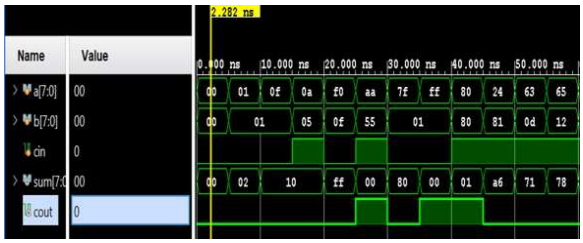

Figure 4. Simulation waveform of non-pipelined hybrid adder

By optimally integrating these two adder structures, the hybrid design minimizes critical-path delay while maintaining low hardware overhead, making it suitable for high-speed arithmetic units in DSP and low-power VLSI applications. The functional simulation of 8-bit hybrid adder without pipelining confirms the correct arithmetic behaviour of different combinations of input operands. The 8-bit inputs a[7:0] and b[7:0] are applied without any intermediate register storage, and sum[7:0] is generated within the same cycle. A purely combinational design was implemented as the output transitions occur immediately. The cout signal is asserted only when the output signal is overflowing.

B. Results for pipelined architecture.

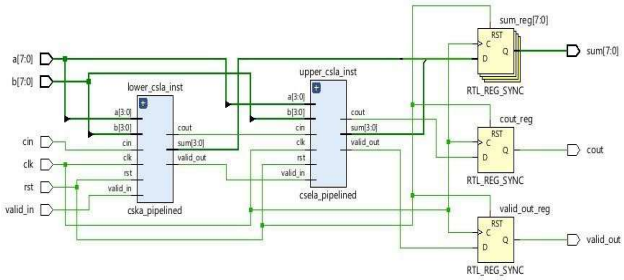

Figure 5. RTL Design of Pipelined hybrid adder

The pipelined hybrid adder integrates lower and upper blocks with registers, enabling pipelining of the structure. The CSKA efficiently accelerated the carry propagation of through the lower bits, while CSLA precomputes the carry for two possible cases of Cin. Pipeline registers are strategically inserted between the two adder blocks, as well as at the outputs, enabling reduced critical-path length and higher operational frequency. The use of clock, reset, and valid-signal synchronization ensures proper data flow and supports continuous high-throughput processing. This hybrid pipelined approach offers a superior balance between area, delay, and power, making it suitable for high-speed arithmetic units in FPGA-based system and DSP applications.

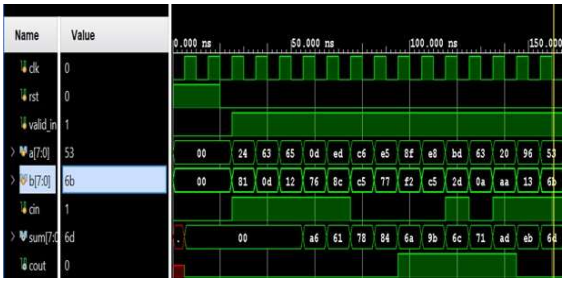

Figure 6. Simulation waveform of Pipelined hybrid adder

The pipelined hybrid adder allows input operands to be processed concurrently across two stages by introducing sequential registers between the lower CSKA and upper CSLA blocks. The waveform illustrates how when valid_in is asserted, input values a[7:0] and b[7:0] are recorded on the positive clock edge. Pipeline latency causes the corresponding results sum[7:0] and cout to be shown after one clock cycle. The valid_out signal indicates that a new valid output is generated after each cycle, once the pipeline is filled. This demonstrates enhanced throughput performance while also preserving accurate arithmetic functionality.

C. Comparative analysis

By comparing the two configurations, the trade-offs between hardware overhead and performance are clear. The pipelined design achieves a setup-time reduction from 6.537 ns to 4.090 ns (≈37.4%) and a hold-time improvement from 2.073 ns to 0.288 ns (≈86.1%). This indicates a shorter critical path and better timing stability. These gains are achieved with a slight increase in resources. The look up tables (LUTs) rise from 10 to 11, and 40 additional flip-flops are required. The power consumption also increases from 5.937 mW to 6.172 mW. Thus, pipelining improves timing reliability and throughput for high-frequency applications. The non-pipelined hybrid remains preferable while minimizing area and power is the priority. The results were obtained using Vivado's default synthesis settings. Although synthesis directives (area or performance optimization)

affect the trade-off between delay and resources, both architectures were evaluated under identical conditions. Hence, the proposed design remains robust across typical synthesis strategies, with only minor variations in area or power.

TABLE I: COMPARATIVE ANALYSIS OF NON-PIPELINED AND PIPELINED HYBRID ADDERS WITH RESPECT TO STANDALONE ADDERS

Architecture	Adder	Power (W)	Timing analysis (ns)		Utilization	
			Setup	Hold	LUT	FF
Non-Pipelined	CSLA	5.953	6.545	2.073	10	-
	CSKA	5.893	7.102	2.071	8	-
	Hybrid Design	5.937	6.537	2.073	10	-
Pipelined	CSLA	6.324	4.090	0.388	15	26
	CSKA	6.084	4.090	0.451	8	24
	Hybrid Design	6.172	4.090	0.288	11	40

The proposed pipelined hybrid adder achieves a setup delay of 4.090 ns with 11 LUTs, representing a 37.4% delay reduction compared to its non-pipelined hybrid version (6.537 ns). In comparison, the hybrid prefix adder in [11] reports up to 76.39% delay reduction, but this is achieved in 90 nm ASIC technology with higher architectural complexity. FPGA-based hybrid CSLA designs in [12] demonstrate 49.06%–71.59% delay improvement, but at the cost of increased multiplexer stages and higher logic utilization. System-level CSLA implementations in [14] achieve 60–75% delay reduction, though these gains are application-specific and not at standalone adder level. Circuit-level optimization in [15] reports 34.23 ps delay for a single full adder, which does not directly scale to word-level designs. The proposed design offers competitive timing improvement with lower logic overhead under uniform FPGA synthesis conditions, making it well suited for high-speed arithmetic and MAC-oriented applications.

V. CONCLUSION

Overall, in this work, an 8-bit hybrid adder architecture was designed and evaluated using both non-pipelined and pipelined architectures. From the non-pipelined analysis, the hybrid adder achieves a power value of 5.937 mW, while maintaining setup and hold requirements similar to the conventional adders. When pipelining is introduced, the performance improves significantly, reducing setup time to 4.090 ns and hold time to 0.288 ns. This clearly shows the impact of pipeline registers to achieve high-speed operation.

The comparison presented in Table 1 confirms that the hybrid adder delivers better performance than designs based on standalone adder architectures. The pipelined version further enhances throughput while maintaining the power consumption. Therefore, combining different adder logic styles with pipelined stages results in a balanced trade-off between speed, area, and power.

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