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Efficient Techniques in Full Adders and Logic Gates with Optimum use of Multi Valued Logic, Double Pass Logic and Ternary Logic in CNTFET Technology with Comparative Analysis with CMOS Technology

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***Abstract*—In this paper, carbon nanotube field effect transistors (CNFETs) technology is analysed with respect to Full Adders, Half adders and logic gates with MVL and ternary logic. The assorted paper shows that CNTFET along with MVL and DPL are much better than CMOS technology. It is observed that ternary logic circuits are effective in providing lower power consumption with several interconnections. The power consumption and average delay in CNTFET based ternary full adders have been reduced upto 51.9% from 89.09% in CMOS counterpart. Quantum-Dot Cellular Automata (QCA) technology is found to be much effective than other existing technologies.**

***Index Terms*— BTME, CNTFET, DTME, QCA.**

I. INTRODUCTION

A. CNTFET

A Carbon Nanotube Field Effect Transistor refers to FET that utilizes only one CNT or series of CNTs as channel in place of using bulk silicon to make MOSFET structure. Carbon Nanotube Field Effect Transistors (CNTFETs) are skilled nano - scaled devices designed to be used in high and low power consumption circuits.

B. Scaling of MOSFET

1. Silicon wafers with highly doped p-type are used to make gate implementation.
2. Then oxidation is performed. Nickel and aluminium are chosen to make catalyst layer and facilitate the growth.
3. Now perform CVD (Chemical Vapour Deposition) modeling.
4. Now lift the electrode structures [1].

According to Moore`s law, the no. of transistors in an integrated circuit/chip will doubled about or after every 2 years. Moore`s law is observation and projection of past decades. It is a resulting formula that is connected with gains from experience in productivity [2]. As we know that energy efficiency is one of the most important features for electronic systems with higher performance in such industrial experiments and its

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applications. Basically, algorithms and logics in computation of digital are purely dependent on the 2 -valued code, i.e., high or low (0, 1). In a transient state where the logics are changing from (0 to 1) or changing from (1 to 0), ternary full adder logics (three valued logic) can be used in a binary logic of digital computation that is (0 or 1) [3]. Steady state growing in device scaling that progress in demand for power- efficiency, highly speed efficient circuits that are capable of multi tasking stereotypes that is Radix-2 (binary ,0 and 1) number systems[4] as compared to Radix-2 system , multi-valued logic that increase the performance of digital circuits.
Converter using multi-valued logics have more number of input gates MOSFETS for signed ternary 16nm CMOS technology. The designing of circuits is expensive if we use devices with gates of floating inputs, which are not good with CMOS structure design using the functional circuits up-to date [4]. The ternary full adder has achieved high speed and reduced power with less complexity using CNTFETS. However, delay, time equalization, and power consumption are essential tasks to reduce effective output delay for high speed operation using wave – pipelining.

II. PROPOSED DESIGN

The trans-conductance and output resistance are implemented on 16nm CMOS, the intrinsic gain of transistors is about 10, resistance is purely of the order 350ohm and matched input of 50ohm[13].

A. Static Ternary Logic Double Pass Transistor as Novel CMOS

As in Fig.1, new static TDPL is Simplified ternary inverters (STI)/ternary identity cell. The pMOS substrate will be connected to Vdd and GND is connected to nMOS [14]. The above analysis is based without static power consumption, and clocks are realized in the circuit based on the input and ternary logic. [14].

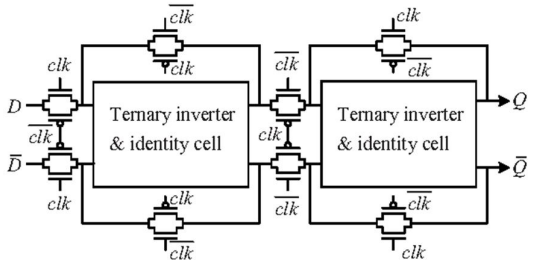

Fig.1

B. Device Model

As the CNTFET model of the intrinsic channel region has the device non-idealities, elastic scattering also includes the resistance of quantum dot and the parasitic capacitance with the doping source to drain region itself as well as source to base resistance that interfering between the doped CNT and source to drain contact with metal[15].

C. Delay Ternary Memory Element

A very important and useful element in binary logic is delay (D) flip-flop. Input application depends on a clock pulse and implementation of shift registers. Delay ternary memory elements (DTME) can be designed using binary ternary logic elements (BTME) with pMOS connected to ground and nMOS connected to Vdd [16].

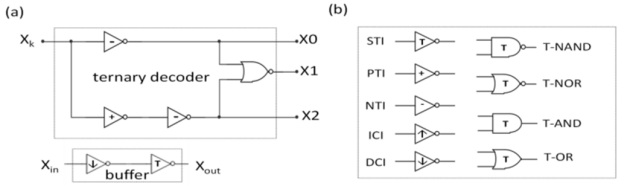

Fig.2

The conversion from ternary to binary bit is standardized for CMOS in which we have multiple input floating gate MOSFETS. The design and fabrication will be done at 16nm n-well CMOS process and we tested the performance [17].

TABLE-I

Voltage level	Logic value
-Vcc	0
0	1
+Vcc	2
binary	0 and 1

D. Design of Robust, Energy Efficient Full adder Using ternary logic

Basically the optimization of design to ignore any kind of degradation at the output and final level, voltage at output, absorbed less power, and delayed in the critically path delay and also have been at less voltage supply. As we know that full-adder using ternary logic has duplicated cells in large numbers, regularity in layout, and interconnected complexity is also an important factor [18].

Designing of full adder using k-map has its own advantages and disadvantages. The main disadvantage of static CMOS circuit in pMOS linear block is less mobility of the pMOS devices as compared to nMOS devices. This is the only reason why pMOS device sized upto attain the desired performance [18].

E. Ternary AND/NAND-OR/NOR

Ternary full adder buffer or NOT circuit, a new AND/NAND and OR/NOR are also designed. The voltage transfer characteristic shows abrupt changes for the ternary logic but a linear line to a buffer ternary logic [19].

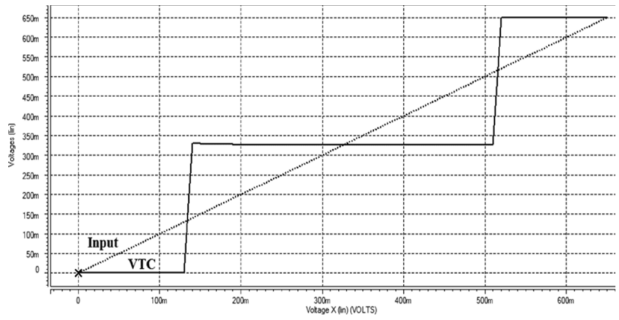

Fig.3

F. Quantum Dot Cellular Automata

The QCA shell switches to polarization in between the 2 polarizations which include the excess of electrons and the dots of the cells. The QCA cells will maintain their current polarization and will not change their states due to the neighboring cells[20].

III. SIMULATION RESULTS

The design and fabricated ternary logics using half and full adders logic gates show good ternary performance as compared to silicon ternary and CNT ternary full adder. The designing shows 59% reduction in numbers of transistors in comparison to already existing CNT ternary full adder. In future, this circuit will be used in applications with data of higher density, area with smaller chips, higher computation speed [21].

CMOS also differential ring oscillators, with very low supply voltage at the end of voltage controlled oscillator [22].

The analog circuit performance depends upon faster performance of frequency and capacity of driving embedded op-amp of power consumption trade off [23].

IV. CONCLUSIONS

Reduced power dissipation, less noise margin and reduced power delay are obtained using H-SPICE having PVT variations. PVT and EDP designed 1.5x and 5.6x lower than that of the most accurate state art of design. From the H-SPICE simulation results, the effective and proposed approach is valid with 16nm CMOS device parameter with the sequential circuit and ternary half and full adder.

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