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A Novel H Bridge- based Inverter with 21 Level Staircase Output

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***Abstract*—Multilevel inverter is an emerging technology in the field of power electronics without which there is no industrial growth. High power sinewave inverter with minimum distortion is required in numerous applications of the industry. This requirement is not attainable using a single switch and therefore multilevel inverter stretched its hands with its several advancements. In present days multilevel inverter takes its role with staircase output and reduced harmonics. The 21 level inverter is proposed here with reduced number switches and reduced harmonics. Since the number of switches are reduced the switching frequency is also getting reduced. The power quality of the proposed 21 level inverter is increased by using selective harmonic elimination technique (SHE). The staircase output is achieved with the simulation using MATLAB/ SIMULINK and the same staircase output is obtained with the implementation of hardware also.**

***Index Terms*— Multilevel inverter (MLIs), PWM techniques and Total Harmonic Distortion (THD), Cascaded H-bridge, SHE.**

I. INTRODUCTION

According to "Ref. [1]", since 1975, the multilevel inverter took its form. The crucial development of the multilevel inverter initially started with three levels after which several multilevel inverter topologies have been industrialized. The staircase output is obtained by the use of series power semiconductor switches and several DC sources with lower voltages. As DC sources, batteries, capacitors and also renewable voltage sources can be used. The commutation and gate signal requirements of more number of switches make the system complex and expensive and so multiple DC sources are used. The rated voltage of the switches is based on the DC voltage source to which the switches are connected. As in "Ref. [10], in the history of multilevel inverter there are three different types of structures have been implemented. They are Cascaded H-bridge converter with separate dc sources, diode clamped (neutral clamped), and flying capacitors (capacitor clamped). Out of these technologies Cascaded H-Bridge multilevel inverter is one of the well-known, most advantageous, much simpler and basic method of multilevel inverter.

As in "Ref. [2]" in the cascaded multilevel inverter, H-bridge inverter is used. Number of H bridges are connected in series, each H-bridge having a separate DC source. The capacitor or diode is not required for clamping purpose. These are the advantages of cascade multilevel inverter over diode clamped and flying capacitor multilevel inverter. And also as we see in the output waveform will be sinusoidal in nature if

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number of level is increased and even we don't filter it. Reference [1], also discusses the plentiful modulation techniques and control models that have been developed for multilevel inverters. They are sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM) and others.

Of these techniques, SHE technique is used in our 21 level inverter since it provides a suitable solution for medium and high power systems to synthesize an output voltage which allows a reduction of harmonic content in voltage and current waveforms.

II. MULTILEVEL INVERTER

The concept of multilevel Inverter (MLI) is kind of modification of two-level inverter. In multilevel inverters, more than two voltage levels are combined together in order to create a smoother stepped output waveform, and the output waveform obtained in this case has lower harmonic distortions. Smoothness of the waveform is dependent on the voltage level, (i.e.) as we increase the voltage level the waveform becomes smoother.

A. Advantages of Cascade H Bridge Multilevel Inverter

"Ref. [3]" discusses the advantages of the cascaded multilevel inverter over different multilevel inverter configurations.

- Capacitors or clamping diodes are not needed for.
- Even if we don't filter the output, the output waveform is quite sinusoidal in nature.
- Automatic voltage sharing, smaller dv/dt stresses, switching redundancy
- Requirement of least number of components

B. Block diagram

Fig. 1 explains the operation of the multilevel inverter. The DC supply is given to the multilevel inverter. The DC sources are chosen to be asymmetrical so that the number of output voltage level is increased. The controlled signals for switches of the inverter are generated by using PIC micro controller and these signals are amplified in the driver circuit. These amplified signals are fed to the switches of the MLI and the staircase output waveform is displayed in CRO.

C. Cascadded H-Bridge Topology

As in "Ref. [4]"Cascaded H Bridge multilevel inverter is one of the most important topologies of multilevel inverters. It can be used for both single and three phase conversion. In Cascaded H-Bridge multilevel inverter, Number of H-Bridges are connected in series. Each H-Bridge has separate DC source which is to be obtained from any natural sources such as sunlight or wind energy or anything, ultra-capacitors, fuel cells or batteries to produce inverted ac output. From "Ref. [3]" it is clear that, the Cascaded H Bridge multilevel inverter is constructed to produce an anticipated AC voltage from several levels of DC voltages. It is also simpler than diode clamped and flying capacitor multilevel topologies because of the above mentioned advantages.

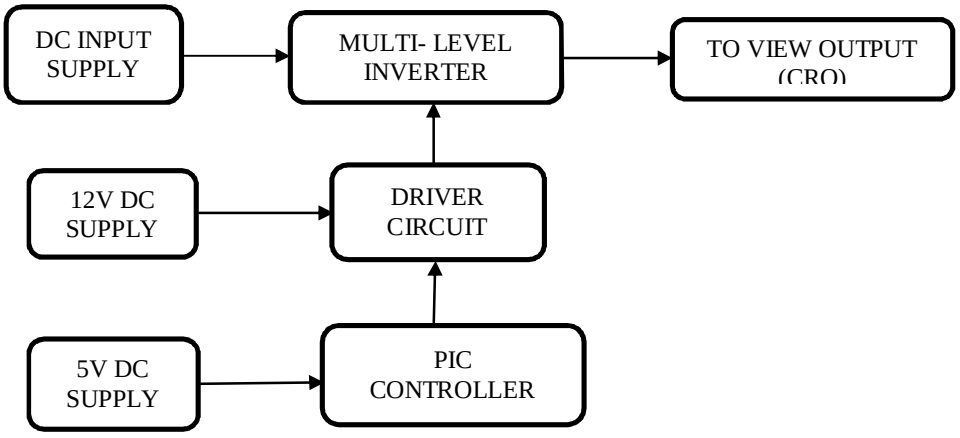

Fig.1 Block diagram of multilevel inverter

D. Proposed system

A new multilevel inverter with reduced number of switches and gate driver circuits is proposed in this paper. The proposed topology is shown in fig. 2. The output level is increased up to 21 with reduced THD and the switching losses also get reduced. From "Ref. [11], the PWM techniques are used in conventional approach where the reference and carrier signals are compared to provide the required gating signals and these signals are given to the inverter switches. The number of switches required to achieve m levels is given by Ns = 2(m − 1). According to this equation, for the implementation of 21-level CMLI, the number of switches required is 40. These 40 switches are reduced to 12 switches in the proposed ACMLI topology. Four isolated DC sources are used. As in "Ref. [5]" the output voltage is divided into two parts. The left side is called level generation part which is responsible for level generation in positive polarity & negative polarity. The right side is called polarity generation part which is responsible for the generation of polarity of the output voltage. These two parts (left part and right part) are combined to generate the multi-level output voltage waveform. This proposed ACMLI topology controls the EMI, minimizes the total harmonic distortion using selective harmonic elimination (SHE) technique and also minimizes power semiconductor switches than conventional multilevel inverter. The conventional single-phase 21-level inverter uses 40 switches, whereas the proposed topology uses only 12 switches with the same principle. For the pulse generation PIC microcontroller PIC16F877A is used.

E. Operation of the Proposed Topology

"Ref. [5]" Table 1 explains the different switching ON, OFF states of different switches for obtaining different voltage levels. Complementary pair of switches are S9, S10, S11 and S12. Positive half cycle (level: +1, +2, +3, +4…) can be generated across load when S9, S10 are turned ON together and negative half cycle (level: -1, -2, -3 and -4…) can be generated across load when S11, S12 are turned ON together. For the output voltage to be "zero" (level 0), the switches S2, S4, S6 and S8 switches are turned ON. For the output voltage to be "V_{DC}" (level +1), switches S1, S4, S6 and S8 are turned ON. For the output voltage to be "2 V_{DC}" (level +2), switches S2, S3, S6, and S8 are turned ON. Switches S1, S3, S6 and S8 are turned ON, for the output voltage to be "3 V_{DC}" (level +3). Switches S1, S4, S6, S7 are turned ON for the output to be "$4V_{DC}$" (level +4). Switches S1, S3, S5, S7 are turned ON for the output voltage to be "$5V_{DC}$" (level +5). Switches S1, S3, S5, S8 are turned ON for the output to be "$6V_{DC}$" (level +6). Switches S2, S4, S5, S7 are turned ON for the output to be "$7V_{DC}$" (level +7). Switches S1, S4, S5, S7 are turned ON for the output to be "$8V_{DC}$" (level +8). Switches S2, S3, S5, S7 are turned ON for the output to be "$9V_{DC}$" (level +9). Switches S1, S3, S5, S7 are turned ON for the output to be "$10V_{DC}$" (level +10). So, complementary pair S9, S10 are in ON condition for all these positive 10 levels. For all the negative 10 levels, the same switches are in ON condition, but the complementary pair S11, S12 will be in ON condition.

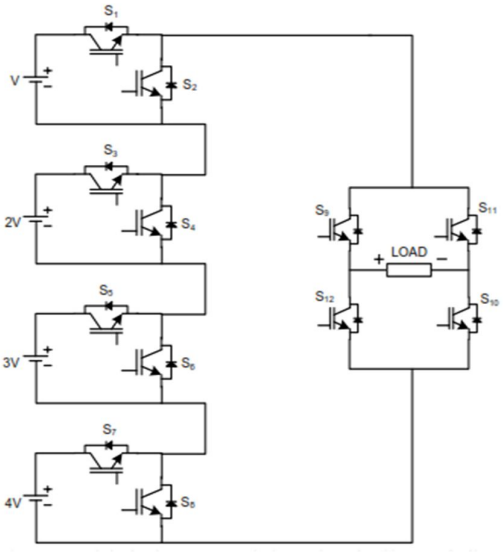

Fig.2 proposed topology

TABLE I. SWITCHING STATES OF PROPOSED SCHEME

Voltage level	Switching State												Output Voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
+10	1	0	1	0	1	0	1	0	1	1	0	0	10V
+9	0	1	1	0	1	0	1	0	1	1	0	0	9 V
+8	1	0	0	1	1	0	1	0	1	1	0	0	8 V
+7	0	1	0	1	1	0	1	0	1	1	0	0	7 V
+6	1	0	1	0	1	0	0	1	1	1	0	0	6 V
+5	1	0	0	1	0	1	1	0	1	1	0	0	5 V
+4	0	1	0	1	0	1	1	0	1	1	0	0	4 V
+3	1	0	1	0	0	1	0	1	1	1	0	0	3 V
+2	0	1	1	0	0	1	0	1	1	1	0	0	2 V
+1	1	0	0	1	0	1	0	1	1	1	0	0	1 V
0	0	1	0	1	0	1	0	1	1	1	0	0	0 V
-1	1	0	0	1	0	1	0	1	0	0	1	1	-1 V
-2	0	1	1	0	0	1	0	1	0	0	1	1	-2 V
-3	1	0	1	0	0	1	0	1	0	0	1	1	-3 V
-4	0	1	0	1	0	1	1	0	0	0	1	1	-4 V
-5	1	0	0	1	0	1	1	0	0	0	1	1	-5 V
-6	1	0	1	0	1	0	0	1	0	0	1	1	-6 V
-7	0	1	0	1	1	0	1	0	0	0	1	1	-7 V
-8	1	0	0	1	1	0	1	0	0	0	1	1	-8 V
-9	0	1	1	0	1	0	1	0	0	0	1	1	-9 V
-10	1	0	1	0	1	0	1	0	0	0	1	1	-10 V

F. Harmonic elimination strategy

The selected harmonic elimination technique is used in this proposed scheme. The lower order harmonics are eliminated by using this method. "Ref. [6]" explains the reasons for implementing the harmonic elimination.
1. Harmonics causes the Electromagnetic Interference. Without harmonic elimination, snubbers or EMI filters will be needed for designed circuits for more protection as result, designed circuits would cost more.
2. EMI can interface with control signals used to control power electronics devices and radio signals.
3. Harmonics can create losses in power equipment.
4. Harmonics can lower the power factor of a load. Increased harmonic content will decrease the magnitude of the fundamental relative to the magnitude of the entire current, as a result the power factor would decrease.
In multilevel inverter there are mainly four kinds of control methods. They are 1. Traditional PWM control method, 2. Selective harmonic elimination method 3. Space vector control method 4. Space vector PWM control. The harmonics cannot be completely eliminated by using traditional PWM, space vector PWM and space vector modulation methods. The selective harmonic elimination technique which is very simple and efficient method is used in this paper. This technique is widely used in the control of conventional VSIs in order to improve much more the quality of the output voltages.

G. Selective harmonic elimination technique

"Ref. [7]", "Ref. [8]". By using Selective Harmonic Elimination technique (SHE), the efficiency of the MLI is increased by reducing output Total Harmonic Distortion THD associated with the switched output of MLI. It is done in the proposed topology by selecting suitable switching angles α1, α2, α3, etc….α21. From "Ref. [9]" for the twenty one levels configuration, the Fourier series expansion of the staircase output voltage waveform of the proposed topology is given in (1)

$$V(\omega t) = \sum_{n=1,3,5}^{\infty} \left(\frac{4V_{dc}}{n\pi}\right)[cos(n\alpha_1) + cos(n\alpha_2) + cos(n\alpha_3) \ldots\ldots cos(n\alpha_{21})]\sin(n\omega t) \ldots\ldots (1)$$

This waveform has 10 step angles $\alpha_1\alpha_2\alpha_3 \ldots\ldots \alpha_{10}$. Therefore the switching angles are chosen in such a way that it should not generate 3rd, 5th, 7th and 9th order harmonics while attaining the desired fundamental voltage. The mathematical statements of these conditions are given in the equations (2) to (6).

$$\frac{4_{dc}}{\pi[cos(\alpha_1) + cos(\alpha_2) + cos(\alpha_3) + \cdots\ldots cos(\alpha_{10})]} = V_f \ldots\ldots (2)$$

$$\frac{4V_{dc}}{\pi[cos(3\alpha_1) + cos(3\alpha_2) + cos(3\alpha_3) + \cdots \ldots . cos(3\alpha_{10})]} = 0 \ldots . . (3)$$

$$\frac{4V_{dc}}{\pi[cos(5\alpha_1) + cos(5\alpha_2) + cos(5\alpha_3) + \cdots \ldots . cos(5\alpha_{10})]} = 0 \ldots . . (4)$$

$$\frac{4V_{dc}}{\pi[cos(7\alpha_1) + cos(7\alpha_2) + cos(7\alpha_3) + \cdots \ldots . cos(7\alpha_{10})]} = 0 \ldots . . (5)$$

$$\frac{4V_{dc}}{\pi[cos(9\alpha_1) + cos(9\alpha_2) + cos(9\alpha_3) + \cdots \ldots . cos(9\alpha_{10})]} = 0 \ldots . . (6)$$

The low-order harmonics 3, 5, 7, and 9 are eliminated by using these mathematical statements.

III. Experimental Observations

The result of this staircase multilevel inverter is derived both in software and hardware.

A. Software Implementation

The circuit for 21 level inverter is simulated in MATLAB/ SIMULINK and the simulation circuit is shown in fig. 3. The gate pulses, output load current and voltage are obtained as given below in fig.4, fig. 5, fig. 6.

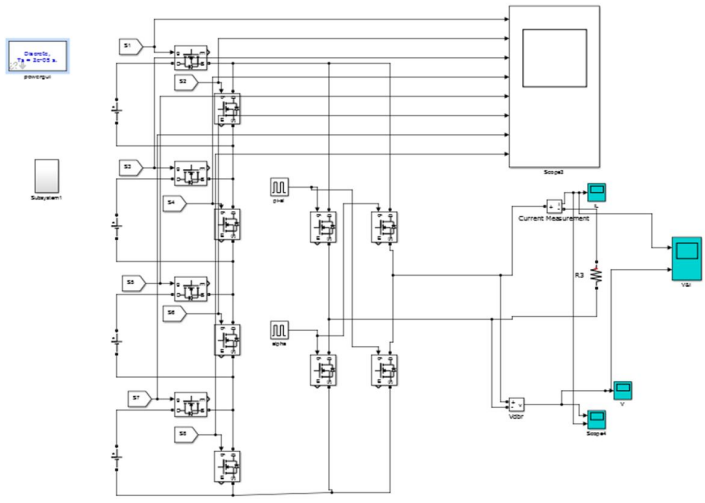

Fig. 3. Circuit diagram

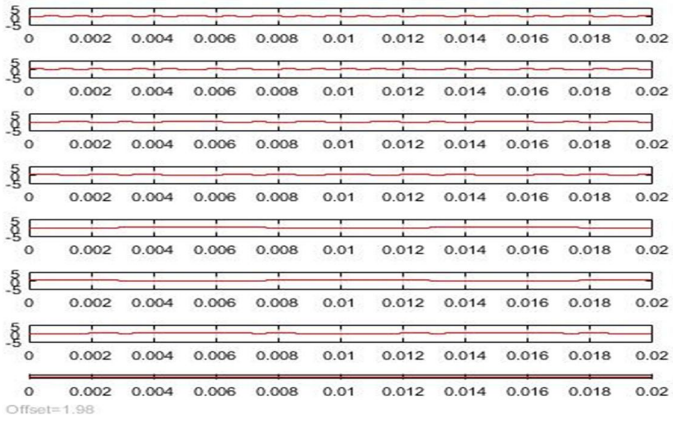

Fig. 4. Gate pulses for MOSFET

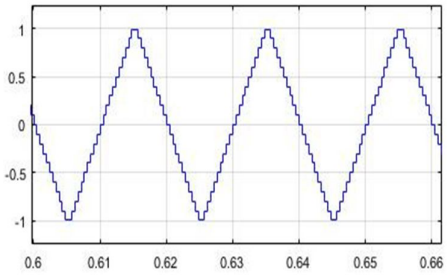

Fig. 5. Load Current

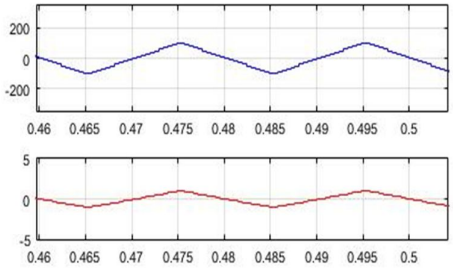

Fig. 6. Load current and voltage

B. THD Analysis

The FFT analysis is done in the MATLAB and found that the THD of the proposed multilevel inverter is reduced to 12.64% using SHE technique. It is shown in fig. 7.

C. Hardware Implementation

In the hardware of 21 level inverter since the different voltage levels 5V, 10V, 15V, 20V are set it is also called asymmetrical cascaded multilevel inverter. The whole hardware set up and the output voltage is shown in fig.8 and fig.9 respectively.

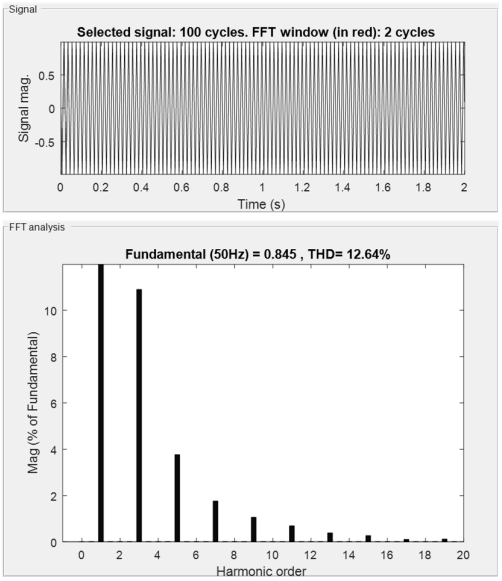

Fig. 7. THD Analysis

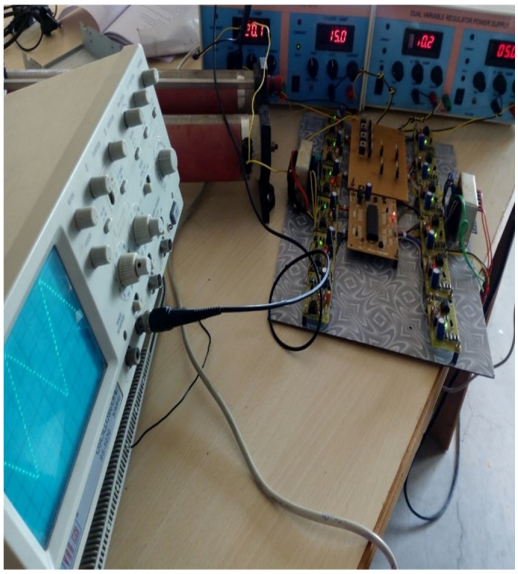

Fig. 8 Photograph of complete hardware setup

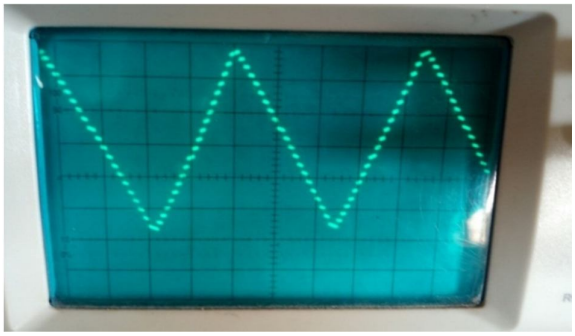

Fig. 9 Output 21 level staircase waveform

IV. CONCLUSIONS

This paper introduces a new 21 level inverter topology with asymmetric cascaded H-bridge configuration. In order for maximizing the number of output voltage levels, this asymmetric DC sources configuration is employed. DC sources are correctly sized and organized in order to let the proposed topology to produce both negative and positive half cycles. Thus the need for conventional polarity changer H-bridge is eliminated. And also, the switching losses are getting reduced and the cost required for the devices becomes less because of the use of 12 switches instead of using 40 switches. In addition to that, by using selective harmonic elimination (SHE) technique, the THD is also reduced to a reasonable value. This scheme has successfully been implemented and tested by using R2012a version of MATLAB/Simulink software. The hardware has also been designed and the staircase output waveform has been obtained.

As future work, the number of voltage levels can be increased to obtain pure sine waveform and the THD can be improved by using suitable harmonic elimination technique.

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