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Recent Trends in LC Voltage Controlled Oscillator to Achieve Low Phase Noise: A Literature Survey

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***Abstract*—The Voltage Controlled Oscillator is the most essential part of the transceivers that deals with generating a system frequency in the RF range for most of the wireless Devices. LC voltage Controlled Oscillator plays essential role in the many applications of RF frequency band – ISM frequency band (Industrial, Scientific, Medical) like Zigbee, Bluetooth, front-end RF transceiver, - IEEE 802.11a/b/g, - IEEE 802.15.4, etc. The performance and accuracy of these application designs depends upon the features and development methods of the Oscillator. As requirement to fulfil accuracy and power constrains, new techniques have been presented to improve the features like phase noise, FOM, tail current and low power. In this era, we have different methods to improve features of VCO to get the better results. Still research is going on to achieve more accurate results. So, questions may arise in researches' mind about selection of the technique to improve the performance for required application. The selection of the proper technique involves improvement of particular feature and which improves overall performance of the system. This is the main motive to write a comprehensive survey of Voltage controlled Oscillator from forgoing to contemporary. In this paper, Details of all the techniques to improve Phase noise in the RF – ISM frequency band with merits - demerits including low power and FOM is presented. In this paper comparative analysis is also given to find the features in this field. The paper is concluded with the survey, which serves as reference for the researchers in the field of RF – ISM Frequency band LC Voltage controlled oscillator.**

***Index Terms*— LC Voltage Controlled Oscillator, Phase Noise, Tail Current, Current Mirror.**

I. INTRODUCTION

The increasing demand of wireless compact devices in the recent era with special necessity of accurate and low power feature emphases the RF - designers to work at the maximum limit of the technology. Over a decade, work has been done on the Voltage controlled oscillator, which is heart of the Phase Lock Loop to generate accurate and stable system frequency. The parameters including low power, low FOM, better tuning range, compact circuit and cost need to be considered while designing. The thirst for the requirement in major applications of RF – ISM frequency band like ZigBee, RF transceivers, RF front-end for IoT applications [[1]], Bluetooth – BHE transceivers [[2]], IEEE 802.11a/b/g, Zigbee [[8],[9]], IEEE 802.22 cognitive radio receiver

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[[7]],5G transceivers [[11]], IEEE 802.15.4 [[3],[4]] and narrow band electronics [[5]], where LC Voltage Controlled Oscillator is the crucial part of the system. This requires immense scop for the researchers to design accurate LC VCO [[6]].

To fulfill the requirement of these applications, Phase Lock Loop [[12],[14]], Frequency synthesizer [[13]] and frequency multipliers are widely used to generate high system frequency from crystal oscillator or low frequency and also to synchronize the generated frequency with input frequency. As a highly required and essential building block of PLL, Frequency multiplier and frequency synthesizer, a voltage Controlled oscillator, operating at RF – ISM frequency band with low phase noise, low power consumption, accurate and wide tuning range, is highly demanded. To achieve these all parameters with scaling of MOSFET and reduced supply voltage is challenge for designers. The phase noise in the Voltage controlled oscillator plays a crucial role in the design, may degrade the overall performance of the system, if not properly optimized. In the range of GHz Frequency generation applications, Ring oscillators and LC oscillators are commonly used [[15],[16] ,[17]]. Compare to LC oscillator, Ring oscillators suffer from poor phase noise, so LC VCO is the better choice for RF -ISM band applications. LC VCO is more appealing due to better phase noise performance, low RMS jitter and lower power consumption [[18],[66]]. Although it occupies larger area compared to that of ring oscillator [[21], [66]].

The paper is organized as follows; section II describes all the topologies of LC Voltage Controlled oscillator with the basic operation of LC VCO to generate stable oscillating frequency. Section III presents the preliminaries about phase noise generation in the LC oscillator with comparative analysis between different papers and section IV concludes the paper with remarks.

II. Prologue of LC Voltage Controlled Oscillator

A. Topologies of LC VCO

The basic topologies of LC Voltage controlled Oscillator are – NMOS only, PMOS only and complementary cross coupled LC VCO [[73]]. Each topology has better features compare to other two topologies in comparison with different features, according to the requirement of features the selection of the topology is done in different papers.

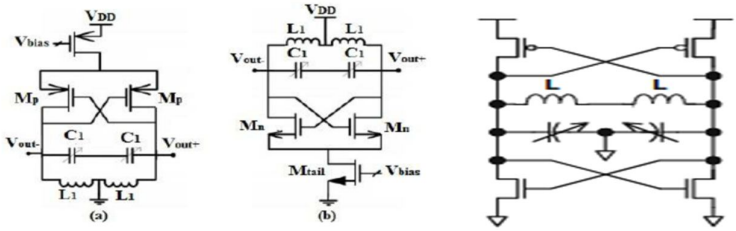

Figure 1: (a) PMOS only [[33]] (b) NMOS only Topologies [[33]] (c) complementary LC Oscillator [[66]]

As output voltage amplitude of oscillation is double compare to NMOS only structure due to PMOS pairs in the complementary LC VCO [[23], [24], [25]]. The complementary cross coupled structure offers higher transconductance at a given current, due to this it will result in faster switching of a cross-coupled differential pair of MOSFETs. The complementary structure also performs better rise time and fall time symmetry, which results in less up conversion of 1/f noise with lower frequency noise sources [[26]]. Different types of noises are present in the LC oscillator result in the phase noise is explained in literature [[27]]. The cross coupled transistor pair represents the one-port oscillator to provide a negative resistor to compensate for the energy loss in the LC tank in order to sustain the oscillation with the given frequency [[22]]. The Barkhuizen's Criteria is satisfied only at the resonant frequency of the oscillator, because the magnitude of the gain will become maximum and its phase will become zero when the LC tank is resonating. Therefore, if the (gm) transconductance of the amplifying MOSFET is designed large enough to ensure that its gain is larger than or equal to unity at the resonant frequency. This is the required condition to maintain the oscillation of the oscillator. With the noise at any suppressed frequency, the noise component will be amplified at the resonant frequency, passed further into the positive feedback loop of the oscillator and further amplified till the MOSFET enters into the saturation region so that the oscillation amplitude is maintained. This is the required condition to generate oscillation and maintain the oscillation of the LC VCO. The mathematical steps are derived in literatures with noise source model and steady state resonant model of LC oscillator [[22], [24]]. In the previous research papers, it is observed that LC oscillators have been designed with Bipolar transistors and phase noise performance is also

observed [[28],[29]]. For the completeness, it is also observed that in bipolar junction transistors (BJT) oscillators one another conversion of phase – delay modulation effect has been found [[36]]. LC oscillator with MOSFET has better phase noise and tunning range compare to Bipolar Transistors [[31]].

B. Preliminaries of LC Oscillator

The required and necessary condition for the LC oscillator to sustain oscillation is expressed by (1) [[67], [65]],

$$gm_{DEVICE} \geq \chi \cdot gm_{TANK} \quad (1)$$

Where, gm_{DEVICE} is the negative transconductance of the active device, gm_{TANK} is the transconductance of the LC-tank at the resonant frequency. χ is a constant, the literature [[67]] suggests that χ, an adjustable constant, is about to 3. The value is selected in between 3 to 5 according to design [[65]]. The power consumption of the VCO core is depending upon this value. The value of gmTANK should be minimum to reduce power consumption and gmDEVICE is reduced by reducing width or current of the device. The phase noise plays a critical and crucial parameter in VCO optimization. The phase noise is expressed in equation 2 [[65], [30], [32]]: the original lesson's equation, to find out oscillator phase noise.

$$L(\Delta w) = 10\log\left\{\left(1 + \left(\frac{f0}{2Q\Delta w}\right)^2\right)\left(1 + \frac{w0}{|\Delta w|}\right)\left(\frac{FkT}{2Pav}\right) + \frac{2kTRK0}{\Delta w^2}\right\} \quad (2)$$

Where, Q is the quality factor of the oscillator, k is the Boltzmann's constant, T is the absolute temperature,K0 is oscillator gain, P_{av} is the oscillation output power, F is the noise factor of the amplifier.

As shown from phase noise equation (2), Oscillator gain (K0) is directly and oscillator Q (TANK Q) is inversely proportional to phase noise. By selecting higher value of the Q phase noise can be reduced and higher value of oscillator gain degrades the phase noise. Here, it is observed from the equation, the trade-off is between power dissipation and phase noise.

For LC oscillator, Frequency tuning range is also very important parameter for the RF – ISM band frequency application. The oscillating frequency (fLC) is expressed in Equation 3:

$$f_{LC} = \frac{1}{2\Pi\sqrt{LC}} = \frac{1}{2\Pi\sqrt{L(Cvar+Cpar+Cmos}} \quad (3)$$

By above equation, it is reflected the trade-off between the frequency tuning range and the phase noise. The tuning range depends on the varactor characteristics as shown in Equation 4:

$$\text{Frequency Tuning range} = \frac{Cpar+Cvmax}{Cpar+Cvmin} \quad (4)$$

Here, Cpar-parasitic capacitance of the VCO circuit Cvar - varactor capacitance.

Wide Frequency tuning range can be achieved by large varactor capacitance and small value of parasitic capacitance [[65], [67]]. Accumulation nMOS varactors can be used because they have a good ratio of CV_{max}/CV_{min} [[19], [20]]. The parasitic capacitances come from the active devices and the substrate capacitances of the on-chip passives. Consequently, inductor is the heart of the LC oscillator. The LC oscillator is designed to operate in current-limited regime [[65]]. In this regime, the output differential amplitude (Vm) is approximately equal to the product of equivalent resistance and oscillator current. The equivalent resistance is derived by:

$$R_{eq} = \frac{W0LQlQc}{LCW0^2Ql+Qc} = W_0LQ_{tank} = \frac{Qtank}{W0C} \quad (5)$$

Here, Q_{tank} = (QL/QC), Ratio of Inductor Q and Capacitor Q, W_0^2= (1/LC).

Equation (5) shows some tradeoffs in value selection of L and varactors as capacitors. Larger value of inductor reduces LC tank loss and improves noise, but will occupy large area. However, as the varactor capacitance decreases and parasitic capacitance remains constant, reduces the tuning range of the oscillator. For proper design of LC oscillator, the correct value of L and C is selected to achieve all practical aspects.

C. Figure of Merit

In the design of LC oscillator circuits, designers often try to get phase noise and power consumption at the minimum limit for a given oscillation frequency. Since, this is the contradictory objective to get both at minimum level, this trade-off is reflected in the calculation of Figure-of- Merit (FOM) as follows [[30]],

$$FoM = L(\Delta w) + 10\log\left[\frac{P}{1mW}\left(\frac{\Delta w}{w0}\right)^2\right] \quad (6)$$

Where, w0 is the oscillation frequency, P is the DC power consumption, Δw is the offset output frequency, L(Δw) is the oscillator phase noise.

D. *Tail Current*

Tail current is the current generated by the biased mosfet or current source connected at the tail or top of the LC oscillator. The value of tail current is made large when the oscillator output voltage reaches its maximum or minimum value and when the sensitivity of the output phase to injected noise is minimum; the tail current is made small during the zero crossings of the output voltage when the phase noise sensitivity is large [[41]][[44]]. This is made possible by different techniques to shape the tail current and a LC oscillator with tail current shaping has a better DC to RF conversion and larger oscillation amplitude with equal power dissipation. This technique results in improvement of Phase noise.

E. Output Oscillator Voltage

In the steady-state, the LC oscillator's output voltages are

$$V_{o,p} = V_{dd} + A\cos(\omega_0 t) \quad (7)$$

$$V_{o,n} = V_{dd} - A\cos(\omega_0 t) \quad (8)$$

Where, A is the single-ended amplitude, Vdd is the supply voltage. To achieve better oscillator output voltage, LC oscillator in the current limited regime such that, cross coupled pair of mosfets do not enter into deep triode region. In that case, the voltage at the tail node (Vs) is approximately a sinusoid with frequency $2\omega_0$ [[41]].

$$V_s = A\cos(2\omega_0 t - \theta) \quad (9)$$

Where, as is amplitude of tail node voltage, θ is phase delay compared to the output voltage. The phase variations in the LC oscillator output in response to a noise current injected into the tank is a periodic function, often referred to as the impulse sensitivity function (ISF) [[50]].

In the table 1 survey on LC oscillator with different focus is listed. First column shows year of survey paper publication, second shows author and third column show purpose of the survey on which the review is focused. In the review paper [[51]] total 44 papers are compared with the parameters of oscillators - IC technology (nm), carrier frequency Fc (GHz), frequency tuning range ΔF (%), phase noise PN, power dissipation and figure of merit . From this comparative analysis table, the lowest value of FOMt, power and phase noise is found with wider range of tuning is searched. The concept of switched capacitors, switched varactors and current controlled block is explained with reference to architecture from literature.

TABLE I. SURVEY PAPERS ON LC OSCILLATOR

Year	Author	Details
2003	M. Rachedine et al [54]	Integrated CMOS LC Oscillators for wireless communications
2007	Owen C. et al. [[55]]	QVCO techniques for better Phase noise
2007	Peter K. et al. [[57]]	LC oscillator comparative analysis with techniques
2009	Chun H. et al. [[53]]	LC oscillator improving parameters
2011	Mahmoud M. et al. [[56]]	LC oscillator techniques for noise, tail current shaping
2012	M.A. Nandanwar et al [[52]]	LC oscillator survey for low power and phase noise
2015	V. Macaitis et al [[51]]	LC oscillator review with better values of parameters

In Review paper [[52]] the comparative analysis of different literature with parameters of LC oscillator – technology, power supply, oscillator frequency, tuning range of oscillator with voltage tuning range and power consumption is presented. Details of feedback model of oscillator, voltage-controlled frequency tuning and power consumption is given. Techniques covered in the paper are focused on low power with reduced phase noise. Presented first technique is nMOS only oscillator with decoupled capacitor and polysilicon resistor to reduce power as well phase noise. In second technique LC oscillator with nMOS current mirror as tail bias and pMOS current mirror as top biased with constant tail current is discussed. LC oscillator with pMOS current mirror results in lower phase noise is concluded. Next technique in the literature with double Pseudo resistance and parallel capacitors to achieve reduced power and last technique is QVCO with Reconfigurable LC tank is discussed. In Paper [[53]] discussion is focused on improving parameters of LC oscillators. Techniques of different LC oscillators are focused to reduce phase noise and power consumption of oscillator with detailing of Phase noise and Tuning range. In this paper phase noise contribution in the LC oscillator from the circuit components – MOSFETs, tail current source, Tank and thermal noise is discussed. Filtering technique with inductor and capacitor to reduce phase noise by cancellation of second harmonic, but at accost of large area is shown. Noise cancellation concept is shown by resistive and capacitive network is discussed, but architecture

suffers from reduced headroom and the need of dual threshold devices. Tail current noise is reduced by current switching but issue of increasing the supply or substrate noise. At last tuning range can be increased by resistively tuned variable inductor technique is shown from literature.

In paper [[54]] the different topologies of LC Oscillator nMOS only and Complementary oscillator from published literature is discussed with the techniques used to noise generated in oscillator. The effect of quality factor of inductor and capacitor as varactors is explained with reference. As high Q of Inductor is better choice for the LC oscillator, different approaches are listed in the paper. The key issues of quality factor of capacitors as varactor are listed with merits and demerits of techniques. Performance trends like: power consumption, FOM with effect of all topologies of LC oscillator, integrated inductor and filter used in techniques are discussed. At last system integration issues of VCO gain, tuning range and phase noise with tradeoff between them is discussed. In paper [[55]] different quadrature cross-coupled voltage-controlled oscillators (QVCO) based on LC tank resonators are compared on the basis of different topologies like: P-QVCO, Series coupled, Switched biasing, Transformer-based resonator. Detailing about basic operation of QVCO, phase and amplitude measurement and FOM is given. Comparative analysis between parameters of Qvco is shown in the table. In paper [[56]] different techniques of LC oscillator are discussed from literature focused on high quality factor, low noise for wide band wireless communication. The reported techniques are – nMOS cross coupled, CMOS cross coupled LC oscillator with tail biasing and pMOS cross coupled oscillator with top biasing. NMOS and PMOS cross coupled oscillators with current mirror tail and top biasing. Other techniques include resistor with tail bias and an NMOS-based varactor to generate differential in-phase CLK (I) and quadrature-phase CLK (Q) clocks are discussed. Comparative analysis between parameters of LC oscillator is shown in table. In paper [[57]] comparative analysis is done between different topologies of LC oscillators like: tail current biasing with current source, current mirror and QVCO. Concepts of PN, FOM, tail current shaping and tradeoff of LC oscillator are discussed.

III. Comparison of different Techniques to reduce Phase noise

A. Inductive degeneration

This paper [[34], [37]] presents two different techniques to reduce phase noise of LC voltage Controlled oscillator. The inductive degeneration and capacitive filtering techniques are used to reduce phase noise in the tail biased LC VCO. In this paper [[34]] as shown in figure 2, first VCO design is denoted by VCO1 and second is denoted by VCO2. Both Voltage controlled Oscillators - VCO1 and VCO2 have the same inductive and capacitive filtering techniques with on chip noise filter- L and C.

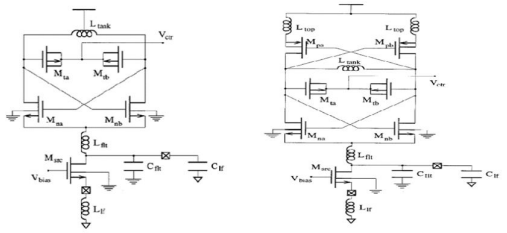

Figure: 2 (a) Capacitive and inductive filtering (b) Inductive degeneration with LC filtering

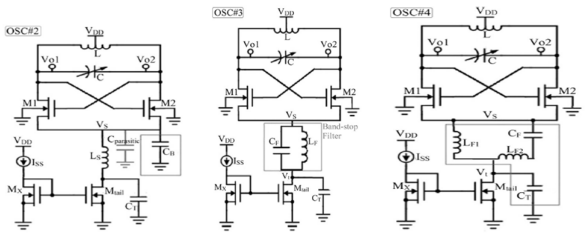

Figure 3. (a) Tail biasing – current source with LC filter (b) Tail biasing–current source with Band stop and C filter (c) Tail biasing – current source with 2 L, C and Ct filter

Here, two capacitors are used with inductive filtering. Where as in [[37]] only single capacitor serves the purpose. In addition to design of VCO2, an on-chip inductive degeneration, denoted by Ltop is added with pMOS cross coupled pair. It is observed from the comparison table that, the use of a single inductor in series with the common source of both pMOS switches results in a lower phase noise. This is because of an asymmetry between the nMOS and the pMOS cross coupled pair. The main advantage yielded by the inductive degeneration in VCO2, increase with lower offset frequencies, where the 1/f noise of the tail transistor totally dominates the phase noise [[34]]. In this paper simulation results are presented with on chip and off chip inductors, where best simulation results with off chip Inductor at a cost of high area requirement.

B. Inductive and capacitive Filtering

In this paper [[60]], as shown in figure 3, tail biasing is applied through the current mirror. To improve the phase noise of the LC oscillator, second harmonic noise reduction technique is used with proposed technique. In the

first technique, current mirror is connected to the nMOS oscillator through inductor, which is inductive filter and on capacitor is connected for noise reduction [[34], [35]]. Ct capacitor, parallel to current source is used to shape the tail current also improuves phase noise, called capacitive filtering [[41]]. In the second technique, LC filter – inductor and capacitor are parallely connected to each other and current mirror is coneected to the oscillator through LC filter, which is behaving like band stop filter. Now, in the third technique one more inductor is added in the bandstop filter, which is in series with capacitor and parallel to inductor1. This arrangment improuves 2nd harmonic noise, more matching between Vs node voltage and output voltage, which improuves phase noise, but high area requirement is here.

In table 2, comparative analysis of different LC oscillator is presented. First column shows year of publication and second column shows author name with reference no listed in references of the published literature. Here, survey of all the parameters – supply voltage, technology used for design, tuning frequency of the LC oscillator, frequency tuning range of the oscillator, phase noise, offset frequency, figure of merit (FoM) and power consumption are presented. From this table current scenario of the achieved results of parameter values are observed. Current technology and supply voltage value used for simulation is reflected. This comparative analysis will help researchers to achieve better results.

C. Tail biasing

It is observed form the literature [[23],[28]] that, the tail MOSFET used to balance the tail current in the oscillator may have a large impact on the generation of phase noise, often it is being the largest contributor, as techniques are used to reduce phase noise by tail current shaping. The high-frequency tail current noise occurred at twice the oscillation frequency is down-converted into phase noise by the hard switching oscillator [[34]]. This will contribute to the total phase noise of the oscillator [[48]]. In the paper [[50]], as shown in figure 4, three LC oscillators are simulated – simple LC oscillator, Conventional and proposed LC oscillator in this paper. In the below figure three circuits of LC oscillator is shown. In this paper, using the concept of Impulse Sensitivity Function (ISF) in Hajimiri's phase noise model, cascode tail biased LC oscillator is simulated with comparison to simple and conventional circuit.

In this oscillator two extra MOSFETs – Mx1 and Mx2 are added in series with tail bias mosfet – Mtail. With this two mosfets, tail current shape is made sinusoidal and tail current is made minimum at zero crossing outputs, made maximum at output peak points. Width of these mosfets is adjusted to get better phase noise. Value of Rdc resistor is selected large to reject tank loss and rejects noise injected in tank. Capacitor Csh is connected at the drain of tail MOSFET works as filter to reduce phase noise.

TABLE II. COMPARATIVE ANALYSIS OF LC OSCILLATOR WITH PARAMETERS

Year	Author	Supply Voltage	Tech.	Freq.	Tuning Range	Phase Noise	Offset Freq.	FOM	Power
2000	Bram D. et al. [[39]]	1.8V	0.65 µm	2GHz	1.79 – 2GHz	-125dBc/Hz	600kHz	-	-
2000	F. Svelto et al. [[43]]	2V	0.35µm	2.12GHz	1.8 -2.45GHz	-120.5dBc/Hz	600kHz	187.5	-
2001	C. Samori et. al [[31]]	2.5V	0.25µm	5GHz	4.20 – 5.05GHz	-94 dBc/Hz	100kHz	-	-
2001	Emad H. et al. [[35]]	2.5V 2.5V	0.35µm 0.35µm	1.2GHz 1.2GHz	-	-153dBc/Hz -152dBc/Hz	3MHz 3MHz		-
2002	Pietro A et al. [[34]]	1.4V 2 V	0.35µm 0.35µm	-	1.96 - 2.36 GHz 1.69 - 1.96 GHz	-103.5dBc/Hz -105.5dBc/Hz	100kHz 100kHz	-	-
2003	J. Gil et al. [[66]]	1.5 V	0.18µm	2.55GHZ	-	-119.2 dBc/Hz	1MHz	185.57	1.5mw
2004	Ming-J. et al. [[76]]	2.5V	0.25µm	-	0.8 – 3GHz	-91dBc/Hz	600kHz	-	10mw
2005	Babak S. et al. [[41]]	1.5V	0.25µm	2 GHz	1.755 - 2.123 GHz	-134dBc/Hz	3MHz	185.5	-
2006	Babak S. et al	1.5V	0.25µm	2 GHz	-	-117.5dBc/Hz	600kHz	-	-

	[[44]]								
2006	L. H. Lu et al [69]	1.8V	0.18µm	2.9GHz	500MHz-3GHz	-102dBc/Hz	1MHz	153	28mw
2007	A. Jannesari et al [[59]]	1.8V	0.18µm	1.8GHz	-	-130.3dBc/Hz	1MHz	-	-
2009	S. Cheng et al [[70]]	3V	0.35µm	1.5GHz	1.06 - 1.88GH	-116.1	1MHz	158.45	20.4mw
2010	Oleg N. et al. [[77]]	.5V	0.18µm	6.77GHz	-	-131.3dBc/Hz	3MHz	196.3	1.6mw
2011	Rafaella F. et al. [[71]]	1.2V	0.9 µm	2.16GHz	-	-106.2dBc/Hz	.4MH	183.6	.53mw
2011	Gauglitz et al. [[66]]	-	0.12-µm	4.5GHz	24%	-126.0dBc/Hz	1MHz	182	10mw
2014	Meng-t. et al. [[72]]	1.4 V.	0.18µm	4.94 GHz.	4.92 -5.7 GHz	-118dBc/Hz	1MHz	188.6	2.5 mW
2016	Kai Men [[63]]	1.8V	0.18µm	1GHz	6% Tuning	-120dBc/Hz	1MHz	179.8	1.03mw
2016	Xinyi W [[75]]	.5V	0.18µm	2.25GHz	11%	-119.4dBc/Hz	1MHz	181.3	3.23mw
2017	Bahram et al. [[50]]	1.8V	0.18µm	4GHz	-	-116.8 dBc/Hz	1MHz	188.9	1mw
2017	Bahram J et al. [[64]]	1.8V	0.18µm	10GHz	-	-107.8dBc/Hz	1MHz	186.2	1.45mw
2017	Bahram J [[60]]	1.2V	0.13µm	2GHz	-	-130dBc/Hz	1MHz	192.3	2.4mW
2017	Jafari B. [[64]]	1.8V	0.18µm	10GHz	-	-107dBc/Hz	1MHz	186.2	1.45mw
2018	Yin Z. et al. [[68]]	1.8V	0.18µm	-	1.126-2.713 GHz	-117.2dBc/Hz	1MHz	188.78	13.6mw
2018	Divyesh S. et al. [[73]]	1.8v	0.18µm	2.4GHz	2.4 – 2.48GHz	-124dBc/Hz	1MHz	187.25	2.86mw
2019	Pravinah S.et al. [[74]]	1.2V	0.18µm	2.45GHz	2.2 – 2.9GHz	-120dBc/Hz	1MHz	185.40	1.73mw

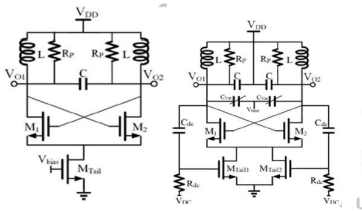

Figure: 4 (a) Simple LC Oscillator (b) Conventional LC Oscillator

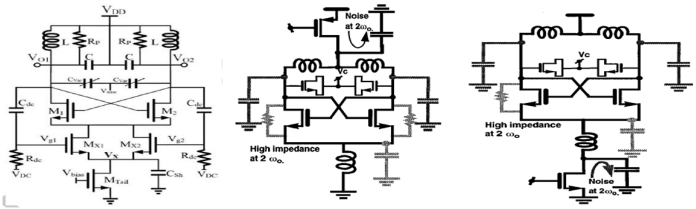

Figure: 5 (a) Top Biased LC Oscillator with Filter (b) Tail Biased LC Oscillator with Filter (c) Proposed cascode tail biased LC oscillator

Mx1,2 mosfets receive DC voltage fron Vdc source, which is adjusted at low voltage to keep oscillation constant and tail mosfet in saturation. Both Mx1,2 get AC voltage from capacitors Cdc connected at the output nodes of the oscillator and resistors. This proposed LC oscillator circuit results in better phase noise but high value of resistors and capacitors are required to fulfill the conditions. In paper [[63]] complementary LC oscillator with tail biasing is proposed. The presented techinque supress the phase noise contribution from the active devices. As the gate of biasing mosfet is coupled at drain through capacitor and bias voltage is applied through resistor. The cyclostationary noise ocured at the oscillator tail bias current source is reduced, reults in better phase noise [[63]]. In paper [[64]], conventional biasing is used. Two tail mosfets are use to bias the LC oscillator. Both the mosfets receive DC voltage from Vdc supply voltage through resistor and AC voltage through capacitor, which is connected at the output oscillator.

In paper [[73]], nMOS only, pMOS only and complementary LC oscillator is simulated and compared with the proposed one LC oscillator. Simulated these three oscillator has current mirror tail biasing techique to reduce phase noise. Compare to nMOS only and complementary oscillator pMOS only LC oscillator has better phase noise but larger power consumption. In this paper, proposed technique has current mirror tail biasing, but current mirror is connected with the vdd through mosfet. In the compared technique current mirror is resistor connected. The pmosfets cross coupled pair is connected with parallal mosfets, which are multifinger pmos. This technique

also results in reduced phase noise, as reduction in gate resistance will directly reduce thermal noise and results in better phase noise.

D. Top Biasing with filter

Conventional top biasing

The paper presented [[35]], as shown in figure 5, the top-biased differential LC oscillator is presented, where the current source is connected from the positive supply to the center tap of the differential inductor. If the junction capacitors to ground are ignored, these two oscillators are identical in that the bias current source-biased pMOS is in series with the supply-voltage source. Here, in comparison with the tail biased oscillator, the position of the basing is exchanged without affecting the circuit topology. However, top and tail biased circuits are different when the junction capacitors are included. The presented technique of top-biased oscillator offers better phase noise because of in the circuit the current source is placed in an n-well, rather than in the substrate, which reduces the substrate noise. Also, the top-biased oscillator up-converts less flicker noise compares to tail biased into phase noise. So, overall phase noise reduced. Also, noise filter circuit is added with top biased VCO, which shunts noise frequencies around the second harmonic to ground. But without inductive and capacitive filtering, this top biasing technique dose not result in better phase noise. In paper [[62]], top biasing is applied through current source and LC filter is applied to reduce phase noise. Here, 4 layers helical inductor is used to reduce area compared to other on chip inductor.

Top biasing with Current mirror & cascode

In this paper [[39]], top biasing with cascode tail current technique is presented. In this paper two nMOS LC oscillators are designed with top biasing. In comparison with paper [[40]], extra circuit – one capacitor, parallel to top biasing circuit and one extra mosfet, cascode with this top biasing circuit are added to common mode node of tail biasing to remove extra common mode variations. As the main parameter of VCO design is overdrive voltage Vgs -Vt, of nMOS. The selection of this voltage plays a role in flicker noise, output amplitude, power consumption and added parasitic of the nMOS. Here, in this technique the value of 1/f3 – phase noise factor is selected by keeping gm of nMOS constant. As a tradeoff, the value of Vgs – Vt is also chosen. This technique serves better phase noise by reducing flicker noise 1/f3 up conversion from tail current source at accost of extra supply voltage is required to bias the VCO.

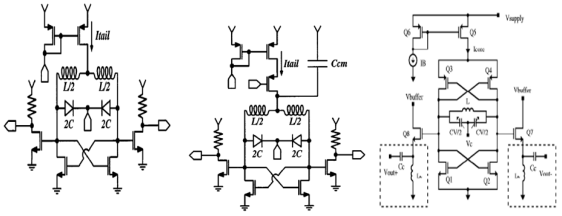

Figure: 6 (a) Top biasing [[39]] (b) Cascode Top biasing with C filter [[39]] (c) Top biasing with current mirror [[66]]

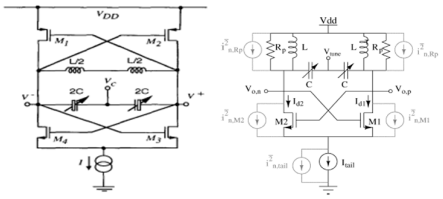

Figure: 7 (a) Tail biasing with current source [[43]] (b) Tail biasing with current source [[44]]

E. Tail Biasing with current source

In the presented paper [[43], [44]], as shown in figure 7, tail biasing is directly applied through current source to reduce the phase noise. As the direct current source applied at the nMOS cross coupled pair, injects current in the oscillator with proper amount and time, will minimize the ISF and reduces phase noise [[47]]. In [[44]] pulsating bias current is applied through the current source. Here, the proper value of current source is required to get better phase noise to fulfill practical requirements. An improvement in phase noise is achieved by making current pulses narrower, by reducing conduction angle. Here, an extra circuit is required to get pulsating current source.

F. Tail current shaping with current mirror

As shown in figure 5, presented in paper [[41]], represents nMOS oscillator with tail shaping circuit. In this arrangement current mirror circuit is used with current source biased with Vdd. The parallel/ shunt capacitor is used to shape the tail current. The capacitor value is also selected to get better tail current shape. Phase noise of the oscillator is reduced by entering tail current at proper time into the tank, when ISF is minimum. Simulated result values are given in the table. Compare to differential colpitts oscillator [[42]], this technique gives better results. This technique reduces power, phase noise and FOM but requires current source of Iref value. In the

[[44]] in place of constant current applied at the tail bias, pulsating current – narrow current pulses are applied at tail bias. All the mathematical steps to get tail current and output voltage equations are derived. In this arrangement better phase noise is achieved at a cost of extra circuit of peak detector and buffer to get pulsating current, connected at the gate of mosfet in the current mirror.

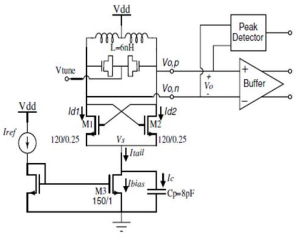

Figure 8: Tail current shaping with current mirror

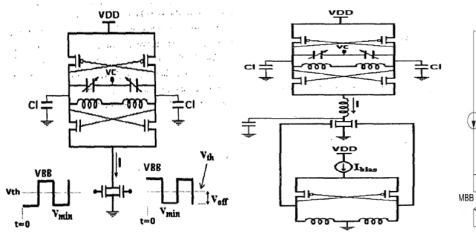

Figure 9. (a)Tail current switched biasing [58] (b) Tail current complementary biasing [58] (c) Tail current switched biasing [59]

G. Tail current switched biasing

In this [[58]] paper, flicker noise generated by the tail transistor is reduced by switched biasing. The tail current is composed of two mosfets having their drain connected with LC oscillator thtrough inductive filter and gates connected to the output of another LC fixed frequency oscillator as shown in figure 9 (b). Capacitive filtering is applied to reduce second harmonic noise. The concept of 1/f noise reduction through switched bias [[49]] is applied though the mosfets connected at the tail of oscillator through drains. Gates of the mosfets receive voltages in the form of pulse train as shown. As a result, LC oscillator receives pulsating current. This technique reduces phase noise by reduction in 1/f noise but double area required for the circuit. In the paper [[59]] switched biasing technique is proposed. Tail bias is connected at the drain of two mosfets and gates are connected with the gate and drain of MBB mosfet, where gates are received switching from the external circuit. Drain of Mbb mosfet is biased to Vdd through current source. This technique reduces phase noise by reduction in 1/f noise but extra switching circuit is required. In paper [[61]], noise cancellation technique is introduced with switched tail biasing. Here, switching is applied at the gate of the mosfet which is in parallel with the current source with drain and source. Extra RC network is connected- Rac and Cac, which behaves as high pass filter to improve phase noise. Biasing node is connected to vdd through R1 resistor and switch through capacitor Cac. Here, Rac resistor connected with Vbais and this voltage is generated by replica bias circuit as shown in this paper. This technique improves phase noise but involves more extra circuits.

H. Other Techniques

In [[46]] with the circuit of simple MOS differential LC oscillator, how varactors convert AM noise into FM is explained with derivation and effect of control voltage on the varactors to generate frequency tuning is derived and simulated with the effect on phase noise. Paper [[46]] presents the switched capacitive tuning to reduce Phase noise. Here, weighted capacitor array of Mos varactors are used in parallel with three Metal layer Inductor. The technique can increase the tuning range of the oscillator and results better phase noise.
In this paper [[68]] active inductor is used in the LC oscillator to solve the problem of high area requirement or off chip inductor. In this paper differential active inductor is used. Complementary LC oscillator is used with extra components including capacitors, current source and mosfets are aimed to get higher output power.

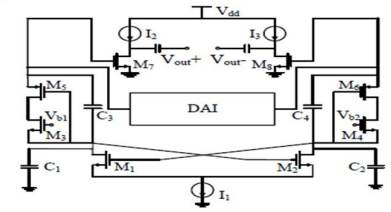

Figure 10. Active Inductor- CMOS LC VCO [[68]]

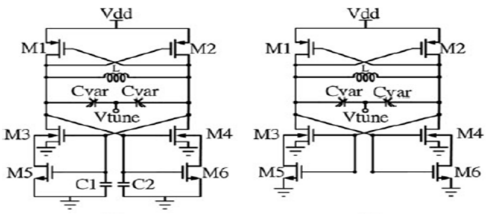

Figure: 11 (a) Body biased Q enhancement LC VCO (b) Body biased LC oscillator

In paper [[69]], tunable active inductor is presented to increase tuning range and decrease area as well phase noise. Compare to [[69]], in [[68]] less power consumption and better phase noise is achieved. But active

inductor technique has drawback of high-power consumption is to get less area and phase noise. In paper [76], high Q active inductor is used for constant power consumption and wide tuning range. High Q of the inductor results in better phase noise. In this technique a feedback resistor is used to improve the Q value of the inductor, which is used to tune the inductor in the proposed circuit.
Another approach is shown in [[70]], resistively tuned variable inductor is proposed. In this technique issue of high-power consumption is there to achieve better phase noise and tuning range. In paper [[74]], conventional high swing complementary class- C oscillator is explained and simulated. Proposed technique has extra circuits of auxiliary gm class B and tail biasing with pMOS connected with resistors and capacitor. Resistors are connected with Vbias and capacitor used as capacitive source degeneration to improve phase noise. This technique improves phase noise but required extra circuits to fulfill the requirements. In paper [[77]], new resonator technique is introduced to get lower phase noise. In this paper serial resonators are connected with this main resonator circuit. Here, main LC tank circuit is connected in parallel with other two pair of inductor and capacitor. This technique reduces impedance of the main resonance and high Q value reduces the phase noise. Serial resonators are designed with bonding wire inductors to reduce the electromagnetic interference. This oscillator is digitally controlled and digital interference is improved by this technique. In paper [[75]], pMOS only topology is used as LC oscillator. Here, LC tank circuit is formed with AMOS varactors as capacitors and a symmetric three-port inductor. The ac coupling capacitors and resistors are used here to control the bias current, this technique is used at the gate of the mosfet. In addition to this technique, a back gate bias voltage is connected to reduce threshold of mosfet and results in increased transconductance. Output voltage of the oscillator is collected from the inverter amplifiers are behaved as buffers to get better output voltage. In this paper, [[71]] an LC voltage-controlled oscillator (LCVCO) is designed to optimize the methodology based on the gm/Id technique and on the exploration of all inversion regions of the mofet (MOST) is presented. As asolution of tradoff between phase noise and current consumption, this technique is introduce to get better phase noise as well power consumption. In this paper, [[72]] a low-power CMOS LC voltage-controlled oscillator (VCO) with body-biasing technique is introduced. Low-phase noise is achived by Q-enhancement techniques. A self-body biased circuit is shown is below figure that can reduce power consumption. In this paper derivations of the Q-enhancement and reduction in the phase noise of the circuit are also discussed. In paper [[72]], complementary LC oscillator with body biased technique is introduced. From the above circuit, nMOS cross coupled pair is connected thourgh the substrate with the drain of biasing mosfets and source of nMOS mosfets are connected to ground. Here capacitors as shown in figure, connected between gate and source each of biasing mosfet. These two circuit connection technique imoruves phase noise, but layout and fabrication of this circuit requires extra steps to create body bias.

IV. Concluding Remarks

The review paper presents comprehensive survey of LC Voltage controlled oscillator for RF – ISM frequency band applications with different techniques to reduce phase noise. Although, paper also provides details of different three topologies of LC VCO with the improved parameters like - FOM, power consumption, tunning range. In the comparative analysis it is also reflected that the technology used for the design of oscillator is reduced and scaled power supply with better results can be achieved. This survey started with conventional LC voltage-controlled oscillator with fundament features. The methods and techniques with different topologies of VCO to get better phase noise including the issues of FOM, power consumption and tuning range are discussed with pros and cons of presented techniques. As reviewed in the paper, nMOS only and complementary oscillator topologies are more used compared to pMOS only topology. The techniques to improve phase noise,
Tail current biasing techniques are more used with inductive and capacitive degeneration techniques are used, but inductive degeneration occupies more area, Inductive and capacitive filtering techniques discussed here can be used with other techniques to improve phase noise, but again inductive filtering has demerit of area. Compare to top biasing technique, tail biasing technique results in better phase noise, Tail biasing is applied with direct current source, current mirror, biased mosfet, cacode tail biasing. Tail current shaping techniques result in better phase noise and Switched biasing technique improves result of phase noise but involves extra circuit for switching pulse generation. Active inductor technique has demerit of high-power consumption and Body biased technique requires special fabrication steps. Switched capacitor as well tunable inductor techniques are more focused on frequency tuning range, but with improvement in Q value of the tank technique results better phase noise.
The techniques reviewed in this paper used for LC oscillator to improve phase noise are highly depend upon the application and requirements of major parameters.

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