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Review on Low-Power and High-Speed Dynamic Comparators for Precise Applications

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***Abstract*— A major advancement in the design of high-speed, low-power electronic systems are the dynamic latching comparator. Because of its self-calibrating architecture, there is no need for additional parts, guaranteeing efficiency and simplicity. It achieves a small size with low offset voltage by using cutting-edge complementary metal oxide semiconductor (CMOS) technology. An inventive capacitive digital to analog converter (DAC) structure lowers overall capacitance and saves energy, while the focus on balanced routing improves stability. Speed and power efficiency are further increased by the suggested switching mechanism and a two-stage comparator with a PMOS latch. This article focuses on the latest advancements in the architectures of high-speed dynamic comparators and their metrics. Review reveals that two stage dynamic comparators with an appropriate clock signal and PMOS technology perform better than other types of comparators.**

***Index Terms*— Comparator, Low-Power, High-Speed and Dynamic Comparator.**

I. INTRODUCTION

The analog to digital converters or simply ADCs plays a very critical role in modern day devices, particularly in digital electronics and in the interfacing between analog and digital systems. ADCs are important components as they convert the analog data into digital data which can be further processed, manipulated, or stored as per requirement. Most of the real-world signals including temperature, light, pressure, sound is all continuous and analog in nature. ADCs converted these data from analog to discrete digital data which are processed and manipulated by devices such as microcontrollers and signal processors. They facilitate the conversion of physical quantities into discrete data that makes it more accurate and reliable in representation. ADCs are the fundamental components of the communication systems, sensors, and various measuring devices. In consumer electronics specifically, in smartphones, digital cameras, audio interfaces or wherever the digital signal processing is required. In industries ADCs are useful in automation, control systems and instrumentation of data acquisitions and analyzers [7].

Analog-to-digital Converters (ADCs) come in a variety of forms, each having unique uses and operating principles. With the use of a DAC and comparator, successive approximation ADCs (SAR) use a binary search technique to effectively estimate input voltages. Oversampling and noise shaping are used by delta-sigma ADCs to achieve high-resolution conversions. Pipeline ADCs expedite the conversion process by segmenting it into phases. While flash ADCs often have lesser resolution, they allow fast conversions using parallel comparators. For precise readings, Dual-Slope ADCs measure input voltage by discharging at a predetermined rate and integrating over a

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predetermined amount of time. Time-to-digital converters (TDCs) are useful for accurate time measurements since they transform time intervals into digital form. Charge-Redistribution ADCs employ numerous sub-ADCs to improve resolution, whereas interpolating ADCs use capacitor charge redistribution for conversion [7]. The type of ADC to choose depends on the needs of the application. Comparator architectures differ in terms of performance and design. Although they are straightforward, single-stage comparators have trouble accurately resolving small input variations. Although they can be more sophisticated, two-stage comparators increase accuracy. Though quick, dynamic comparators require a lot of power. Although pipelines comparators are ideal for high-speed applications, they are complex and prone to inaccuracy. Latch comparators give up speed for simplicity and power efficiency. They can be complicated, track-and-hold comparators provide a consistent output during sampling. Flash comparators require sophisticated circuitry and significant power consumption, but they are fast and have great resolution. Trade-offs between speed, accuracy, power, complexity, and particular applications requirements must be considered when selecting a comparator [7].

Compared to alternative comparator architectures, dynamic comparators are superior in several ways. They are incredibly fast and provide quick signal processing, which is essential for data collecting or high-speed communication systems. Because of its ability to precisely handle smaller input voltage variations, and the design allows for higher resolution, making it perfect for accurate measurements in instrumentation systems or sensor networks. Even while they may require more power to operate, they frequently continue to operate with energy efficiency, which is crucial in applications where power is limited. Furthermore, dynamic comparators guarantee improved comparison accuracy by minimizing offset errors through design features like dynamic preamplification. Dynamic comparators are a recommended option for high-performance systems due to their ability to handle high-frequency signals efficiently, which further strengthens their eligibility for applications dealing with rapid data processing or RF signals.

II. Literature Survey

Razavi et al. [1] explored precision techniques for comparator design in high-performance analog-to-digital converters (ADCs) with parallel conversion stages. Key findings include circuit designs achieving 12-bit resolution in BiCMOS and CMOS technologies. The BiCMOS comparator achieves a 200 pV offset at 10 MHz with 1.7 mW power dissipation, while the CMOS comparator achieves less than 300 pV offset at up to 10 MHz with 1.8 mW power dissipation. The conclusion emphasizes the integration of bipolar and CMOS devices for high-performance analog circuit design. Overall, the paper contributes to enhancing ADCs by addressing trade-offs in comparator design for optimal speed, resolution, and power dissipation.

Hong et al. [2] addressed the collaborative project led by Hyeok-Ki Hong addresses power consumption challenges in time-interleaved ADCs. The team introduces a multi-step hardware-retirement (MSHR) technique to simplify complex logic and DACs in high-resolution ADCs. They present a low-power 2.6b/cycle-based SAR ADC implemented in 45nm CMOS, showcasing efficiency improvements. The ADC achieves competitive dynamic performance with 15.4mW power dissipation at 1.7GS/s. The MSHR technique proves effective in reducing power consumption, making the project valuable for high-speed, high-resolution ADC design.

Ragab et al. [3] briefly introduced a novel digital background calibration technique for pipelined ADCs. The method leverages comparator decision time to correct interstage gain errors and capacitor mismatches. Notably, it does not modify the original analog signal path, offering flexibility in input signal swing and bandwidth. Simulations on a 12-bit pipelined ADC demonstrate substantial improvements in signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR), enhancing them from 44 dB and 48 dB to 72 dB and 86 dB, respectively. That technique achieves fast convergence with an SNDR convergence time of less than 3 × 10^6 cycles. The approach is characterized by low analog complexity, making it a promising solution for power and area efficient pipelined ADC design.

Khorami et al. [4] introduced a low-power, high-speed two-stage dynamic comparator in 0.18 μm CMOS technology. By using PMOS transistors and a unique activation sequence, the circuit achieves controllable pre-amplifier gain while minimizing power consumption. Simulation results show a 50% reduction in power consumption and a 210 ps decrease in comparison time compared to conventional circuits, maintaining the same offset voltage budget. The design offers efficient flexibility, allowing the offset voltage and power consumption to trade with speed and addresses the need for a fast, low-power comparator in high-resolution applications.

Cho et al. [5] presented a 10-bit, 20 Samples/s pipeline ADC in 1.2 μm CMOS, achieving 35 mW power dissipation. Key features include digital correction for dynamic comparators and optimized capacitor scaling. With switched capacitor circuits at 3.3 V, the ADC exhibits 0.6 LSB INL, 59.1 dB SNDR at 100 kHz, and 55.0 dB

SNDR at Nyquist sampling (10 MHz). Operating with a 1 V differential input range, 220 pV input-referred RMS noise, and below 3 mW power dissipation at 1 MS/s with 58 dB SNDR, this design is suitable for low-voltage, low-power video-rate applications.

Figueiredo et al. [6] briefly addressed kickback noise in latched comparators, critical for analog-to-digital converters. Reviewing existing solutions, it introduces two novel techniques demonstrated through HSPICE simulations in 0.18 μm technology. Despite the typically higher kickback noise in power-efficient comparators, the proposed methods significantly reduce it without a substantial increase in power dissipation. This work contributes insights to enhance latched comparator performance in analog-to-digital conversion systems.

Khorami et al. [7] suggested method for dynamic comparators technique, the pre-amplification stage is stopped without influencing the comparator's dynamic behavior. This considerably lowers the pre-amplifier stage power consumption, which accounts for a large amount of the overall power consumption. This method reduces overall power consumption by more than 50%, according to simulations conducted across multiple comparators. The effectiveness of this circuit technique in lowering power consumption without sacrificing speed or offset voltage is emphasized in the conclusion. The suggested method shows a possible decrease of up to 56% in power consumption, as confirmed by simulation findings, while having a negligible influence on speed by terminating the pre-amplifier stage when it is not needed.

Abbas et al. [8] proposed a design for an on-chip high-speed clocked comparator utilizing 65nm CMOS technology, specifically suited for digitizing high-frequency, low-swing signals. The comparator uses ten MOS transistors in total across its two stages (regenerative and amplification). In addition, the study presents an economical method of determining the comparator's maximum clock speed and offers a comparison with a traditional reference design. The suggested circuit outperforms the reference circuit at comparable power consumption for high frequencies, operating 31% faster on average. The paper also presents a new low-cost technique to determine the highest clock frequency that can be used with on-chip clocked comparators, thereby reducing the need for expensive testing apparatus that is usually needed for high-frequency signal measurements.

Holleman et al. [9] presented a low-power, high-precision dynamic comparator with a time-domain bulk-tuned offset cancellation technique. This novel technique minimizes additional power consumption and delay while eliminating input-referred offset significantly. Ten circuits worth of results demonstrate a significant improvement, with the offset standard deviation falling from 5.415 mV to 50.57 μV—a factor of 107.1. The cancellation technique guarantees quick convergence over a range of common-mode inputs and shows no discernible offset or noise introduction. Together with the offset cancellation circuitry, the comparator uses 4.65 mW, or 23 pJ per comparison, when operating at 5V and 200 kHz clock frequency. The low-power, high-precision comparator presented in this study has fast convergence, fine resolution, and low power consumption, making it suitable for high-speed applications leveraging process scaling advantages.

Amico et al. [10] addressed the shortcomings of calibration techniques seen in high-speed low-resolution ADCs by presenting a 5-bit 1-Gs/s Folded Interpolated ADC in 90- nm CMOS technology without calibration. Power consumption is greatly decreased by employing dynamic comparators and a folded interpolated architecture. Bigger transistors guarantee intrinsic device matching, and higher kickback noise on comparator inputs is reduced by an improved dynamic comparator. The ADC uses 7.65 mW to achieve 4.3b-ENOB and 260 MHz effective resolution bandwidth when operating at 1.2 V. By doing away with the requirement for calibration, extra circuitry, and dead time, this method provides a high-performance ADC design that is more efficient

Gao et al. [11] introduced a novel single-stage dynamic comparator that outperforms earlier dynamic comparator designs and provides a broad input common-mode range. Compared to previous models, this new comparator exhibits over 1.2 times faster speed and less than 80% power consumption while keeping input-referred noise and offset levels constant. It performs better than traditional dynamic comparators, as noted in earlier research showing the quickest comparison speed and least amount of power consumption. Its offset and input-referred noise are marginally greater than those of[, but they are still similar to those of. Among all the dynamic comparators that have been examined, this comparator stands out for having the widest practical common-mode range, which can even handle voltages higher than the power supply. It is extremely efficient due to its superior speed, power consumption, and common-mode range

Hassanpourghadi et al. [12] presented in their paper and is intended for use with ADCs. Traditional comparators have internal circuit mismatches that force trade-offs between power, offset, and speed. By utilizing a two-stage, two-phase methodology, this innovative comparator addresses these issues and lowers the offset voltage brought on by these mismatches. Its efficacy is confirmed by thorough statistical analysis and Monte Carlo simulations conducted across a range of process corner cases. This proposed design shows at least a threefold decrease in offset voltage and a significant 44% reduction in power consumption when compared to typical comparators in 180 nm

and 90 nm technologies. These outcomes confirm this new dynamic comparator's suitability for high-speed ADC applications.

Miyahara et al. [13] postulated a low-offset, low-noise dynamic latched comparator with self-calibration, achieving a 1.69 mV offset at 1 sigma and 0.6 mV input noise. The self-calibrating technique eliminates the need for amplifiers, reducing power consumption to 40 μW/GHz. The comparator, requiring only one phase clock, demonstrates superior performance compared to conventional designs. Experimental results in 90 nm 10MP CMOS technology confirm the effectiveness of the proposed calibration method, making the comparator suitable for deep sub-micron CMOS applications with minimal area and low offset voltage requirements.

Nikoozadeh et al. [14] explored load capacitor mismatch impact on the offset of a regenerative latch comparator in 0.18-μm CMOS. Analytical models, compared with simulations, highlight that a 1 fF imbalance can lead to significant millivolt offsets. The study underscores the need for balanced routing and operating the latch close to inverters' thresholds. Strategies like introducing deliberate capacitance mismatch are suggested for effective offset mitigation.

Sendi et.al. [15] presented a novel switched-capacitor Digital to Analog Converter (DAC) employing a ladder of series capacitors. The DAC features a correction phase that enhances precision, making it mismatch and process independent. The proposed structure ensures accurate voltage division without extra power consumption. Simulation results affirm the mismatch independency of the DAC, showcasing its potential for ultra-low power and high precision applications.

Chang et al. [16] introduced an area-efficient tri-level switching scheme for SAR ADCs, utilizing a new quarter-reference voltage (Vaq) and reusing LSB capacitors. The proposed scheme achieves an 87.5% reduction in total capacitance and a 96.48% decrease in switching energy compared to conventional methods. It ensures good accuracy, making it suitable for small-area and low-power applications

Yazdani et al. [17] proposed an ultra-efficient switching method for successive approximation register ADCs, optimizing the sampling of input signals to reduce switching energy. By employing a single reference voltage (Vq = Vref/4) and lowering the supply voltage, the method achieves a 99.41% reduction in switching energy and a 50% decrease in DAC area compared to conventional methods. The DAC's precision remains unaffected by the supply voltage, making it suitable for high-resolution, low-power applications.

Razavi et al. [18] postulated the Strong-ARM latch, widely employed as a sense amplifier or comparator, is known for its use in the Strong-ARM microprocessor. Three key advantages of this circuit are its zero static power consumption, direct production of rail-to-rail outputs, and a low input-referred offset primarily from one differential pair. This study explores the circuit and its properties, acknowledging its significance and versatility in various applications.

Dubey et al. [19] presented a low-voltage, high-speed CMOS Double-tail Dynamic Comparator (DTDC) designed for efficient data conversion. Simulations in 45 nm CMOS technology show a delay of 166.29 pS and power dissipation of 2.3 μW at a 0.8 V power supply. The proposed DTDC outperforms existing designs, being 76% faster than one and 40% faster than another, with superior energy efficiency, reduced kickback noise effects, and significant area savings. It is well-suited for modern portable and high-speed communication systems.

Dastjerdi et al. [20] introduced a low-power, high-speed two-stage dynamic comparator utilizing PMOS transistors at the input. The second stage is activated with a controlled delay, enhancing pre-amplifier gain, while the first stage is subsequently turned off to minimize power consumption. Simulation results in 0.18 μm CMOS technology demonstrate a twofold reduction in power consumption and a 210 ps improvement in comparison time, maintaining the same offset voltage budget as conventional circuits. The comparator achieves a 76.2% speed boost, making it suitable for high-speed, high-resolution applications with acceptable offset voltage.

Lotfi et al. [21] addressed the demand for ultra-low-power, area-efficient, and high-speed analog-to-digital converters, emphasizing dynamic regenerative comparators for enhanced speed and efficiency. The paper provides a detailed delay analysis of dynamic comparators, yielding analytical expressions to guide designers in exploring trade-offs. A novel dynamic comparator design is proposed, modifying a conventional double-tail comparator to achieve low-power, fast operation, even in small supply voltages. Post-layout simulations in a 0.18 μm CMOS technology validate the analysis, demonstrating significant reductions in power consumption and delay time. The proposed comparator achieves maximum clock frequencies of 2.5 GHz and 1.1 GHz at supply voltages of 1.2 V and 0.6 V, consuming 1.4 mW and 153 μW, respectively, with a 7.8 mV input-referred offset standard deviation at 1.2 V supply.

Sharifkhani et al. [22] introduced a method to significantly reduce the power consumption of two-stage dynamic comparators without affecting their dynamic behavior. The approach targets the excess power consumption during the latter part of the comparison when additional pre-amplification gain is unnecessary. By adding two transistors

in series with the current source of the pre-amplifier stage, the proposed method achieves a power consumption reduction of 30% to 58%. Both post-layout simulations and analytical derivations confirm the effectiveness of the method, showcasing its potential for enhancing the efficiency of dynamic comparators across various implementations.

Namgoong et al. [23] discussed the sequential approximation register (SAR) ADCs power consumption bottleneck by theoretically examining the best comparators to achieve the required overall performance at the lowest possible power levels. The power allotted to each bit step need not be uniform, according on the SAR ADC mathematical model that is being provided. The best possible distribution of the comparator power budget across all bit stages is achieved by formulating an optimization problem. According to simulation studies, using alternative comparator power allocations can result in power reductions of up to 50% and 60% for 10-bit and 12-bit SAR ADCs, respectively. The study also examines comparator noise allocation, demonstrating that near-ideal performance in 10-bit ADCs may be achieved with two comparators, resulting in a 40% reduction in power consumption. Significant power savings are provided by the suggested method, particularly in high-resolution SAR ADCs.

Rabiei el al. [24] introduced a novel high-speed, low-power dynamic comparator design using a cross-coupled mechanism, targeting applications like bio-implantable circuits and analog-to-digital converters. Through simulations in a 90-nm CMOS technology, the proposed comparator achieved impressive results, including a 3 GHz maximum clock frequency, 6 nW power consumption, and 79 ps delay time, showcasing significant advancements in power efficiency and speed compared to existing designs. These findings highlighted the potential of the proposed comparator to enhance the performance of various applications, particularly in bio-implantable devices, by enabling faster and more energy-efficient analog-to-digital conversion.

III. Performance Summary And Comparison

The numerous recent developments in the design of dynamic latch comparators for DAC techniques are displayed in Table 1.

TABLE I. COMPARATOR METRICS PERFORMANCE

References	[1]	[2]	[4]	[5]	[9]	[10]	[16]	[20]	[21]	[24]
CMOS Technology	1um	65 nm	180 nm	1.2 µm	0.5um	90 nm	0.13 µm	45nm	180 nm	90 nm
Supply Voltage [V]	5	1.2	-	-	-	-	1.2	0.8	1.2	1
Power	1.8mW	44.6 mW	435 µW	-	-	2.2 mW	0.82 mW	2.3µW	-	6.19 nW
Area	50 x 250 um^2	0.18	-	3.2 × 3.3	64k um^2	0.0165	0.052	2.92 $µm^2$	28µm× 14µm	-
Offset Voltage	300uV	-	2.5 mV	-	-	-	-	-	7.8 mV	-
Clock Frequency	-	-	2.1G Hz	-	3.3M Hz	1.75G Hz	-	0.25G Hz	-	2.5G Hz
Resolution	-	11	-	10	-	-	10	-	-	-
Input Capacitance	40fF	-	-	1pF	-	-	2.5pF	-	-	-
SNDR[dB]	-	50.9	-	59.1	-	29.9	57	-	-	-

IV. Conclusion

The dynamic latched comparator represents a notable advancement in low-power, high-speed design, featuring a self-calibrating architecture that eliminates the need for additional components. Utilizing deep sub-micron CMOS technology, it achieves a compact size with minimal offset voltage. Emphasizing well-balanced routing addresses load capacitor mismatches, enhancing overall stability. The innovative capacitive DAC structure reduces

capacitance and optimizes energy consumption. The suggested switching process for SAR ADCs significantly improves power efficiency. Introducing a two-stage dynamic comparator with a PMOS latch enhances speed while reducing power consumption. The self-biased DTDC design showcased in this comparator contributes to achieving higher conversion speeds with lower power dissipation, marking progress in the evolution of more efficient electronic systems.

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