Grenze International Journal of Engineering and Technology, June Issue

Exploring Full Adder Design Options for 90nm Technology Node: An In-depth Performance Analysis

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***Abstract*— This study presents a comprehensive examination of the various full adder circuit designs, which form the core of many high computational arithmetic logic circuits in low voltage low power VLSI designs. Any researcher's ultimate objective is to increase speed and efficiency while minimizing the circuit's need for space by optimizing its performance. In this paper, the benefits and drawbacks of several design techniques employed in the development of the full adder have been examined. Various state-of-the-art full adders at the 90nm technology node have also been compared and analyzed.**

***Index Terms*— Low-voltage (LV) Low-power (LP), Full adder (FA), XOR/XNOR cell, CMOS, Complementary pass-transistor logic (CPL), Pass transistor logic (PTL).**

I. INTRODUCTION

With the evolution of portable electronic gadgets and transistor scaling, the designing of low-power and high-performance microelectronic circuits has surged immensely. Modern digital signal processors, image and video processing operations or any application-specific circuits seek the efficient usage of arithmetic circuits for the execution of the required computations including convolution as well as advanced filtering operations. As arithmetic circuits play an essential part in VLSI circuits and systems, the full adder is the most elementary cell incorporated in all the stated devices [1]. One-third of the power in high-performance microprocessors is consumed by arithmetic circuits [2].

The development of various logic styles has improved the arithmetic cells as well as enhanced the performance and reduced the cost of the integrated circuits. Minimization of supply voltage is a prominent method to scale down the power consumption, but it blights the driving capability of cells and reduces the circuit speed. Due to the substantial usage of full adders, their enhanced performance will optimize the Arithmetic and Logic Unit (ALU) in the microprocessors and will boost the performance of the entire system [1]-[3]. To design a full adder, several papers have been presented with various CMOS logic styles [2]-[4]. With similar functions but distinct internal logic structures, these logic styles yield variations in power consumption, propagation delay, wiring complexity and size of the circuits. They can be analyzed as classical design adders or hybrid design adders.

As per the classical approach, the FA is designed in a single module by making use of the MOS transistors. A substantial example of this style is the complementary CMOS(C-CMOS) FA [2]. It includes 28 transistors for designing pull-down and pull-up networks of the full adder and yields full-swing outputs and robustness against transistor sizing and voltage scaling. Each input is connected to the gates that consist of at least an nMOS and a pMOS transistor. Thus, the speed of the adder is compromised due to high-input capacitance.

The hybrid design style divides the structure of the FA into three modules [3], [5], [6]. With the help of module 1,

Grenze ID: 01.GIJET.9.2.8_2

the simultaneous generation of full-swing XNOR and XOR outputs of the input signals takes place. As Module 1 drives the other modules, the driving capabilities of the XOR-XNOR signals ought to be remarkable. With the help of Module 1 and Cin, Module 2 and Module 3 generate the sum and carry outputs (Cout), respectively. This approach has the edge over the classical style as the optimization of the modules is feasible at the individual level. Moreover, the reduction in the internal power dissipating nodes is caused by the decrement in the number of transistors. FA has been realized with the hybrid approach by researchers to optimize its performance without trading its output.

As the performance of hybrid FA is substantially affected by the performance of the XOR-XNOR circuit, various approaches to design the XOR-XNOR circuit have come up recently. Radhakrishnan had designed an XOR-XNOR circuit using six transistors. His circuit consists of two complementary feedback transistors for restoring the weak logic in complementary output nodes (XNOR and XOR) when both the inputs consist of the same values i.e. 11 or 00 [7]. This approach undergoes extensive delay for similar inputs as output reaches the final voltage level in two steps. The Chang et al overcomes the slow response by using two additional pMOS and nMOS transistors at the XNOR as well as XOR output nodes, respectively [4]. This approach leads to full output swing as well as good driving capability. At XOR-XNOR output nodes, an extra parasitic capacitance is added by the cross-coupled structure.

The XOR-XNOR circuit was further improved by Naseri and Timarchi through the usage of 12 transistors [8]. The power consumption of this circuit is low with better delay performance. It consists of an external inverter and thus its performance can be boosted by the elimination of the inverter. Kandpal et al improved the delay performance by designing a 10-T XOR/XNOR cell [9]. This low-power design is based on CPL logic and cross-coupled structures. It generates XOR-XNOR output simultaneously. Garg et. al. [10] suggested a 2-input XOR gate for improving noise and leakage power performance based on Foot Driven Stack Transistor Domino Logic (FDSTDL). Here the transistor count remains high. Beitollahi and Hajiqasemi [11] circuit consists of a MOSFET count lesser than conventional single rail and dual Rail XOR domino gates.

II. Literature Review Of Various Full Adders

With numerous adder cells being developed over the decades, their implementation and simulation in a common environment are advantageous. This paper presents a comparative analysis of the design of a full adder implemented using different techniques.

A. CPL Adder

Here the circuit uses the CPL technique to construct a full adder with a good voltage swing using involves 32 MOS transistor. High switching activity is caused due to high transistor count that leads to huge power loss. Moreover, a higher transistor count might lead to a larger surface area on microprocessor chips. Therefore, CPL is not preferred in low-power devices. Furthermore, voltage degradation is a significant issue in CPL logic.

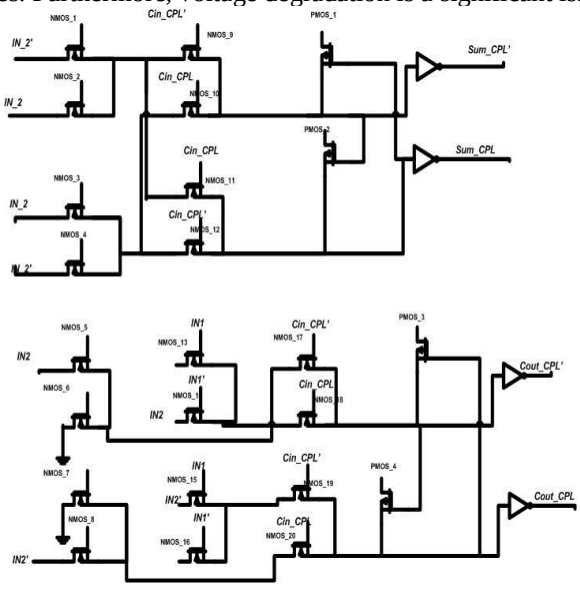

Fig. 1 CPL ADDER [12, 19]

B. HPSC Adder

The high number of transistors and more delay is caused due to usage of the Complementary CMOS technique in producing the sum and the carry. Thus, this HPSC full adder cell has been implemented where the XNOR and XOR module is implemented by using 6-pass transistors.

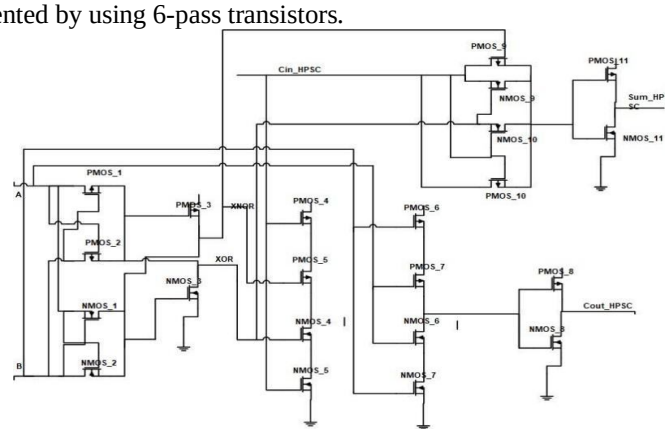

Fig. 2 HPSC ADDER [16]

C. 10T SERF

While optimising the delays and propagation delays, the Static Energy Recovering Full Adder is implemented using XOR and XNOR. This circuit [Fig. 3] leads to a reduction in power consumption due to the unavailability of a ground path. Here, the control gates reuse the charge and it is stored as load in capacitance. Thus, this logic design results to be an efficient and optimized design for storing energy.

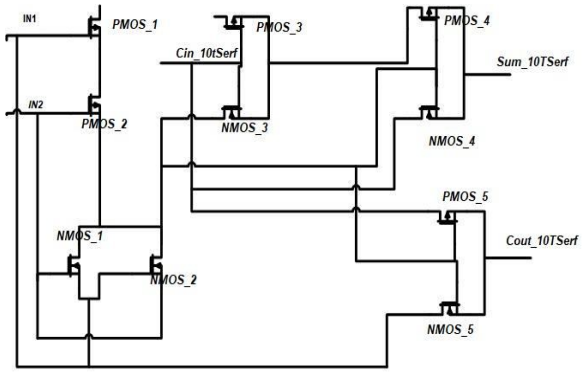

Fig. 3 10T SERF ADDER [29, 19]

D. C-CMOS

This circuit [Fig. 4] consisting of 28 transistors is quite sturdy against voltage scaling while being robust against transistor size. The major drawback of the C-CMOS adder is the addition of buffers for the compensation of high input impedance.

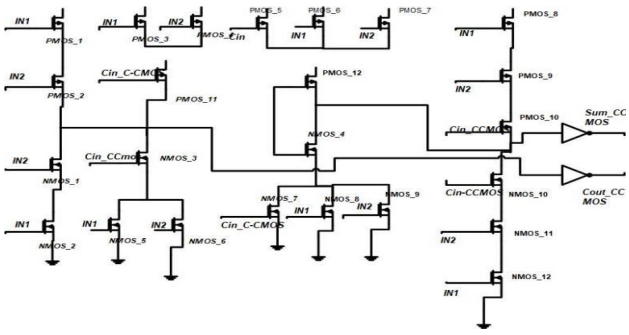

Fig. 4 C CMOS ADDER [13, 19]

E. TFA

This logic design based circuit [Fig. 5] includes 16 transistors to overcome the major drawback of voltage degradation in some logic designs (e.g. CPL). However, its signal strength reduces when connected in cascade. Moreover, the major concern among VLSI designers is its driving capability.

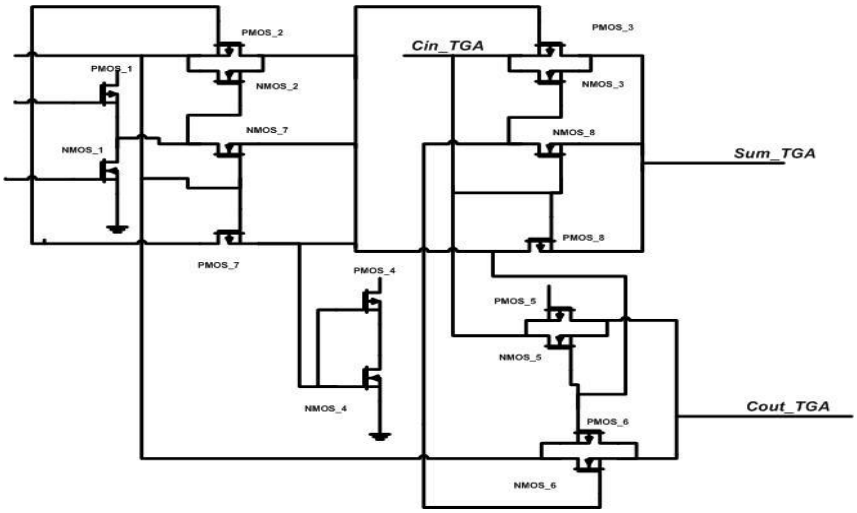

Fig. 5 TFA ADDER [15, 19]

F. TGA Adder

This circuit [Fig. 6] includes 20 transistors for designing a TGA adder to overcome the major drawback of voltage degradation in some logic designs. Though the pros and cons are similar to that of a TFA adder, it varies in orientation and transistor count. Its signal strength reduces when connected in cascade. Moreover, the major concern among VLSI designers is its driving capability.

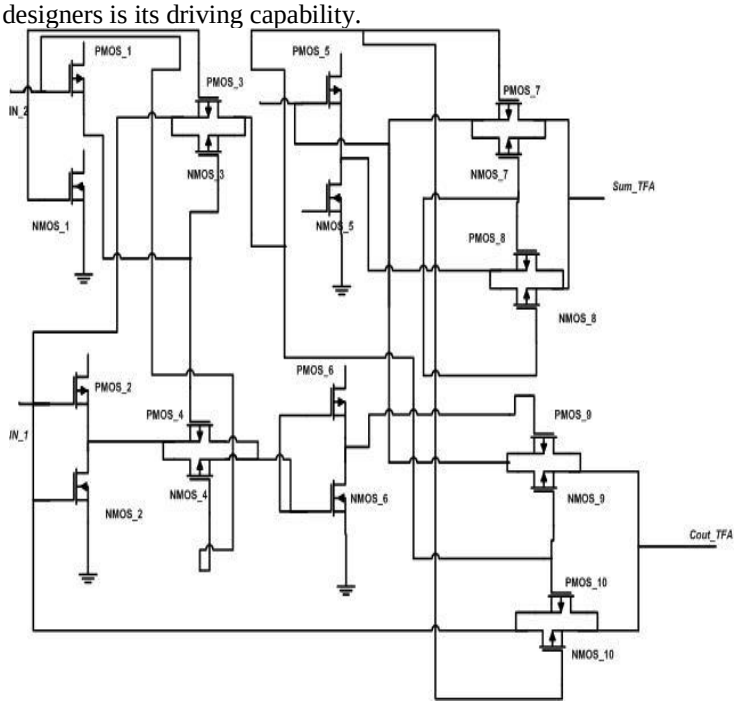

Fig. 6 TGA ADDER [14]

G. 10T GDI

GDI design consists of three terminal inputs with P node, N node and G signifying PMOS, NMOS and Gate terminal respectively. Though the primitive cell seems similar to CMOS logic, the difference resides between the

two. In this circuit [Fig. 7], both PMOS and NMOS transistors, are connected to their diffusions. The gate serves as the common terminal. The effect of logic's body is reduced by connecting the terminal of the body to the diffusion as shown in the figure.

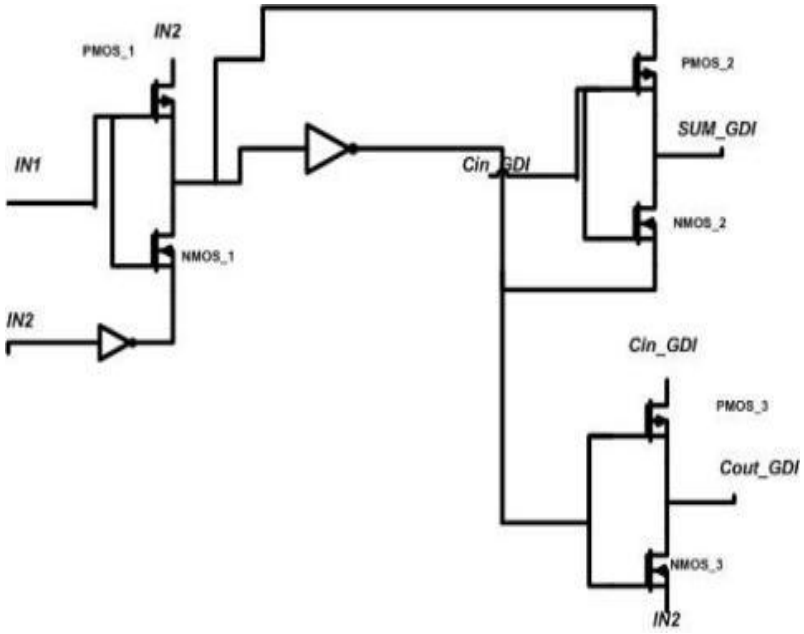

Fig. 7 10T GDI ADDER [18]

H. DPL Adder

This adder circuit [Fig. 8] consists of 28 Transistors for implementation. Outputs of OR as well as And gates are fed into a TG based 2:1 MUX. The addends are the inputs to OR and AND gates whereas the input carry term is the multiplexer's select bit. PTL is used by the OR and AND gates. The major advantage of this design is less propagation delay for DPL due to no internal generation of a signal takes place that controls the multiplexer's select bit. However, the power consumed by DPL is more and its driving capability is poor.

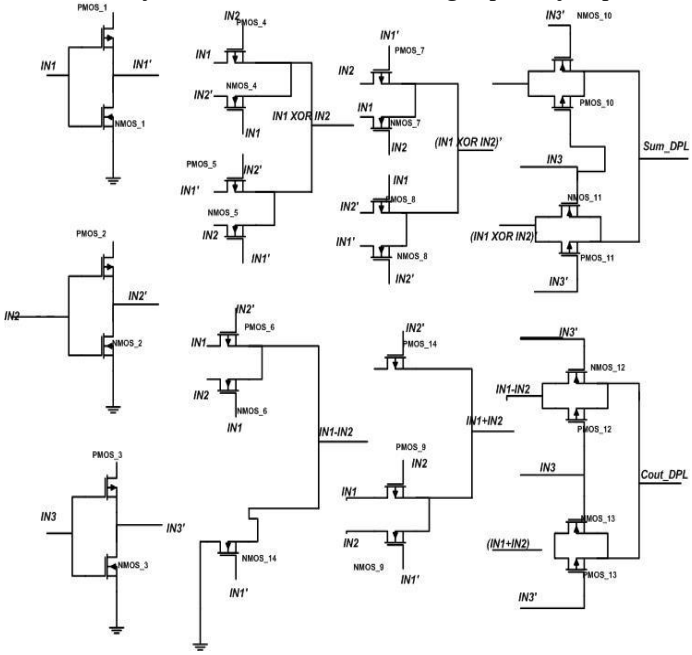

Fig. 8 DPL ADDER [17]

III. Comparative Analysis

Conventionally, some of the earliest versions were CPL or C-CMOS-based full adder cells. However, their PDP, delay and power remain to be satisfactory yet. Here, we can observe that the CPL-based full adder has quite less delay and PDP(0.203 fJ). However, the usage of C-CMOS and CPL full adder in the modern microprocessor is limited as they occupy a larger area in layout design due to high transistor count. Being a major concern in CPL, voltage degradation is overcome by using buffers to restore the voltage levels. The addition of buffers further increases the transistor count and surface area in a chip.

HPSC adder shows the best results considering the power performance. However, high delay leads to higher PDP than TGA, CPL, C-CMOS and other Hybrid adders. Though the TGA adder shows a higher delay than the C-CMOS adder, it surpasses C-CMOS in terms of PDP and power. We can observe that TFA here consumes less power than TGA but PDP and delay are twice more than TGA.

Table I. Comparison Of Performance Parameter [20]

Technology	Ref. No.	No. Of transistors	Power (uW)	Delay(ns)	PDP(fJ)	Comments
CPL	[12]	32	2.183	0.093	0.203	• Low PDP and low propagation delay with good voltage swing. • High switching activity and high transistor count • Buffers required to restore voltage. • Not preferred for processors in small portable devices due to high area consumption
HPSC	[16]	22	1.623	0.232	0.377	• Driving capability is satisfactory with high input impedance. • Alternative for the Complementary CMOS technique & overcomes its high transistor count & delay.
10T SERF	[18]	10	500.5	0.00528	2.6426	• Special structure with low transistor count & low surface area. • Circuit fails to work at supply voltages below 0.3V (Threshold loss problem). • It is an efficient and optimized design for storing energy.
C-CMOS	[13]	28	1.872	0.135	0.253	• Robust against voltage scaling and sizing of the transistor. • Transistor count is high. • Input impedance is high.
TFA	[15]	16	1.689	0.298	0.503	• Transistor count is very low. • Low surface area is required. • Driving capability is poor. • Consumes less power than TGA but PDP & delay are twice more than it
DPL	[17]	28	6.994	0.269	1.881	• Pass transistor logic provides it with a good voltage swing. • High transistor count with a quite high PDP and power loss.
TGA	[14]	20	1.715	0.141	0.242	• Less surface area requirement with low PDP and propagation delay • Cascade connection decreases its signal strength. • Limited to high fan-out situations due to poor driving capability.
10T GDI	[18]	10	456.2	0.00215	0.9808	• Low complexity of the logic design & less surface area with reduced propagation delay • Strong 0 and strong 1 at the output are not feasible.

IV. CONCLUSION

Here the paper gives a comparative analysis of certain existing full-adder cells. Moreover, the merits and demerits of each adder cell have been discussed meticulously. Researchers have developed numerous adders employing various logic styles and techniques, and thus it is imperative to analyze the performance as well as their pros and cons. This broad comparison of all the adder cells will certainly exhibit gradual improvement in delay, propagation delay, and power dissipation. Standard 90 nm technology has been used for all the aforementioned full adder cells. With this comparative study, we seek to assist the VLSI designers to come up with the optimum full adder as per the system requirements.

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