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HDL-based Realization of a 16-QAM Modulator with Sine/Cosine Carrier Generation and Symbol Mapping

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***Abstract*— This article describes the design and simulation of a 16-Quadrature Amplitude Modulation (16-QAM) modulator in Verilog Hardware Description Language (HDL), and its functional verification were performed in the Model Sim simulation environment. 16-QAM is one of the more commonly used digital modulation types and combines amplitude and phase modulation to enable four bits per symbol transmission to ultimately offer better spectral efficiency. The process uses digital symbol mapping, I/Q separation into the components they represent, and carrier modulation using orthogonal sine and cosine waveforms. The modulator designed is intended for FPGA-based systems and is suitable for high-speed digital communications purposes. The simulation results verified the functions of symbol mapping, waveform generation, guaranteed performance, and the output patterns were sufficiently similar. The architecture represents a basic building block for hardware-based communication systems and can be implemented to extend support for other higher-order QAM schemes or to be integrated/combined with channel models and demodulators for end-to-end system building and expansion.**

***Index Terms*— 16QAM, Modulator, I/Q Mapping, Model Sim, and simulation.**

I. INTRODUCTION

With increasing wireless systems and data-intensive applications, the requirement for increased bandwidth efficiency and higher data rates also increases. To meet these, more advanced digital modulation methods have been developed as the foundation of modern communication standards. One of these, 16-Quadrature Amplitude Modulation (16-QAM), is remarkable in the capability of carrying four bits per symbol using the phase and amplitude variations of the carrier wave, sending four times as much information per symbol as more direct schemes like BPSK and QPSK, but over the same bandwidth [1], [3], [9]. Its increased spectral efficiency, however, is at the expense of increased implementation complexity and higher signal-to-noise ratio (SNR) requirements in order to accommodate very low bit-error rates (BER) [3]. This balance is at the center of modern standards of communications such as Wi-Fi (IEEE 802.11), 4G LTE, and cable modem systems, where maximum channel utilization is a fundamental design constraint [9]. Low-power hardware implementation of 16-QAM is especially important in real-time digital communication systems, where deterministic timing, low power usage, and processing speed requirements are typically such that they necessitate an optimized Field-Programmable Gate Array (FPGA) or Application-Specific Integrated Circuit (ASIC) implementation [1], [2], [4]. Hardware acceleration offers fine-grained control over every step of the modulation process, from symbol mapping to carrier and digital signal generation, with lower latency and high-speed data transfer [5], [7].

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The article provides a complete implementation of a 16-QAM modulator in Verilog HDL for FPGA prototyping and verification boards. The design is built on a modular subblock architecture for symbol mapping, I and Q signal generation, digital up conversion using numerically controlled sine and cosine oscillators, and timing control for deterministic signal response [1], [4], [7]. Special attention is also given to fixed-point arithmetic and resource sharing to minimize logic and DSP block utilization on target FPGAs [5], [10]. Functional verification and simulation were conducted through the Model Sim environment to ensure that all the intermediate signal paths possess the expected amplitude and phase relationships as embodied by the 16-QAM constellation diagram [1], [2]. The simulated output of the modulator is compared with theoretical expectations and its performance evaluated under ideal and noisy channel conditions to ensure its robustness against additive white Gaussian noise (AWGN) and distortion, opening the door to further demodulator design research and bit-error rate optimization [6], [8]. This hardware-ready design can serve as a stepping stone to further development, including coherent demodulation, adaptive channel equalization, and higher-order QAM schemes, to facilitate deployment in a full communication transceiver in wireless broadband and beyond-5G systems [5], [8], [10].

II. Literature Survey

Over the years, many researchers engaged in efforts to make the implementation of 16-QAM modulation and demodulation simpler and more efficient using an FPGA. One of the early works showed that by using Quadrature Direct Digital Frequency Synthesizers with a back end Altera Cyclone-II chip could produce the sine and cosine carriers with a great degree of accuracy at low power and low resource utilization over a variety of frequencies [1]. Other groups progressed on to simpler implementations of BASK, BFSK, BPSK, and QPSK modulation on the same FPGA boards while using PWM for the carrier signals so that they consumed less power and space budget but maintained quality of the signal [2]. An interrogation of 16-QAM modulated signals in a real wireless channel, highlighted the ability to change constellation size 'on the fly' depending on signal-to-noise ratio which allowed for better use of bandwidth and lowered errors in noisy environments with the correct constellation size in relation to signal conditions [3]. Author's also specified that the Verilog code generated from a Simulink model of 16-QAM modulation showed hardware that was able to map 16-QAM symbols correctly and achieved good timing, as such, they implied that simulation model can relate quite closely to hardware designs [4]. There has also been work done in enhancing the speed of these designs, and one of the teams was able to develop a pipelined modulator that had no delay at frequencies up to 120 MHz, making it practical for broadband and high-speed data links [5]. There has been much more advanced work that has examined demodulators, where a team was able to develop a modulator that used Direct Digital Synthesis (DDS) to recover the carrier and be able to modulate up to 612 MHz using Xilinx FPGAs, and performed reliably even with different levels of noise [6]. However, the researchers also performed extra research for improved timing and synchronization, including using a Gardner algorithm for clock recovery that was able to reduce jitter and phase noise so that the demodulator was able to more accurately decode 16-QAM signals [7]. Other researchers have attempted fully parallel demodulators using Virtex-7 boards that would allow them to process multiple streams simultaneously with minimal power consumption and still keep a very low bit-error rate (BER) in reasonably realistic wireless conditions [8In a wider comparison of modulation types for 4G , LTE networks; 16-QAM is a mid-ground technique since it has a good combination of higher data rates and resilience to noise which make it effective for most systems [9]. Finally, reviews of design suite software such as Xilinx System Generator indicated that simulating / test a 16-QAM design prior to implementing it on real hardware to save time and improve the design overall [10]. All works above combined show how simple a 16-QAM method can be implemented and tested on real hardware, making it a suitable resource for future wireless communication systems.

III. Block Diagram and Flow Chart

A. Block Diagram

The illustration in figure 1 depicts the basic configuration for a 16-QAM (Quadrature Amplitude Modulation) modulator, a basic modulation format commonly used in modern digital communication systems. To facilitate analysis, the input binary data are grouped into two independent streams referred to as in-phase (I) and quadrature (Q) streams. The position of the two streams is ultimately related to the two components of the symbol (the I and Q respectively) which will yield information depending on change in amplitude and phase, to modulate the two desired signal dimensions. The configuration employs an oscillator to create a carrier signal for modulation. The same carrier will modulate the in-phase component directly, while the same carrier phase

shifted by 90 degrees will modulate the quadrature stream. Because the modulation will occur due to the multiplication of each data stream with the carrier, by-combining the I component with its carrier using cos(wt) and the Q component with the carrier using sin(wt), we can use the multipliers or mixers together. After the modulation is complete for both paths, we will add the outputs of each channel together to produce the desired 16-QAM signal. So, the resultant signal will convey the intended message information through the phase and amplitude of the resulting combined signal. This is a very efficient way to transmit the message by using one carrier frequency to communicate to the receiver the information contained in multiple amplitude and phase states to indicate the intent of the original message.

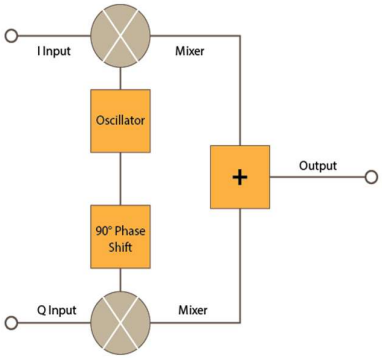

Figure 1. Block Diagram of Modulator

The employment of orthogonal carriers means that the I and Q components will not interfere with one another, thereby providing effective demodulation at the receiving end. This block diagram shows clearly and briefly how 16-QAM modulation is applied in practice. The block diagram depicts how the four bits of data is being taken and then divided into I and q values, which are then sent to a mixer to add the sine and cosine value finally obtaining the modulated output for transmission

B. Flow Chart

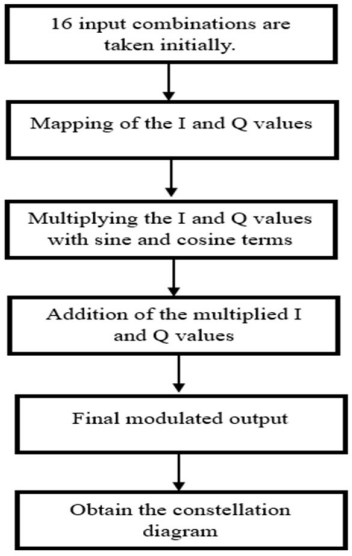

Figure 2. Flow Chart for 16QAM Modulator Design

The sequence of steps in figure 2 clearly illustrates the procedure for producing a 16-QAM modulated signal. Each of the 16 different combinations of the 4-bit input represent a unique symbol. These binary inputs are allocated amplitude values for the in-phase (I) and quadrature (Q) components, and are laid out in a 4×4 constellation pattern, which shows a distinct pair of I-Q coordinates to represent the symbols. When the 4-bit inputs have been allocated amplitude values to the I and Q channels, the modulation can begin, whereby the I

component is multiplied to a cosine carrier wave and the Q component is multiplied to a sine carrier wave. This operation prepares the digitally-modulated in-phase and quadrature signals in the analog domain and together they provide system capacity to carry digital dataThe addition of the two modulated signals produces the final modulated 16-QAM output signal that now has both amplitude and phase applied. The flowchart ends with the constellation diagram's display, where the 16 symbol points are displayed in the I-Q plane. This constellation diagram visually represents the modulation scheme and is useful to analyze the signal quality and its resilience to noise in the communication system.

IV. Proposed Methodology

The methodology proposed is a step-by-step design and simulation of a 16-QAM modulator in Verilog HDL. The table 1 depicts 4-bit parallel digital input data, which is converted to the corresponding amplitudes of the in-phase (I) and quadrature (Q) components. These conversions are according to the conventional 16-QAM constellation, where each symbol corresponds to a distinct pair of I and Q values. Once I and Q components are created, each of them is multiplied by sinusoidal carriers—cosine for the I component and sine for the Q component. The carriers are usually created using a look-up table or direct Verilog sine/cosine generation techniques. The outputs are then combined to form the final modulated signal that contains the information. From table 2, it is observed that each input values has a unique amplitude and phase which results in transfer of more number of bits or information. The modulated output is then monitored using a waveform viewer in ModelSim to verify that the modulation is functioning as desired. Once I and q values are mapped they are multiplied by sine and cosine values.

TABLE I. MAPPING OF I AND Q VALUES

Bits	I (In-phase)	Q (Quadrature)
0000	3	3
0001	1	3
0010	-1	3
0011	-3	3
0100	3	1
0101	1	1
0110	-1	1
0111	3	1
1000	3	-1
1001	1	-1
1010	-1	-1
1011	-3	-1
1100	3	-3
1101	1	-3
1110	-1	-3
1111	-3	-3

TABLE II. CORRESPONDING PHASE AND ANGLES FOR INPUT BITS

Bits	I	Q	Amplitude	Phase (°)
0000	-3	-3	4.24	-135°
0001	-3	-1	3.16	-161.57°
0010	-3	1	3.16	161.57°
0011	-3	3	4.24	135°
0100	-1	-3	3.16	-108.43°
0101	-1	-1	1.41	-135°
0110	-1	1	1.41	135°
0111	-1	3	3.16	108.43°
1000	1	-3	3.16	-71.57°
1001	1	-1	1.41	-45°
1010	1	1	1.41	45°
1011	1	3	3.16	71.57°
1100	3	-3	4.24	-45°
1101	3	-1	3.16	-18.43°
1110	3	1	3.16	18.43°
1111	3	3	4.24	45°

The modulated signal can be mathematically expressed as follows "(1),"

$$S(t) = I \times Cos(2 \times \pi \times fc \times t) + Q \times Sin(2 \times \pi \times fc \times t) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.(1)$$

Where, *fc is the carrier frequency*
I and Q are mapped values
$Cos(2 \times \pi \times fc \times t)$ *and* $Sin(2 \times \pi \times fc \times t)$ *are carrier waveforms*
where the amplitude and phase values are obtained by using "(2)," "(3)," accordingly,

$$Amplitude = \sqrt{I^2 + Q^2} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.(2)$$

Phase = tan^-1(Q/I) ……………………………………………(3)

Different test cases are also applied via a testbench to confirm that every input properly converts into the desired modulated signal. The simulation results assist in confirming the timing, accuracy, and signal integrity of the design. Figure 3 shows how the I and Q values are mapped to obtain the constellation diagram. For a 16QAM, we obtain 16 constellation points, 4 in each quadrant accordingly.

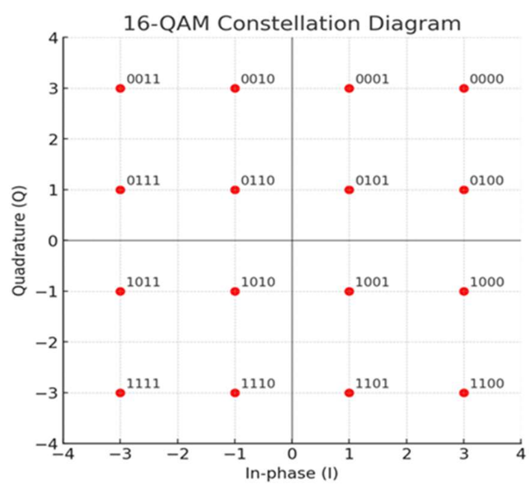

Figure 3. 16QAM Constellation Diagram

V. RESULTS

The QAM modulator was tested by checking all 16 available 4-bit input combinations. All of the input patterns were correctly reflected in the correct I and Q values according to the standard 16-QAM constellation. The outputs we observed in the simulation matched the expected amplitude levels and phase relationships properly. The I and Q signals maintained consistent and stable outputs for multiple clock cycles, indicating the latching and modulation logic are operating properly. Thus, satisfying that the modulator operates correctly in ideal conditions without noise. The figure 4 shows how the combinations of I and Q values are obtained for different input values, also these I and Q values are multiplied with cos and sine waves to obtain the final modulated output. The modulated output have different amplitude and phase levels for each symbol that is generated, there are a total of sixteen symbols generated for which there are three amplitude levels and twelve phases resulting in standard constellation diagram for a 16qam system. The figure 5 shows the output of 16qam modulator, here the 16 input combinations are taken, each input is mapped to corresponding I and Q values based on the lookup table (table1). once the I and Q values are generated they are multiplied with cosine and sine waveforms, these sine and cos waveforms are LUT based. Finally the output is obtained "(4)," after multiplication, these signals are then transmitted.

QAM out = (I × cos wave + Q × sin wave) ……………………..(4)

The figure 6 shows how different levels of amplitudes and phase are obtained for each input, therefore the data transmission rate increases thereby providing higher rates of transmission over a time period.The figure 7 and 8 shows how different angles and phases are mapped on a constellation diagram. The 16-QAM constellation

diagram is a visual plot of the modulation system in which 16 different symbols are encoded into a two-dimensional plane by the in-phase (I) and quadrature (Q) components. Each symbol corresponds to a different 4-bit binary sequence, using 2 bits for the I axis and 2 bits for the Q axis. The diagram is a 4x4 grid in which every point represents a combination of some amplitude and phase, enabling the transmission of 4 bits per symbol. Points are spaced in such a way that they minimize symbol errors due to noise without compromising spectral efficiency. Symmetry of the constellation facilitates the easier implementation of the constellation in digital communication systems, and the well-defined separation between the symbols ensures that distinction among them is possible even in the presence of moderate noise, and therefore 16-QAM is a common modulation method in contemporary wireless and digital communication systems.

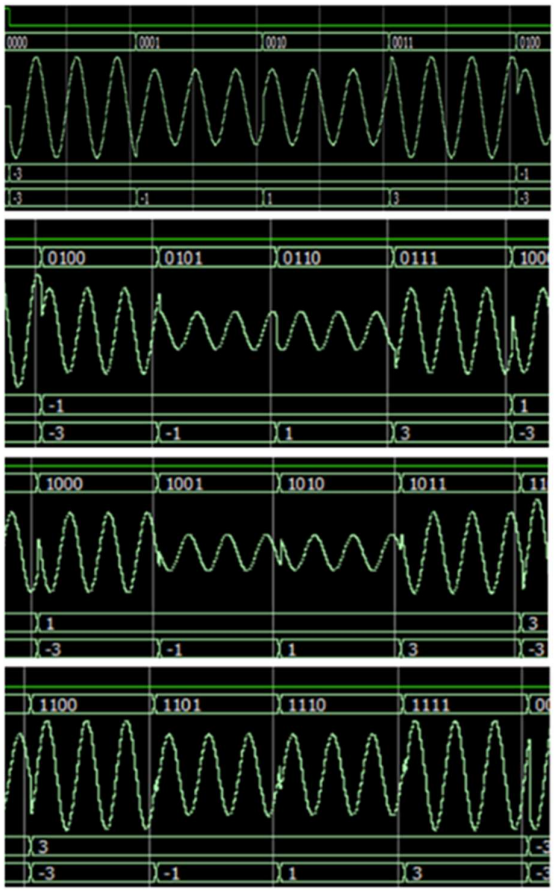

Figure 4. I and Q Values Based on Table 1

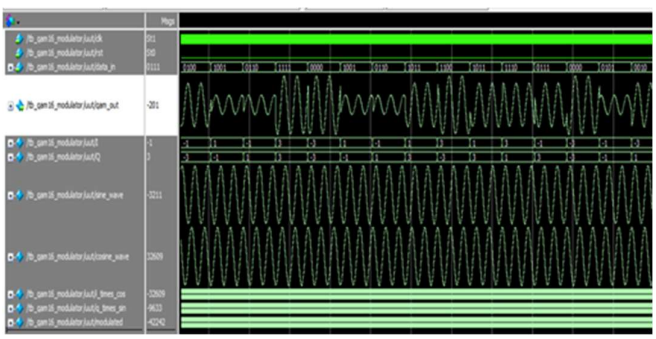

Figure 5. Output of 16QAM Modulator

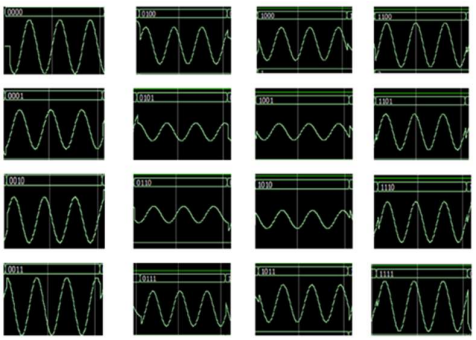

Figure 6. All 16 combinations represented in different phase and angles

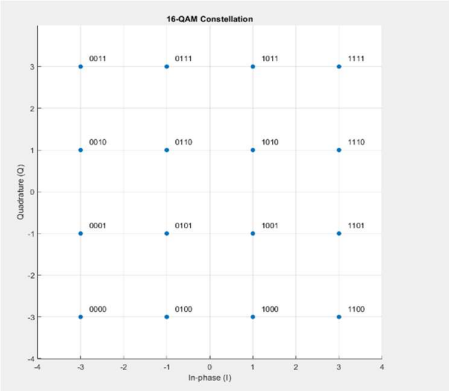

Figure 7. Constellation Diagram of Design Obtained from Matlab

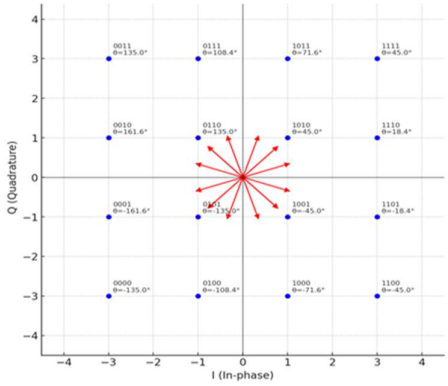

Figure 8. Analysis of Constellation Diagram

VI. CONCLUSION

This design represents substantial progress in understanding advanced digital modulation techniques with the design and development of a 16-QAM (Quadrature Amplitude Modulation) modulator. A complete 16-QAM modulator was developed in Verilog HDL, which included the mapping of all 4-bit input combinations to their corresponding in-phase (I) and quadrature (Q) values from a standard 16-QAM constellation table. By multiplying the I and Q values by sine and cosine carrier signals to form the modulated waveform. The design was simulated, and the constellation output diagram was plotted on MATLAB to test whether the structure of the modulator was functioning correctly and measuring the performance of the overall system. The plotted output included sixteen identified and accurately spaced constellation points for every unique 4-bit input, indicating successful modulation design converting binary data into complex symbols with the required amplitude and phase characteristics of 16-QAM modulation. The use of multiplication by sine and cosine carriers also ensured that the modulated signal was ready for analog transmission and that demodulation could be done via coherent detection ways. The constellation analysis conducted on MATLAB also confirmed, that the output waveform depicted the shape of a 16-QAM signal indicating there was practical use of our design. In summary, we think this project has created a theoretical expectation, but it also provided an implementation accuracy using simulation and graphical presentation using the model Sim platform, which and sufficiently created a strong platform for future work on FPGA streaming systems, allowing for real-time transmission of signals, possibly including demodulation, noise reduction, and in the end the complete build of the system.

REFERENCES

[1] Dr. Kamal Aboutabikh, Dr. Abdul-Aziz Shokyfeh, Dr. Amer Garib, "Design and Implementation of a Digital 16-QAM Modulator Using FPGA," International Multidisciplinary Research Journal Reviews (IMRJR), Volume 1, Issue 2, October 2024.

[2] Dr. Pallavi G. Darji, Ms. Madhvi B. Sukhanandi, "Digital Modulation/Demodulation Techniques on FPGA," International Journal of Novel Research and Development (IJNRD), Volume 7, Issue 4, April 2022.

[3] D. Kaur and S. Mehta, "Analysis and Optimization of 16-QAM Modulation for Wireless Systems," Wireless Communications Journal, Volume 12, Issue 3, March 2020.

[4] Juned K. Qureshi, Dr. Ahmed Sajjad Khan, "Study and Design of 16-QAM Modulator in FPGA," Journal of Emerging Technologies and Innovative Research (JETIR), vol. 6, issue 2, February 2019.

[5] C. Zhang, M. Nguyen, and L. Bose, "FPGA-Based High-Speed Digital QAM Modulator," IEEE Transactions on Circuits and Systems-I, vol. 65, no. 9, pp. 1–10, Sep. 2018.

[6] Remya Rajan, Lijesh L, "Reconfigurable Implementation of QAM Demodulator in an FPGA," International Journal of Technical Research and Applications (IJTRA), Volume 5, Issue 3, May-June 2017

[7] J. Chen and C. Du, "Research and Implementation of 16-QAM Based on FPGA," IEEE, pp. 1–5, 2016.

[8] M. Ayat, S. Mirzakuchaki, and A. A. Beheshti-Shirazi, "Design and Implementation of High Throughput, Robust, Parallel M-QAM Demodulator in Digital Communication Receivers," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 63, no. 8, pp. 1–12, Aug. 2016.

[9] Charles U. Ndujiuba, Oluyinka Oni, Augustus E. Ibhaze, "Comparative Analysis of Digital Modulation Techniques in LTE 4G Systems," Journal of Wireless Networking and Communications, Volume 5, Issue 2, August 2015.

[10] R. Swain and A. K. Panda, "Design of 16-QAM Transmitter and Receiver: Review of Methods of Implementation in FPGA," International Journal of Engineering and Science, vol. 1, no. 9, pp. 1–8, Nov. 2012.