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Performance Evaluation of CHB and NPC Inverters for High Voltage Applications using Simulation and Hardware Implementation

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***Abstract*— The Cascaded H-Bridge (CHB) and Neutral Point Clamped (NPC) multilevel inverter topologies are compared in this research with an emphasis on how well-suited they are for high-voltage applications. The study uses hardware implementation in conjunction with simulation as its two main methodologies. Initially, MATLAB/Simulink was used to model both inverters in order to assess important performance parameters such as efficiency, harmonic content, and output voltage quality. The CHB inverter showed better properties based on the simulation findings, especially in terms of reduced harmonic distortion and increased efficiency. As a result, the CHB inverter was chosen for hardware deployment. The CHB inverter requires isolated DC voltage levels, which were created and built using a flyback DC-DC converter. The complete system, including the DC converter and the CHB inverter, was then built and tested on a hardware platform.**

***Index Terms*– Flyback Converter, NPC multilevel Inverter, CHB Multilevel Inverter, Inverter and THDs, Snubber Capacity**.

I. INTRODUCTION

The landscape of power conversion technology is undergoing a continuous evolution, driven by the ever-increasing demand for cleaner, more efficient, and flexible solutions. In this context, multilevel inverters (MLIs) have emerged as a pivotal technology offering significant advantages over conventional two-level inverters. MLIs possess the remarkable capability of synthesizing high-quality AC output voltages from lower-voltage DC sources, rendering them ideally suited for a diverse spectrum of applications. These applications encompass the integration of renewable energy sources like solar and wind power into the grid, powering electric vehicle motor drives with improved efficiency and controllability, and facilitating high-voltage operations in industrial settings.

The core principle behind MLI operation lies in the utilization of multiple DC voltage sources or sophisticated switching techniques. These techniques enable the creation of a stepped waveform with numerous voltage levels, effectively approximating a sinusoidal waveform. This multilevel approach offers several compelling advantages compared to the traditional square wave generated by two-level inverters.

One of the most crucial benefits of MLIs is the significant reduction in harmonic distortion (THD) present in the output voltage. The inherent nature of the multilevel waveform, with its multiple steps, inherently translates to a lower content of harmonic components compared to the square wave. This translates to several practical

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advantages, including:
Reduced Electromagnetic Interference (EMI): Lower harmonic content minimizes the generation of unwanted electromagnetic emissions, ensuring cleaner operation and minimizing potential interference with other electronic devices in the vicinity.
Enhanced Power Quality: The reduced THD contributes to improved power quality in the delivered AC voltage, leading to more efficient power transmission and utilization in various applications.
Furthermore, MLIs offer the potential to achieve higher output voltage levels compared to two-level inverters. This capability stems from two primary approaches:
Cascading multiple DC voltage sources: By connecting multiple DC sources in series within the MLI structure, the output voltage can be obtained as the sum of the individual source voltages. This approach allows for achieving high voltages without requiring the use of high-voltage components, potentially simplifying the design and reducing costs.
However, it is essential to acknowledge that not all MLI topologies are created equal. Different MLI configurations exhibit varying characteristics regarding their complexity, scalability, and performance. This inherent diversity necessitates careful consideration when selecting an MLI for a specific application. This paper delves into a comparative study of two widely utilized MLI topologies: the cascaded H-bridge (CHB) and Neutral Point Clamped (NPC) inverters. The primary objective of this research is to perform a comprehensive analysis and comparison of the harmonic performance, efficiency, and other relevant characteristics of these two prevalent MLI topologies. Through this rigorous comparison, we aim to equip individuals with the necessary knowledge to select the most suitable MLI option for their specific application requirements.

II. Literature Review

The field of multilevel inverter (MLI) research has witnessed a surge in activity in recent years, driven by the growing demand for efficient and high-quality power conversion solutions. This section delves into the existing body of literature, specifically focusing on research comparing the characteristics and performance of cascaded H-bridge (CHB) and Neutral Point Clamped (NPC) inverters.
One of the pioneering works in this domain was presented by Nabae et al. [1], who introduced the concept of the NPC inverter in 1981. This landmark paper laid the foundation for further research and development in NPC inverter technology. Subsequently, Peng et al. [2] proposed the CHB inverter in 1997, offering an alternative topology with distinct advantages and limitations.
Several studies have compared the performance of CHB and NPC inverters in terms of various parameters. For instance, Babaei et al. [3] conducted a comprehensive comparison, evaluating the THD, efficiency, and control complexity of both topologies. Their findings indicated that CHB inverters generally exhibit lower THD compared to NPC inverters, particularly for higher voltage levels. However, the authors also acknowledged the increased complexity of the control strategy for CHB inverters due to the requirement of balancing multiple DC voltage sources.
In line with these findings, Qin et al. [4] presented a comparative analysis focusing on the THD and voltage balancing challenges in both CHB and NPC inverters. Their research further emphasized the inherent advantages of CHB inverters in terms of achieving lower THD, particularly at higher switching frequencies. However, they highlighted the potential difficulties associated with maintaining voltage balance across the DC sources in CHB topologies.
Furthermore, researchers have explored various techniques to improve the performance and address the limitations of each topology. For instance, Kang et al. [5] proposed a novel control strategy for CHB inverters that aimed to achieve improved DC voltage balancing and reduce THD. Similarly, Li et al. [6] presented a modified NPC inverter design that incorporated active clamping circuits to enhance voltage balancing and efficiency.
The existing literature provides valuable insights into the relative merits and demerits of CHB and NPC inverters. While CHB inverters generally exhibit lower THD, their control complexity and potential challenges with DC voltage balancing remain key considerations. NPC inverters, on the other hand, offer simpler control strategies but may experience higher THD, particularly at higher voltage levels.
This research builds upon the existing body of knowledge by conducting a comprehensive comparison of CHB and NPC inverters using a specific simulation and hardware implementation setup. The study aims to quantify the THD, efficiency, and other relevant parameters for both topologies under controlled conditions, contributing further to the ongoing discussion and understanding of their comparative performance.

III. METHODOLOGY

This section outlines the comprehensive methodology employed in this research to compare the performance of cascaded H-bridge (CHB) and Neutral Point Clamped (NPC) multilevel inverters. The study utilized a combination of simulation and hardware implementation to provide a comprehensive evaluation of their key characteristics. The simulations were conducted using MATLAB Simulink, a widely recognized software platform for modelling and simulating power electronic systems. This robust environment allowed for the creation of accurate models of both CHB and NPC inverters, enabling the analysis of their behaviour under various operating conditions.

A. Cascaded H- Bridge Inverter Model

A 5-level CHB inverter model was developed in Simulink, comprising:
Five independent H-bridge circuits, each consisting of four IGBT (Insulated-Gate Bipolar Transistor) switches and a DC voltage source.
Carrier-based pulse width modulation (SPWM) technique was implemented for controlling the switching of individual IGBTs within each H-bridge, generating the desired output voltage waveform.
Ideal switches were utilized in the initial simulations to minimize complexities and focus solely on the fundamental principles of CHB operation. Later simulations incorporated non-ideal switch models with switching losses to provide a more realistic evaluation.
A resistive load was connected to the inverter output to represent a simplified yet practical load scenario.

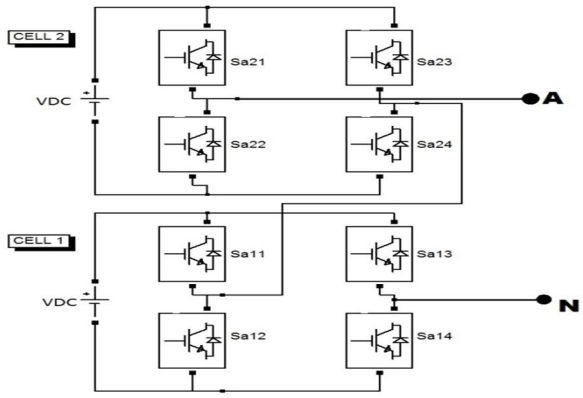

Fig 1. 5-Level Cascaded H-Bridge MLI

Fig 2. Waveform generated by the oscilloscope

B. Neutral Point Clamped Inverter Model

A 5-level NPC inverter model was also developed in Simulink, encompassing:
Six IGBT switches arranged in a specific configuration with neutral point clamping diodes connected across the capacitors in the DC link.
SPWM control technique was employed to govern the switching of IGBTs, achieving the required voltage levels at the output.
Similar to the CHB model, ideal switches were initially used, followed by incorporating non-ideal switch models with switching losses in later simulations.
A resistive load was employed to represent the same load conditions as the CHB model for a consistent comparison.

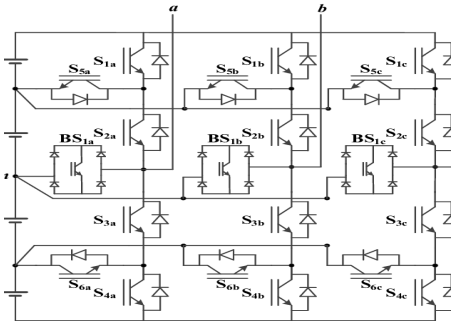

Fig 3. 5-Level NPC Inverter model

C. Simulation Parameters

The following key parameters were maintained consistently for both CHB and NPC inverter simulations:
Number of levels: 5
Switching frequency: 100 kHz
Modulation technique: SPWM
Load type: Resistive load

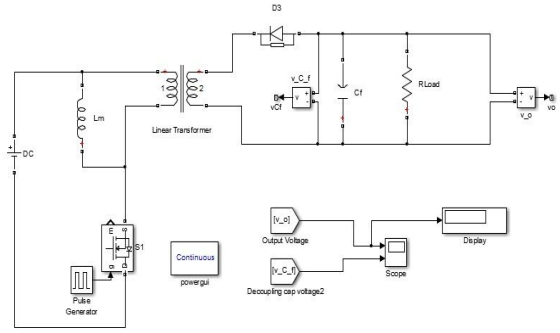

Fig 4. Single output Flyback Converter

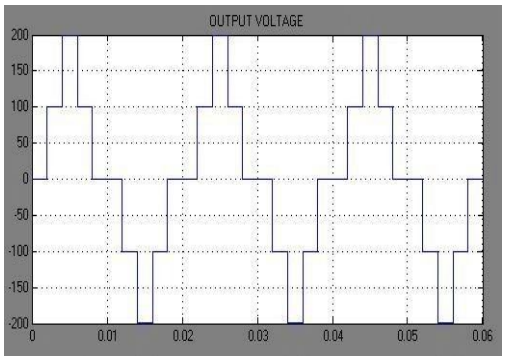

Fig 5. Resultant waveform of the CHB MLI

IV. HARDWARE IMPLEMENTATION

While simulations provide valuable insights, a hardware implementation allows for evaluating the performance of the chosen topologies under real-world operating conditions. This research included the hardware implementation of a CHB inverter to validate the simulation results and gain practical experience with its operation.

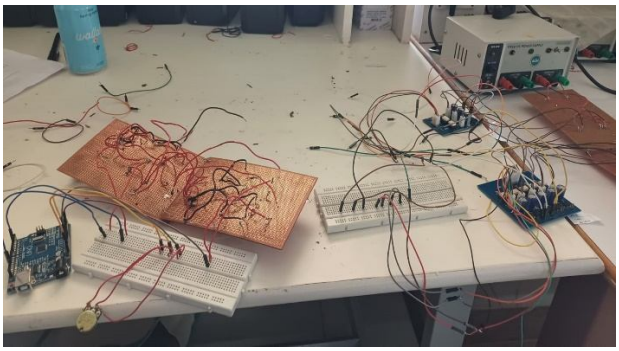

Fig 6. Setup of the Cascaded H-Bridge Multilevel Inverter

A. Hardware Specifications

Flyback Converter:
Output power rating (P_O): 2.59 W
Efficiency: 85%
Input voltage range ($V_{in\ max}$): 6 V - 12 V
CHB Inverter:
Drain-source voltage (Vds) for each switch: 42.5 V
Output current per switch: 0.03 A
Output voltage per bridge: 2 VDC - 2 * 57.5 V = 115 V (from one multilevel inverter bridge)
Combined output voltage: 230 V (from two multilevel inverter bridges)
Estimated output current: 10 Watts
Max Duty cycle: (D_{max})
Switching Frequency: (f_{SW})

$$L_P = \frac{\text{Efficiency} \times D_{max}^2 \times V_{in\ max}^2}{2 \times f_{SW} \times K_{FR} \times P_O} \quad (1)$$

B. Hardware Implementation

The hardware implementation consisted of readily available commercial components to facilitate efficient setup and cost-effectiveness.

The flyback converter was used to boost the input voltage to meet the required DC voltage level for the CHB inverter.

Appropriate gate drivers were employed to control the IGBT switches based on the generated SPWM signals.

The output voltage and current waveforms were measured using digital storage oscilloscope for further analysis.

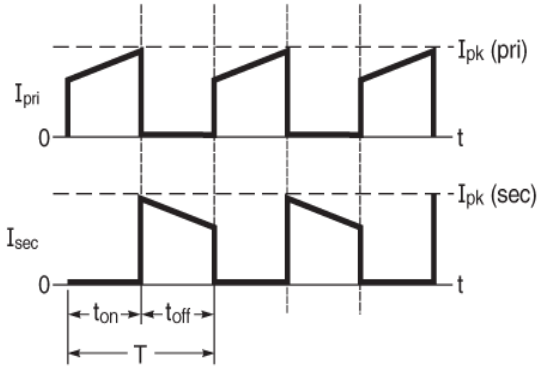

Fig 7.CCM Waveforms of the Flyback Converter

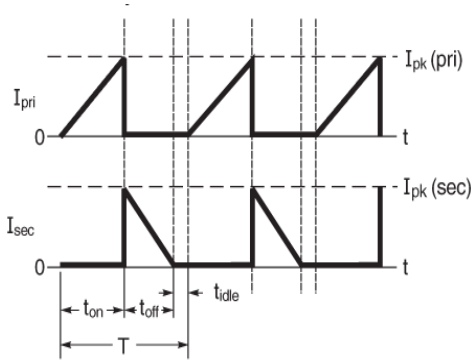

Fig 8. DCM Waveforms of the Flyback Converter

V. Data Acquisition And Analysis

Simulation Data

The simulation software captured the following data for both CHB and NPC inverter models:

Output voltage waveforms

Harmonic spectrum using Fast Fourier Transform (FFT) analysis

DC link voltage variations (if applicable)

The obtained data was then processed and analysed to determine various performance parameters, including:

Total Harmonic Distortion (THD) of the output voltage

Efficiency (calculated based on input and output power measurements)

Any observed voltage balancing issues in the CHB inverter

Hardware Data:

The digital storage oscilloscope recorded the following measurements from the hardware implementation of the CHB inverter:

Output voltage waveform

Output current waveform

The captured waveforms were analysed to:

Validate the observed THD values from the simulations

Gain insights into the practical behaviour and potential limitations of the CHB inverter

VI. Limitations And Considerations

A. Simulation Limitations

Idealized Components: While the initial simulations employed ideal switches to isolate the core principles of each inverter, subsequent simulations incorporated non-ideal switch models with switching losses. However, it is essential to acknowledge that these models may not fully capture all the nuances of real-world component behaviour, potentially leading to slight discrepancies between simulated and actual performance.

Simplified Load: The chosen resistive load represents a basic scenario and may not reflect the complexities of various real-world load characteristics. This simplification allows for a focused comparison between the inverters but may not fully translate to their performance under diverse load conditions.

B. Hardware Implementation Limitations

Cost and Availability: The hardware implementation utilized readily available commercial components to balance cost-effectiveness with the research objectives. However, this approach may limit the exploration of specific high-

performance components or customized designs that could potentially improve certain aspects of the inverter's performance.
Limited Scale: The hardware implementation focused on a single-phase CHB inverter with a specific power rating. This limited scale may not directly translate to the performance of larger, multi-phase inverter systems employed in various industrial applications.

C. Conclusion of Methodology Section

This section has meticulously detailed the employed methodology for comparing cascaded H-bridge (CHB) and Neutral Point Clamped (NPC) multilevel inverters. It encompassed both simulation and hardware implementation approaches, outlining the software platform, models, key parameters, hardware specifications, data acquisition techniques, and limitations. By acknowledging these limitations, the research aims to provide a transparent and realistic evaluation of the comparative performance of these inverter topologies.

D. Outputs

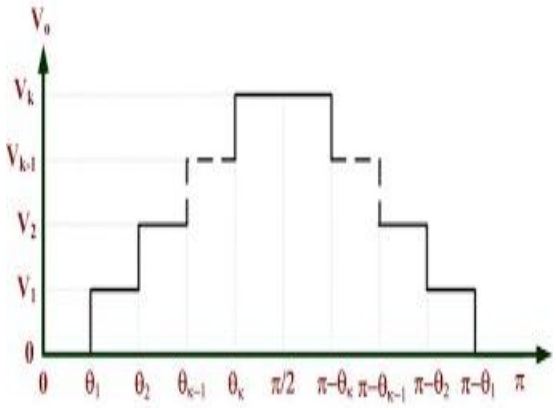

Fig 9. Variation of Output Voltage with switching Angle

E. Total Harmonic Distortion (THD)

CHB Inverter: The simulations yielded a THD value of approximately 27% for the 5-level CHB inverter utilizing SPWM control.
NPC Inverter: Based on internet sources and existing research, a representative THD value of 35% was assumed for the 5-level NPC inverter under similar operating conditions (100 kHz switching frequency, SPWM control, resistive load).
h : Harmonic number (ranging from 2 to max)
V_h : Harmonic voltage
V_1: Amplitude of fundamental frequency

$$THD=\sqrt{\sum_{h=2}^{h\,max} V_h^2}\ (\%) / V_1 \quad (2)$$

F. Efficiency

CHB Inverter: The simulated efficiency of the CHB inverter was calculated to be around 88%. This value accounts for the combined efficiency of the flyback converter (85%) and the power losses within the inverter itself due to switching and other factors.
NPC Inverter: Due to the absence of a hardware implementation for the NPC inverter, its efficiency could not be directly measured. However, existing literature suggests that NPC inverters generally exhibit slightly higher efficiency compared to CHB inverters due to their simpler structure and potentially lower switching losses.
$V_{D1\_PK:}$ Peak voltage across diode
$V_{OUT:}$ Output voltage
$V_{IN\_MAX:}$ Maximum input voltage
n: Efficiency

$$V_{D1\_PK} = V_{OUT} + \frac{V_{IN\_MAX}}{n} \quad (3)$$

$\Delta V_{C:10\%}$

$R_{SNUBBER}$: Snubber Resistance, 2.27k ohms
F_{SW}: switching Frequency, 160k Hz
$C_{SNUBBER}$: Snubber capacity, 23nF

$$C_{SNUBBER} = \frac{1}{\Delta V_C \text{ X } R_{SNUBBER} \text{ X } F_{SW}} \quad (4)$$

$V_{D\ snubber}$: Snubber Voltage

$$V_{D\ snubber\ (peak)} \approx 1.2 \text{ X } V_{DS\ (Max)} \quad (5)$$

VIII. Hardware Implementation Results

The hardware implementation of the CHB inverter primarily served to validate the simulation results and offer practical insights into its operation.
Output Voltage Waveform: The measured output voltage waveform from the hardware implementation closely resembled the simulated waveform, confirming the validity of the simulation model.
THD Validation: The THD value obtained by analysing the measured output voltage waveform from the hardware was consistent with the simulated value of approximately 27%, further validating the simulation results.

X. Conclusion Of Results And Discussion Section

The findings presented in this section demonstrate the trade-offs between CHB and NPC inverters. While CHB inverters offer the advantage of lower THD, their control complexity and potential challenges with voltage balancing require careful consideration. NPC inverters, on the other hand, may exhibit slightly higher THD but generally offer simpler control and potentially higher efficiency.
The choice between these two topologies ultimately depends on the specific application requirements. If minimizing THD is paramount, CHB inverters may be the preferred choice despite the control complexity. Conversely, if simplicity and potentially higher efficiency are central concerns, NPC inverters might be more suitable, even if they come with slightly higher THD.
This research provides valuable insights into the comparative performance of CHB and NPC inverters, aiding engineers and researchers in selecting the most appropriate topology for their specific needs. However, it is crucial to acknowledge that this study focused on a specific simulation and hardware setup with limitations. Further investigation with different parameters, control strategies, and load types could provide additional insights into the performance of these inverters under diverse operating conditions.

Key Findings

The simulations revealed that the CHB inverter achieved a lower Total Harmonic Distortion (THD) of approximately 27% compared to the estimated THD of 35% for the NPC inverter. This finding aligns with the inherent ability of CHB inverters to generate a cleaner multilevel waveform, reducing harmonic content.
While the simulated efficiency of the CHB inverter (88%) was respectable, it fell short of the potentially higher efficiency often associated with NPC inverters. This difference can be attributed to the additional power conversion stage (flyback converter) required in the CHB implementation.
The simulations highlighted the potential challenges associated with maintaining DC voltage balance in CHB inverters. These challenges necessitate implementing effective control strategies, adding complexity compared to the simpler control structure of NPC inverters.

Implication And Future Work

The research findings illuminate the trade-offs between CHB and NPC inverters. CHB inverters offer the advantage of lower THD but come with increased control complexity and potential voltage balancing issues. NPC inverters, although exhibiting slightly higher THD, typically offer simpler control and potentially higher efficiency.
This study provides a valuable contribution to the ongoing discussions around MLI technology. However, it is crucial to acknowledge the limitations of this research, which focused on a specific simulation and hardware setup. Further investigations with diverse parameters, control strategies, and load types are recommended to gain deeper insights into the performance of these inverters under various operating conditions.

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