

Power Efficient Memory based Transistor-Memristor with CMOS Configuration Hybrid Mode Circuits for Future Neuromorphic Computation

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Abstract— This work explores the design of essential arithmetic blocks for digital logic circuits such as encoder, decoder, full adder, multiplexer, and multiplier using a hybrid CMOS–Memristor approach. The aim is to create more compact and energy-efficient alternatives to traditional CMOS designs by taking advantage of the memristor’s programmable resistance. Each circuit has been built and simulated using LT-Spice to study its functionality, power efficiency, and performance. The results show that incorporating hybrid approach of CMOS with memristors significantly reduces the number of components and power usage while maintaining reliable operation. This work highlights the potential of memristor-based logic as a promising direction for future low-power and scalable digital systems. About 98% of power optimization and Hybrid mode arithmetic circuits show optimization up to 98% compared to CMOS technology.

Index Terms— Memristor, LT-spice, CMOS-Memristor hybrid, low power, Digital logic circuit.

I. INTRODUCTION

The idea of the memristor was first introduced by Professor Leon Chua in 1971 as the fourth fundamental circuit element, joining the resistor, capacitor, and inductor [3]. For many years, it remained just a theory until 2008, when Hewlett-Packard Labs successfully built the first physical memristor [16]. Memristor device has special ability to “remember” the amount of current that has passed through it by adjusting its resistance. This unique property gives it non-volatile memory behaviour, meaning it retains its state even after power is turned off. As modern CMOS technology begins to face major hurdles—like increased power leakage, scaling limits, and heat issues memristors offer a promising solution [13][17]. They work at the nanoscale, use very little power, and can be easily combined with existing chip technologies. This allows the creation of hybrid designs, where memristors and CMOS transistors work together. One such method is called Memristor Ratioed Logic (MRL) [7], which uses the switching ability of memristors to perform logic operations with fewer transistors, saving space, power, and improving speed. In this project, we applied this hybrid approach to design important digital circuits more efficiently. Starting with basic gates like NOT, AND, OR, XOR, NOR, we built each using just one memristor and one NMOS transistor.

These simple building blocks were then used to create larger circuits like a 3-bit encoder, 3-bit decoder, 4:1 multiplexer, 1-bit full adder, 4-bit full adder and even a 4-bit multiplier. All these circuits were tested and analysed using LT-Spice, showing clear advantages in terms of lower power usage, faster operation, and smaller size compared to traditional CMOS circuits. This project shows how memristors can help solve real limitations in today's chip design, offering a smart path forward for building the next generation of energy-efficient and scalable electronic systems. Various low power and arithmetic blocks such as multipliers have been proposed using various circuit design techniques such as CMOS low power architectures and GDI techniques [23-28].

II. LITERATURE SURVEY

The idea of resistance changes in metal oxides like TiO_2 , HfO_2 , and Ta_2O_5 dates back to the 1970s, when researchers observed that these materials could retain their resistance state even after power was removed—making them potential memory elements [11], [5]. In 1971, Leon Chua introduced the concept of the “memristor,” linking charge and magnetic flux [3]. However, it wasn't until 2008 that HP successfully built the first working memristor using TiO_2 , confirming its physical existence [16]. Earlier, in 1983, Chua's Circuit brought chaos theory into electronics, enabling the study of complex, unpredictable behaviors in hardware and inspiring applications like secure communication and image encryption [2], [6].

III. MEMRISTOR MODEL

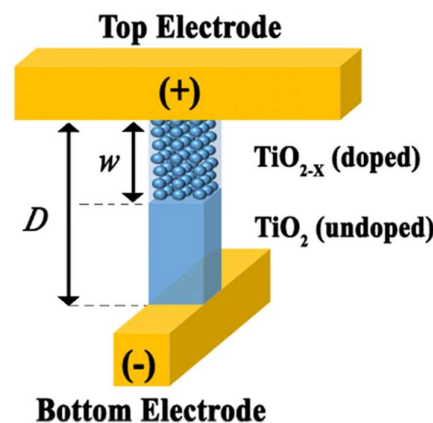


Fig. 1 Structure of Memristor

The memristor is a fascinating electronic device known for its ability to remember the amount of current that has flowed through it, even after the power is turned off. As illustrated in the Figure 1 [5], its physical structure consists of two metal electrodes typically platinum separated by a thin layer of semiconductor material. This layer is divided into two parts: the doped region (TiO_{2-x}), which conducts electricity due to the presence of oxygen vacancies, and the undoped region (TiO_2), which is more resistive. The total thickness of this material is denoted as D , while the width of the doped, conductive portion is w . When a positive voltage is applied across the electrodes, the oxygen vacancies (which are positively charged) migrate toward the bottom electrode, effectively increasing w and turning the device into a low-resistance state [5][7]. Reversing the voltage causes these vacancies to move back, reducing w and switching the memristor into a high-resistance state. The memristor's non-volatile characteristic is what sets it apart; it keeps its resistance state even after the voltage is turned off because vacancies move slowly. This switching behaviour results in a unique current-voltage relationship known as the pinched hysteresis loop, where the resistance depends not just on the current voltage but also on the device's past. The w/D ratio determines the level of conductivity, with higher values corresponding to lower resistance. These properties make memristors highly suitable for nanoscale electronic systems, especially in low-power and high-density VLSI designs [4]. Their compactness, ability to switch states using low voltages, and compatibility with CMOS technology make them promising [2][20]. The memristor model used in this paper is designed to closely replicate the behaviour of real-world memristors by adjusting specific parameters, making it highly adaptable and suitable for a variety of circuit designs. Compared to earlier models, this one offers improved simulation stability and avoids convergence issues, even when used in large-scale logic circuits with hundreds of memristors. It is particularly effective in metal-insulator-metal structured

memristors and can accurately generate output signals in complex combinational logic systems [9]. The model includes mechanisms to account for how the memristor responds differently to positive and negative voltages, influencing its resistance state. When a positive voltage is applied, the resistance decreases, representing a binary "1", and when a negative voltage is applied, the resistance increases, representing a binary "0". This switching capability allows the memristor to function as a non-volatile memory device [15]. To ensure realistic operation, the model includes threshold conditions and state-limiting functions that prevent the internal state from exceeding physical boundaries. It successfully simulates essential memristor behaviours, including the characteristic I–V hysteresis loop, which visually represents its memory effect and non-linear switching properties. Figure 2 shows the symbol of a memristor. When a positive voltage is applied to the memristor, the resistance of the memristor decreases to RON; while a negative voltage is applied to the memristor, the resistance of the memristor increases to ROFF. You can utilize the memristor model as a binary memory by using RON for "1" and ROFF for "0." Figure 2 depicts the I-V hysteresis loop of a memristor.

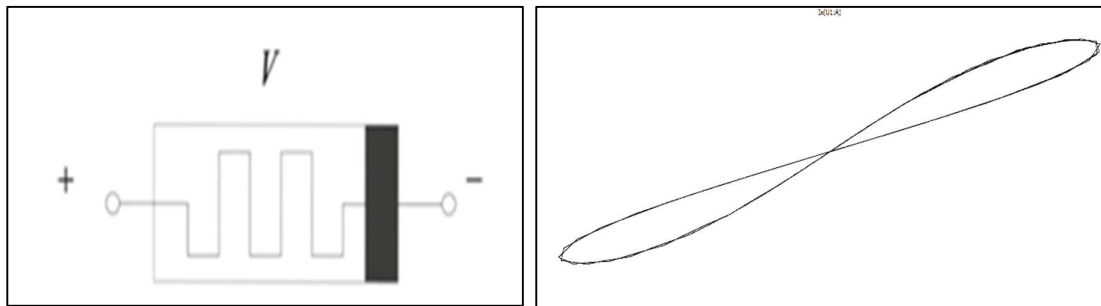


Fig 2. Symbol of Memristor and I-V Hysteresis Loop

IV. METHODOLOGY

In the proposed low-power ALU blocks, a new memristor ratioed logic (MRL) design is adopted, which significantly simplifies the circuit by using only one memristor and one NMOS transistor for each logic gate [7]. This is a major improvement over conventional memristor logic, which typically requires two memristors and two CMOS transistors [2][14]. Unlike traditional designs where output depends on voltage division, the new approach leverages the NMOS transistor's saturation and cut-off regions—controlled by gate voltage—to accurately determine the output without the need for additional inverters [7]. This not only reduces the component count but also lowers power consumption and enhances speed [21], making it ideal for energy-efficient arithmetic logic unit (ALU) operations. By integrating this logic into the ALU architecture, the overall system benefits from compactness, faster response, and better energy performance, aligning perfectly with the goals of modern low-power VLSI design [3][16].

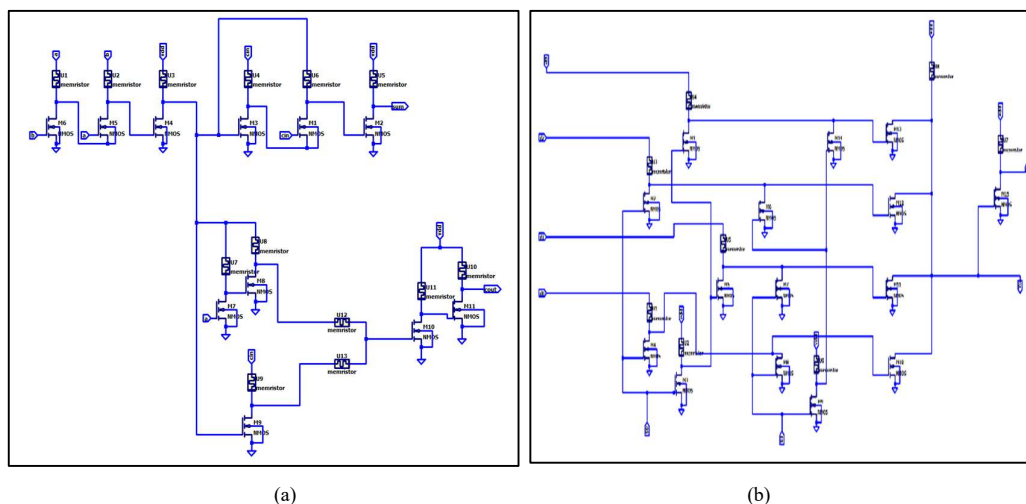


Fig 3. (a) Schematic of Full Adder, (b) Schematic of 4:1 Multiplexer

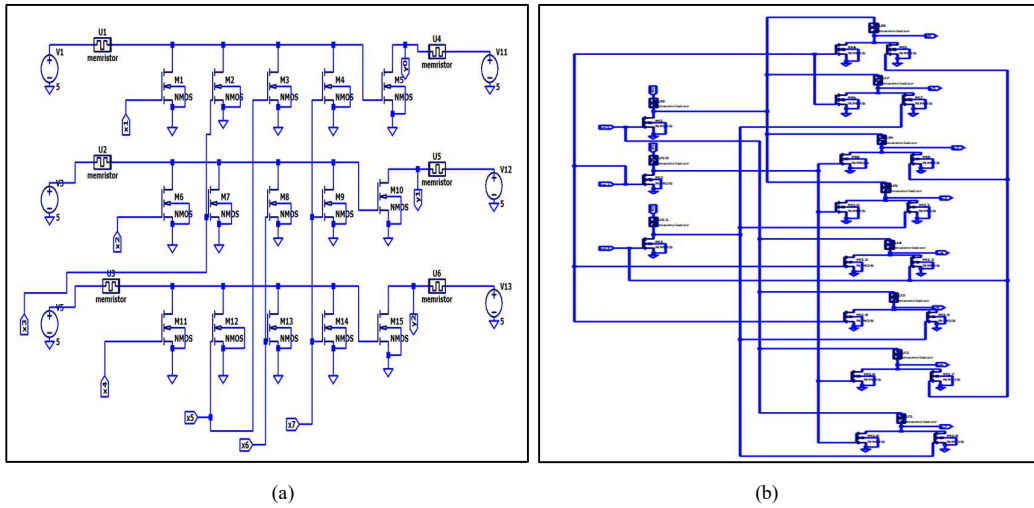


Fig 4. (a) Schematic of 8:3 Encoder, (b) Schematic of 3:8 Decoder

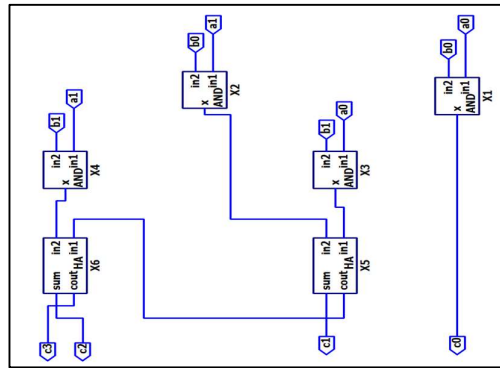


Fig 5. Schematic of 2x2 Multiplier

A low-power full adder, shown in Fig. 3(a), is built using memristor-based XNOR gates along with a 2:1 multiplexer. It takes three inputs—V_A, V_B, and V_CIN—and produces the sum and carry outputs. This simple and efficient setup makes it possible to perform addition quickly while saving both power and chip space, which is especially useful in compact digital systems. Instead of using traditional CMOS logic, memristors are used here to reduce the number of components and improve overall performance. The 4:1 multiplexer in Fig. 3(b) is another example of this efficiency. It selects one of four input lines (D0 to D3) based on control signals S1 and S2. Designed using memristor ratioed logic along with NMOS inverters and NOR gates, it uses just 15 transistors and 8 memristors, which is a big drop from the 28 transistors found in a typical CMOS version. This makes the design much more compact and power-efficient. Similarly, the 3-bit encoder shown in Fig. 4(a) uses memristors and NMOS transistors to turn inputs X1 to X7 into binary outputs Y0 to Y2. Each output bit is formed using NOR gate logic, keeping the design small. It only needs 15 transistors and 6 memristors, much less than the 40 transistors needed in standard CMOS, helping reduce power use and circuit size. The 3:8 decoder in Fig. 4(b) takes a 3-bit binary input and activates one of eight outputs (Y0 to Y7). It uses memristor-NMOS-based inverters and NOR gates, needing just 20 transistors and 12 memristors, while a traditional CMOS design would need more than 70 transistors. This leads to lower complexity, less switching noise, and better performance overall. All these circuits show how using memristor-based logic can make digital systems smaller, faster, and more energy-efficient—perfect for modern VLSI applications. As in Fig. 5 4-bit array multiplier is made using memristor-based AND gates and half adders, arranged in a simple and regular layout. It creates partial products by combining each bit of the two numbers using AND gates, then adds them up step by step with half adders. This setup allows faster processing with fewer parts. Since it uses memristors, the circuit needs less power and fewer transistors, making it a good choice for energy-efficient VLSI designs.

V. RESULTS

In this paper, we use the general memristor model to design the combinational logic circuits, in which encoder, decoder, full adder and 4:1 multiplexer is based on the new memristor ratioed logic, and the 2x2 multiplier are based on the new MRL and the multifunctional logic module. The LT-spice simulations show that the NMOS transistor has $L = 2\mu\text{m}$ and $W = 180\text{nm}$. The memristor has the same parameters, and some of the intended combinational logic circuits work the same way, including power consumption, delay and the no. of components, are calculated and compared with traditional CMOS technology.

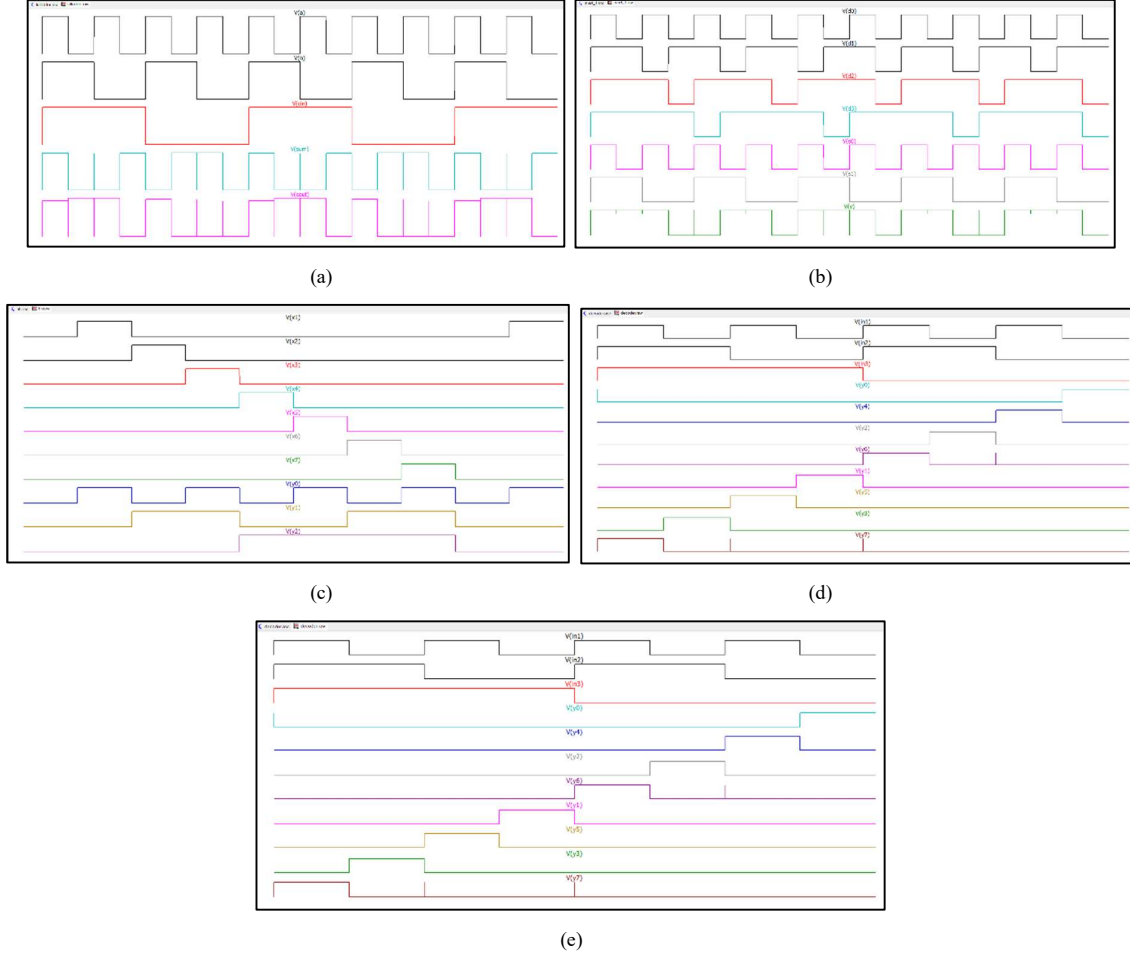


Fig 6. (a) Waveform of Full adder, (b) Waveform of 4:1 MUX, (c) Waveform of 8:3 Encoder, (d) Waveform of 3:8 Decoder, (e) Waveform of 2x2 Multiplier

As shown in Fig. 6(a) the transient simulation of the proposed memristor-based full adder confirms that the sum and carry outputs are accurate across all possible input combinations of A, B, and CIN. The waveform results clearly validate the functionality of the XNOR gates and 2:1 multiplexer used in the design. As shown in Fig. 6(b), the 4:1 multiplexer also performs as expected, selecting the correct data input based on each combination of the address lines. The output waveform confirms smooth and reliable switching behavior controlled by the select signals. Moving to the decoder, the simulation results in Fig. 6(c) demonstrate that for every 3-bit input, the circuit correctly produces a output from Y0 to Y7. The transitions are clean, with no glitches, confirming the proper decoding operation. Likewise, the encoder, shown in Fig. 6(d), provides accurate binary outputs Y0 to Y2 for each valid input from X1 to X7. The waveform transitions are stable and consistent with the expected logic of a 3-bit binary encoder. Lastly, the simulation of the 2x2 multiplier, illustrated in Fig. 6(e), confirms that it generates the correct 4-bit result for all input combinations. The waveforms reflect accurate partial product formation and addition, demonstrating the reliable performance of memristor-based logic in arithmetic circuits.

TABLE I: COMPARISON TABLE OF TRANSISTOR COUNTS

Arithmetic Circuits	CMOS based circuit	Memristor based circuit	% Area Reduction
Full adder	28T	24(11T+ 13M)	56.07
4:1 MUX	28T	23 (15T+8M)	43.57
8:3 Encoder	54T	21 (15T+6M)	71.11
3:8 Decoder	40T	30(19T+11M)	49.75
2x2 Multiplier	48T	40 (s20T+20M)	54.17

Table 1 gives the area reduction estimate of each circuit by 50%-72% based on studies of HP LABS [22] which states that the area of memristor is 0.01 times the CMOS area. Here, T stands for transistors and M stands for memristors. By comparing with existing works such as [19], [10], and [17] and the no. of transistors were reduced [18]. While the 2×2 multiplier uses the most components, the optimized memristor-based design ensures efficient performance.

TABLE II: COMPARISON TABLE FOR POWER MEASUREMENT

Circuits	CMOS based circuit	Memristor based circuit	% Power reduction
Full Adder	57.13uW	950.11nW	98.34
8:3 Encoder	18.92uW	202.11nW	98.93
3:8 Decoder	61.51uW	757.3nW	98.77

Figure 7 is Graphical representation to indicate almost 100% drop in CMOS and proposed Hybrid circuits. When we look at the power usage of these circuits, it's clear that memristor-based designs help to save about 98% of power saving. This gives almost 100% energy optimisation compared to the traditional CMOS circuits. Especially in circuits like the decoder, the drop in power is quite noticeable. Three circuits in Table 2 indicate the power drop in three basic circuits used in arithmetic blocks. This shows that memristors are a better choice when we want to build low-power digital circuit-based systems.

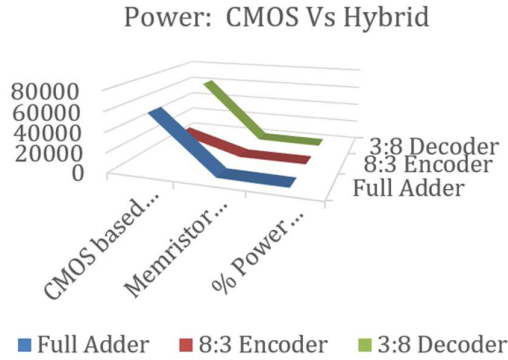


Fig 7. Power CMOS vs. proposed Memristor circuits.

V. CONCLUSION

The work demonstrates the effectiveness of using Memristor Ratioed Logic (MRL) and multifunctional memristor-based modules in the design of combinational arithmetic logic circuits. The proposed approach, verified through LT-Spice simulations, shows significant advantages over traditional CMOS and other memristor-based logic designs. The proposed circuits in this exhibit reduced component count, improved accuracy, lower time delay, minimized chip area, and decreased power consumption. These results highlight the potential of hybrid CMOS–memristor architectures as a promising solution for developing efficient, scalable, and low-power digital systems in future VLSI applications.

REFERENCES

- [1] G.N. Balaji, V. Aathira, K. Ambhikavathi et al., Combinational circuits using transmission gate logic for power optimization. *Int. Res. J. Eng. Technol.* 03, 649–654 (2016)
- [2] K. Cho, S.J. Lee, K. Eshraghian, Memristor-CMOS logic and digital computational components. *Microelectronics. J.* 46, 214–220 (2015)
- [3] L.O. Chua, Memristor: the missing circuit element. *IEEE Trans. Circuit Th.* 18, 507–519 (1971)

- [4] N. Z. B. Haron, S. Hamdioui, Why is CMOS scaling coming to an END? in The 3rd IEEE International Design and Test Workshop (2015), pp. 98–103
- [5] Pal, S., Bose, S., & Islam, A. (2022). Design of memristor based low power and highly reliable ReRAM cell. *Microsystem Technologies*, 28(3), 793–807.
- [6] S. Kvatinisky, D. Belousov, S. Liman et al., MAGIC-memristor-aided logic. *IEEE Trans. Circuits Syst. II*(61), 895–899 (2014)
- [7] S. Kvatinisky, N. Wald, G. Satat, et al., MRL–Memristor Ratioed Logic, in 2012 13th International Workshop on Cellular Nanoscale Networks and their Applications (2012), pp.1–6
- [8] M. Meghelli, A 132-Gb/s 4:1 multiplexer in 0.13- μ m SiGe-bipolar technology. *IEEE J. Solid State Circuits*. 39, 2403–2407 (2014)
- [9] S. Oblea, A. Timilsina, D. Moore, et al., Silver chalcogenide based memristor devices, in 2010 International Joint Conference on Neural Networks (2010), pp. 1–3
- [10] S. Panda, A. Banerjee, B. Maji et al., Power and delay comparison in between different types of full adder circuits. *Int. J. Adv. Res. Elect. Elect. Instrumentation. Eng.* 1, 168–172 (2012)
- [11] S. Pi, C. Li, H. Jiang et al., Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension. *Nat. Nanotechnology*. 14, 35–40 (2019)
- [12] S. G. Rohani, N. Taherinejad, D. Radakovits, A semiparallel full-adder in IMPLY logic. *IEEE Trans. Very Large Scale Integ. Syst.* 28, 297–301 (2020) *Circuits, Systems, and Signal Processing*
- [13] Singh, Memristor based XNOR for high speed area efficient 1-bit Full Adder, in 2017 IEEE International Conference on Computing, Communication and Automation (2017), pp. 1549–1553
- [14] T. Singh, Hybrid memristor-CMOS (MeMOS) based logic gates and adder circuits. *Computer Sci.* 1506, 1–11 (2015)
- [15] Singh, Design and analysis of memristor-based combinational circuits. *IETE J. Res.* 33, 182–191 (2020)
- [16] D.B. Strukov, G.S. Snider, D.R. Stewart, The missing memristor found. *Nature* 453, 80–83 (2008)
- [17] M. Teimoory, A. Amirsoleimani, A. Ahmadi, et al., A hybrid memristor-CMOS multiplier design based on memristive universal logic gates, in 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (2017), pp. 1422–1425
- [18] K. Ganesh, K. S. V. S. Rakesh, R. M. Joany, and E. A. Devi, “Low Power 3-Bit Decoder Design Using Memristor,” in *Proc. 2024 2nd World Conf. Commun. Comput. (WCONF)*, Raipur, India, Jul. 12–14, 2024, pp. 1–6, doi: 10.1109/WCONF61366.2024.10692243.
- [19] Y.Sreenivasulu Goud, K.Sai Vara Prasad, "Design and Implementation of Low Power 3-bit Encoder Using Memristor on LTSpice," in *Proc. 2024 IEEE Int. Conf. Inf. Technol., Electron. Intell. Commun. Syst. (ICITEICS)*, (2024).
- [20] L. Xie, H. A. D. Nguyen, M. Taoui, et al., A mapping methodology of boolean logic circuits on memristor crossbar. *IEEE Trans. Computer Aided Des. Integrated Circuits Syst.* 37, 311–323 (2018)
- [21] Vinay G, Kiran A Gupta, “MAC Unit Implementation using Hybrid-Memristor Ratioed Logic”. 2024 3rd International Conference for Advancement in Technology (ICONAT),1-5 (2024).
- [22] Cha et al., "Defect Analysis and Cost-Effective Resilience Architecture for Future DRAM Devices," 2017 IEEE International Symposium on High Performance Computer Architecture (HPCA), Austin, TX, USA, 2017, pp. 61-72, doi: 10.1109/HPCA.2017.30.
- [23] Kiran Agarwal Gupta, Dinesh K Anvekar, V. Venkateswarlu, “Modeling of Short Channel Devices and Analysis of Design aspects for Power Optimization” *International Journal of Modeling and Optimization*. IJMO 2013 Vol.3(3): pp.266-271
- [24] V. Pramath, G. Pavithra, S. S. Ninawe, "Advancements in Operational Transconductance Amplifiers (OTAs) for Design, Applications & Performance Optimization Techniques with Hardware Implementation," 2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), Kolkata, India, 2024, pp. 542-547, doi: 10.1109/EDKCON62339.2024.10870654.
- [25] K Shanthala, BM Chandrakala, N Shobha, Deepashree D, “Automated Diagnosis of brain tumor classification and segmentation of MRI Images ”, 2023 International Conference on the Confluence of Advancements in Robotics, Vision and Interdisciplinary Technology Management (IC-RVITM), 28-29 November 2023, Bangalore, India
- [26] Monika Katta, T.K. Ramesh, Juha Plosila, AS-Router: A novel allocation service for efficient Network-on-Chip, *Engineering Science and Technology, an International Journal*, Volume 50, 2024, 101607, ISSN 2215-0986, <https://doi.org/10.1016/j.jestch.2023.101607>
- [27] Tejas R., Venkatesh L., Shivamadu D.N., Ravishankar K., Ninawe S.S., Gunjal S.G.H., Pavithra G., "Design & Development of an Automatic Defense System for Warfare Applications", (2024) 15th International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT 2024, 2, pp. 6711 – 6716.
- [28] Pavithra G., Ninawe S.S., Sandeep K.V., Fawad I., "Development of hybrid algorithms for the detection of Infectious Diseases from the X-Ray's images of the Chest Structure of Human Beings" (2024) *Proceedings - ICNEWS 2024: 2nd International Conference on Networking, Embedded and Wireless Systems: Wireless Technology - Building a Digital World*. DOI:10.1109/ICNEWS60873.2024.10731056