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Design a Vedic Multiplier using Xilinx Vivado

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***Abstract*— This research investigates the usage of traditional Indian Vedic multiplier, array multiplier, and Wallace tree multiplier. The main focus of high- speed processors is to minimize power consumption and processing times, which is effectively demonstrated by the Indian Vedic multiplier. The implementation of the design utilizes Verilog, a hardware description language, and the testing phase is carried out using the Modelism simulator. The study compares the performance of these multipliers. The outcomes emphasize that when a ripple carry adder is employed, the Indian Vedic multiplier outperforms both in terms of power consumption and time delays.**

***Index Terms*— Vedic multiplier, array multiplier and Wallace tree multiplier and ripple carry adder.**

I. INTRODUCTION

Vedic multiplication is a method that was taken from the Vedas, a vast collection of religious literature that originated in ancient India. The Vedas are a body of mathematics that was used in ancient India. Numerous computing methods, including multiplication strategies, are included in Vedic mathematics. One of the multiplication methods used in Vedic mathematics is the Vedic multiplier, also known as "Nikhilam Sutra" or "Vertically and Crosswise" multiplication. Vedic multiplication has benefits over conventional multiplication techniques and other multiplication algorithms. There are numerous different kinds of multipliers, including array multipliers, Wallace tree multipliers, Vedic multipliers, When compared to other multipliers, the Vedic multiplier has a shorter delay. The main application of this method is to quickly multiply large numbers.

II. MULTIPLICATION OF TWO DECIMAL NUMBERS BY VEDIC MATHEMATICS

Multipliers serve as essential elements within digital circuits and computer architecture, enabling the execution of multiplication operations on binary numbers. The design of multipliers involves various algorithms and architectures, each offering unique advantages and trade-offs. A multiplier is an electrical circuit that multiplies two binary integers in digital circuits, like those found in computers. It was constructed using binary adders. Vertical and crosswise methods are two different approaches within the Vedic Mathematics framework for performing fast multiplication. Both methods are based on ancient Indian mathematical techniques and are used to multiply large numbers more efficiently than traditional multiplication methods.
As depicted in Figure 1, consider two three-digit numbers ancient Vedic method of multiplication employed to obtain the product of these decimal numbers, as shown in the same figure. Using vertical and crosswise multiplication, the technique yields the product of the two numbers.

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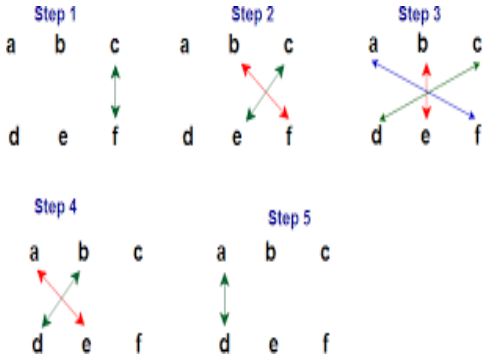

Fig.1.Vedic Multiplication of two decimal numbers

II. VEDIC MULTIPLIER

The Urdhva triyakbhyam formula is a well-known multiplication technique rooted in Vedic mathematics, consisting of 16 sutras. It is a universal method that was utilized in ancient India to speed up the multiplication process. The "Urdhva- Tiryakbhyam" sutra, also known as "Vertically and Crosswise," is widely employed in digital circuits for Vedic multiplication. This approach breaks down the process into smaller, more manageable steps, making it easier to perform mentally and suitable for implementation in hardware circuits.

*A. 2*2 Vedic multiplier*

In this section, we will be discussing the 2*2 Vedic multiplier. The block diagram for this multiplier can be seen in Figure 1. It utilizes two half adders in its design. Consider the values of a being 1:0 and b being 1:0. Fig 2 showcases the output of decimal numbers using Vedic multiplication. Initially, the output is obtained directly from a0b0. The values of a0b1 and a1b0 are processed by a half adder, and the resulting sum is taken as an output. The carry and the value of a1b1 are then passed on to another half adder. In total, the output of this is 4 bits binary length.

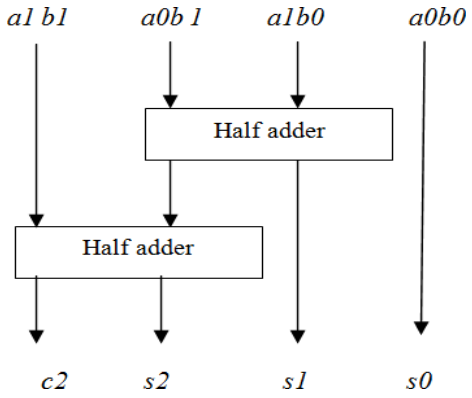

Fig. 2.Circuit diagram

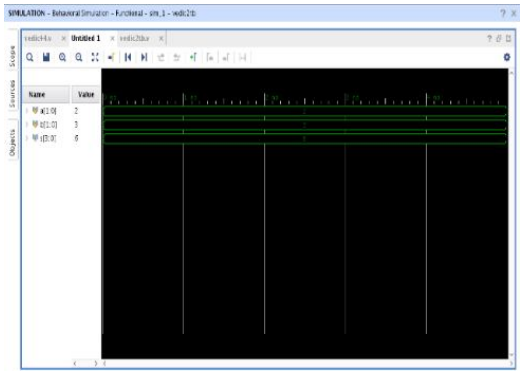

Fig.3.Output

*B. 4*4 Vedic multiplier using ripple carry adder*

1. Ripple carry adder

A ripple carry adder (RCA) is a circuit utilized for performing addition of multiple binary values. Its name is derived from the fact that the carry bit ripples through each full adder sequentially. Within this circuit, each full adder computes a sum and a carry output by adding the input bits alongside the carry bit obtained from the preceding stage. this is relatively straightforward and easy to design, its speed is confined by the propagation delay of the carry signal.. A delay proportionate to the number of bits being added results from the carry bit having to travel through each stage of the adder. This can cause substantial delays with bigger adders.

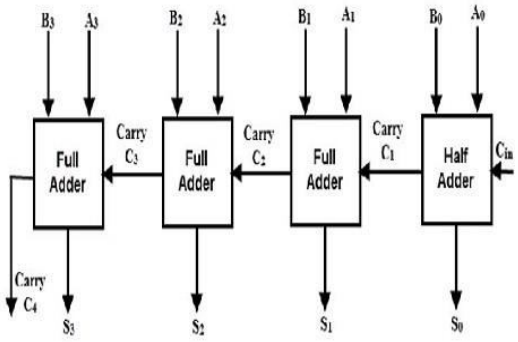

Fig.4. Ripple Carry Adder

*C. 4*4 Vedic Multiplier*

This section outlines the functioning of the 4x4 Vedic multiplier, depicted in Figure 2. This employs three 16-bit adders, four 8-bit Vedic multipliers, and a half adder. The inputs, as illustrated in the diagram, are processed to produce the output, which represents the product of the inputs A[3:0] and B[3:0].

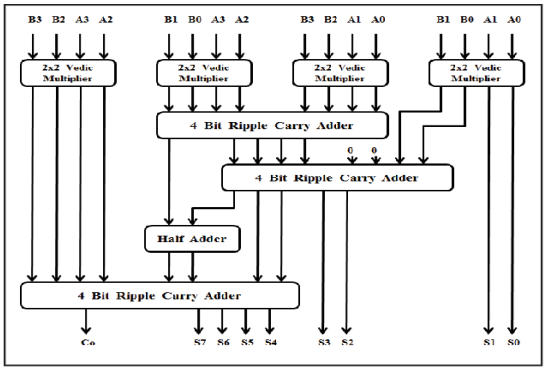

Fig. 1. Block Diagram of 4 bit Urdhva multiplier with Ripple carry adder

Fig.5.Block Diagram

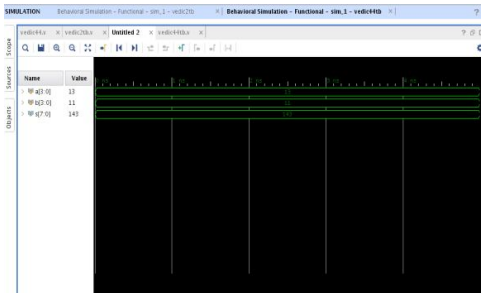

Fig.6.Output

IV Array Multiplier

The construction of the array multiplier is characterized by its regular structure, which facilitates the building process. When multiplying unsigned numbers using an array multiplier, it utilizes full adders and half adders.

These adders are connected in horizontal, vertical, and diagonal arrangements to combine the partial products. In the case of employing complete adders for the initial row of partial products in an array multiplier, Cin is assumed to be '0'. By employing basic routing techniques, precise alignment of partial products can be accomplished without requiring extra logic. Every row of adders generates a fresh partial sum and a sequence of carries by adding a partial product to the sum. Constructing an nxn array multiplier necessitates N (n-2) full adders, N half adders, and N 2AND gates. The delay linked with the array multiplier is determined by the time needed for signals to propagate through each AND gate, full adder, and half adder. A significant drawback of array multipliers is their substantial size, as the linear array size increases exponentially with the number of operands. Moreover, the array multipliers encounter propagation delays caused by the various steps involved in logic operations. In scenarios where high-speed processing is required, these delays can present a notable challenge.
In conclusion, although array multipliers are conceptually and physically simple, their drawbacks in terms of speed, hardware complexity, power consumption, and scalability make them less suited for some applications, especially when compared to more sophisticated multiplication algorithms.

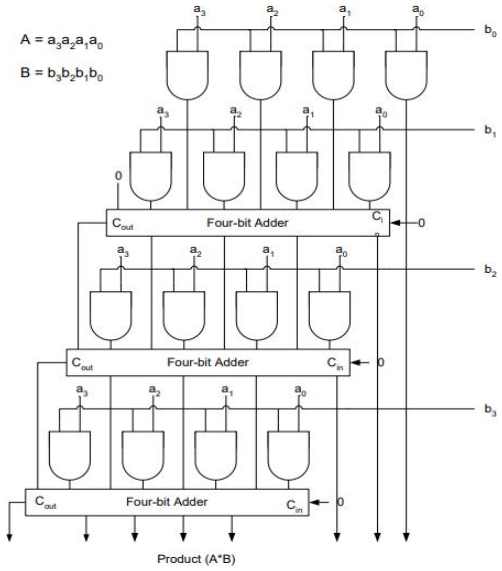

Fig.7.Block Diagram

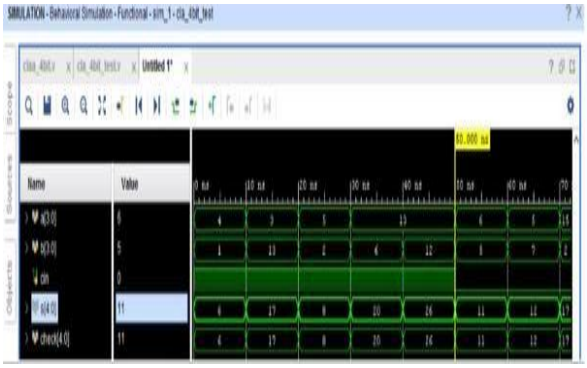

Fig.8.Result

V. WALLACE TREE MULTIPLIER

It uses technology that multiplies integers using a simple and effective approach called column compression. The exceptional swiftness of Wallace trees can be attributed to the logarithmic relationship between delay and word length of the operand in the multiplier, which sets them apart from the linear connection commonly observed in array multipliers. The functioning of the Wallace Tree Multiplier involves three primary steps: the creation of partial products, the grouping of these products, and the execution of addition utilizing adders. An effective multiplication technique used in digital circuit design is the Wallace Tree Multiplier, particularly for high-speed multiplication in microprocessors and digital signal processors. This technique efficiently separates partial

products into positive, negative, and zero groups before combining them, which speeds up multiplication operations, uses less energy, and scales to handle enormous binary values.

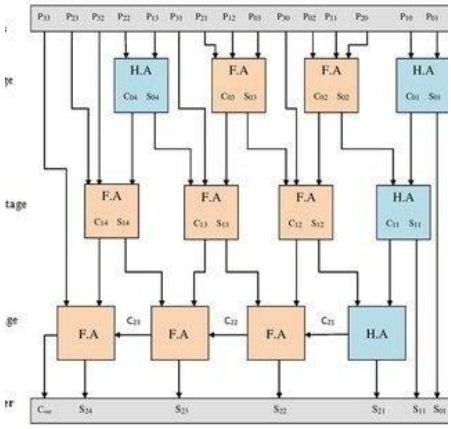

Fig.9.Block Diagram

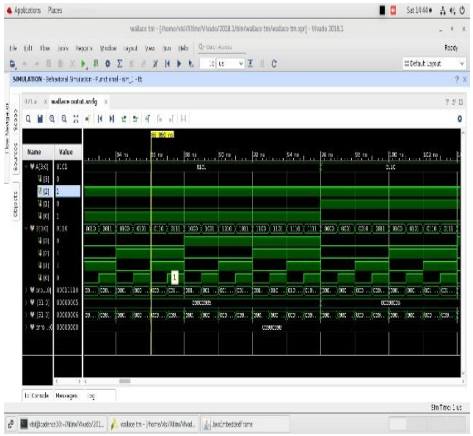

Fig.10.Output

VI. RESULT

The Vedic multiplier, array multiplier, and Wallace tree multiplier were developed using Verilog hardware description language, with simulations conducted in Model Sim. Table 1 presents a comparison of total power, dynamic power, number of LUTs, and total delays. The results indicate that the Vedic Multiplier, when utilizing carry select adder, exhibits lower power consumption than the array multiplier and Wallace tree multiplier.

TABLE 1: COMPARISION TABLE OF ALL MULTIPLIERS

S. No	TYPES OF MULTIPLIERS	WALLACE TREE MULTIPLIER	ARRAY MULTIPLIER	VEDICMULTIPLIER
1	TOTAL POWER	4.406 W	4.347 W	4.32 W
2	DYNAMIC POWER	4.141 W	4.090 W	4.065 W
3	SLICE LUT'S	18	15	19
4	TOTAL DELAYS	16	16	16

VI. Conclusion

Utilizing Xilinx Vivado, the successful implementation of the Vedic multiplier has been achieved. In comparison to the array multiplier and Wallace tree multiplier, the Vedic multiplier, which integrates a ripple carry adder, exhibits reduced power consumption. It can be confidently concluded that the Vedic Multiplier outperforms in multiple areas such as delay and power efficiency. Thorough verification has been performed to ensure the functionality and outputs of the Vedic multiplier.

References

[1] Yogendra and Anil Kumar Gupta," Design of High Performance 8-bit Vedic Multiplier", International Conference on Advances in Computing, Communication, & Automation (ICACCA), September 2016.

[2] S. Jayakumar and S. Sumathi, "High – Speed Vedic Multiplier for Image Processing using FGPA," IEEE/10th International Conference on Intelligent Systems and Control (ISCO), January 2016.

[3] Rendlesham Gupta, Rajdeep Shar, K. L. Baishnab Jishan Mehedi, "Design of high performance 8-bit Vedic Multiplier using compressor," IEEE/International Conference on Advances in Engineering and Technology (ICAET), May 2014.

[4] J. Vinoth Kumar and C. Kumar Charlie Paul., "Design of Modified Vedic Multiplier and FPGA implementation in Multilevel 2d-DWT for Image Processing Applications," Second International Conference on Current Trends in Engineering and Technology - ICCTET 2014, July 2014.