

Comparative Analysis of basic Sequential Circuits based on CMOS and Graphene Nano Ribbon Transistors

Ravisham Santha¹, D. Aneesh Bharadwaj² and Dr. Vasundhara Patel K.S³

¹BMS College of Engineering, Bangalore, India

Email: ravisham.lvs20@bmsce.ac.in

²⁻³BMS College of Engineering, Bangalore, India

Email: devarakoda.lvs20@bmsce.ac.in, vasu.ece@bmsce.ac.in

Abstract—The Graphene Nano Ribbon Field Effect Transistor (GNRFET) based sequential Circuits like D Flip-Flop and counters are presented in this paper. Further, the circuits are also designed using different techniques like the TSPC and PTL. Circuits are simulated using the industry standard HSPICE simulation tool and using SPICE compatible compact model of GNRFET. Simulation results show that GNRFET has a great potential in sequential circuits. Between the two architectures of the GNR implementations, the PTL based circuits are more efficient since, they exhibit better performance.

Index Terms— GNRFET, D Flip-Flop, counters, TSPC, PTL.

I. INTRODUCTION

As the deep submicron ICs are being used in the current day scenario, a lot of issues arise in case of the CMOS transistors. Due to these increasing issues of the CMOS, alternatives like Graphene Ribbons and Nanotubes are being investigated.

MOS technique is one of the most well-known technique in the chip design industry and widely used today to compose integrated circuits in several miscellaneous applications. MOS technology tends to show some disadvantages as we start approaching the submicron technology. In the scaling process some second order effects like channel length modulation, threshold voltage, hot carrier effect and temperature dependency are showing enhanced effect on the working of a CMOS. To avoid these problems newer non-silicon-based technology like Graphene Ribbons and Nanotubes are used as substitutes.

Graphene, which is a monolayer of carbon atoms packed into a 2-D honeycomb lattice, has emerged as a promising candidate material for beyond-CMOS Nano electronics. Graphene-based devices offer high mobility for ballistic transport, high carrier velocity for fast switching, monolayer thin body for optimum electrostatic scaling, and excellent thermal properties. The potential to produce wafer-scale graphene films with full planar processing for devices promises high integration potential with conventional CMOS fabrication processes.

Primarily, the transition from MOS transistors to GNR transistors was a step taken in order to overcome or mitigate the short channel effects in the MOS transistors [1] such as power dissipation, sub-threshold leakage,

and drain-induced barrier lowering (DIBL). GNRFET has the potential to be substitute to the traditional CMOS based transistors.

The performance of the I-V characteristics of GNRFETs is an important parameter in order to understand the reality of replacing it with the traditional MOS transistors. Maziar et al. [2], proposes a method to study the I-V characteristics for different widths and lengths studied in terms of sub-threshold swing, saturation behaviour, leakage current and on-current density.

The implementation of circuits in any technology primarily begins with the implementation of the inverter, in order to study its characteristics and use the same information for other circuits. A performance optimized inverter has been implemented in [3], using the 32 nm GNR technology node, where there is a 2.5 x improvement in terms of delay and PDP.

Since the implementation of sequential circuits was the main motive of this work, the understanding of basic sequential element, a flip-flop is necessary to proceed further. Zarin et al., proposes a method to implement a ternary logic-based Master-Slave D Flip-Flop. Along with the concise understanding of the performance of Flip-Flops implemented using the GNRFET, the concept of Multi-Valued logic is also introduced.

Even in case of Flip-Flops, various modifications have taken place with respect to the primarily available Master-Slave flops, using the dynamic CMOS logic. Papers [7, 9,10] have various implementation of these TSPC based flops in order to have a comprehensive knowledge about its working and understanding the reason behind the low power operation of the TSPC based circuits.

Another logic that attracts major attention due to its lower PDP and simplicity is the Pass-Transistor logic. The flops implemented using this design [8] has a great deal of reduction in terms of delay, and the power when implemented using the 32 nm GNRFET is slightly higher than the TSPC, but the delay is very less. This enables us to use the above-mentioned flops.

The present paper continues the discussion organized as follows. The D Flip-Flops and counters are introduced in section II. In section III indicates the circuit implementation as described. Section IV discusses the Simulation and results. Section V draws conclusion.

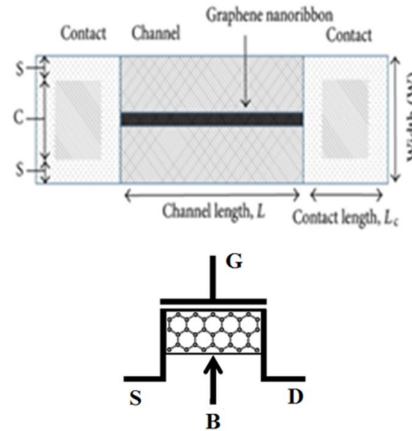


Fig. 1. Top view of GNRFET and its symbol

II. D FLIP-FLOPS AND COUNTERS

A. D Flip-Flop

In today's world, the VLSI designer totally dependent on Flip-flops as it has wide range of applications in various field of electronics. Flip-flops are widely used in spacecraft for numerous processes; these are also used in telecommunication sector to exchange the information and store the data. The functionality of the integrated circuit is controlled by using flip-flops. As an essential component of sequential circuits, Flip-Flops have a large impact on the area, speed and power consumption of modern digital circuits. Flip-flops can be built using either static or dynamic design. Static flip-flops are usually designed with two inverter-based latches that have a large impact on area and delay. However, flip-flops based on dynamic logic have advantages in high operating speed and area density compared to static ones.

Most flip-flops require both clock signal and its inversion, which challenges clock tree synthesis. However, True Single-Phase Clock (TSPC) Flip-Flop, a dynamic flip-flop, needs only a single clock signal. Using single phase

clock and dynamic logic do not only lead to compact design but also faster response. In addition, a unique feature of TSPC flip-flop is the reduction of the overall setup time and delay obtained by embedding logic gates inside the structure. For these reasons, TSPC flip-flop is widely used in many high-speed applications.

Pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, this reduces the number of active devices. The Pass Transistor Logic (PTL) is a better way to implement circuits designed for low power applications.

The power consumption in a circuit can be decreased by reducing the switching activity in the circuit and switching capacitance of each node. Using the Pass Transistor logic also helps in decreasing the short-circuit Current. The work contains the different implementations of the D-FF and the comparison with its CMOS counterparts.

B. Counters

A digital circuit that is used for counting pulses is known as a counter. The counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied. Counters are of two types: Asynchronous or ripple counters and synchronous counters. In an asynchronous counter, the output of the first flop (Q) is given as the clock of the consequent counter. The biggest disadvantage of this counter is that there will be a bigger delay as we have to wait for the output of one Flip-Flop to drive the next one. And in the case of Synchronous counters, the clock is given to all the Flip-Flops. This decreases the delay but increases the number of combinational circuits in between each Flip-Flop.

III. GNR AND CMOS BASED CIRCUITS

Design and simulations TSPC based D Flip-Flop, Pass Transistor Logic based D Flip-Flop, 2-Bit Counter using both GNRFET and CMOS are described in this section.

A. Basic gates using MOSFET and GNRFET

Inverter is the most basic logic which is shown in Fig.2 and NAND gate is shown in Fig.3.

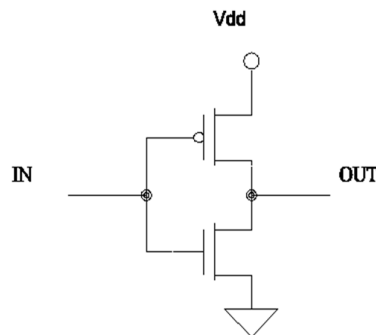


Fig. 2. CMOS NOT gate

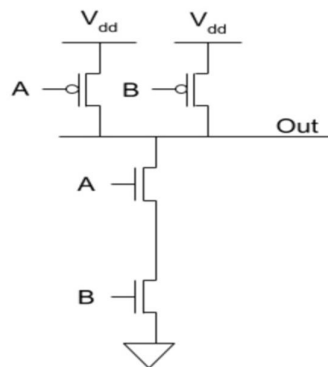


Fig. 3. CMOS NAND gate

XOR gate is designed using four 2-input NAND gates, and it is shown in Fig.4.

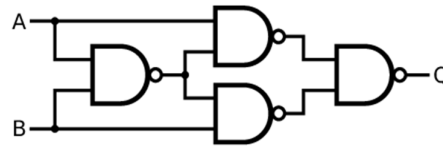


Fig. 4. XOR gate using NAND gates

B. TSPC D Flip-Flop

True Single-Phase-Clock Flip-Flop (TSPC) performs the flip-flop operation with little power and at high speeds. However, dynamic flip-flops will typically do not work at static or low clock speeds given enough time, leakage paths may discharge the parasitic capacitance enough to cause the flip-flop to enter invalid states. The architectures of True single phase clock Flip-Flop based on edge triggering i.e., positive, negative, and positive edge triggered using split output latches.

From the three architectures we consider negative edge trigger for dynamic latches are currently the principal design style for high-speed digital circuits. Because NMOS devices provide stronger pull-down, usually use negative edge-triggered devices in CMOS. As Negative Edge trigger architecture is selected for our TSPC Flip-Flop in that CMOS based circuit the first stage is Non-Pre-charged N then output of that is applied as input to the Pre-charged P stage and at last the output of these is given to Non Pre-charged P stage output of these stage is then complement it by simply connected invert at the output side which shown in following figure ,now for resetting the Negative edge TSPC circuit we connect one PMOS transistor at the output stage of non-Pre-charged P stage it connected between VDD and the output path of Flip-Flop. The single phase of clock is applied to the all the stages of below TSPC Flip-Flop so that it is known as True Single Phase Clock Flip-Flop. Total 12 transistors are required for following circuit including resetting logic.

The advantage of using the TSPC based Flip-Flop in the designs for low power implementations also has a downside that, it can only be function at frequencies in the range of MHz, which is why the simulations have also been carried out keeping that in mind.

At higher frequencies, there are probabilities of glitches in this circuit, which is not very favourable, because of which it is advisable to use it at lower frequencies.

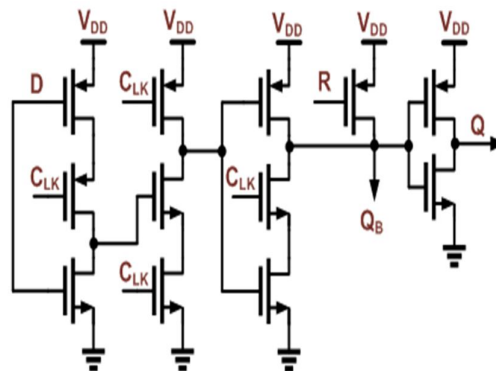


Fig. 6. Circuit of TSPC based D Flip-Flop

C. PTL D Flip-Flop

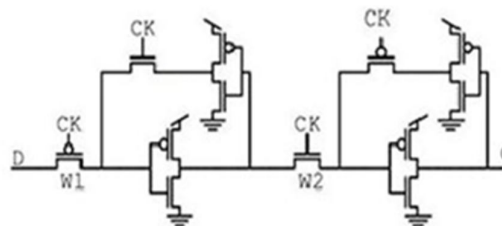


Fig. 7. Circuit of Pass Transistor Logic based D Flip-Flop

2-Bit Counter design using sub circuits

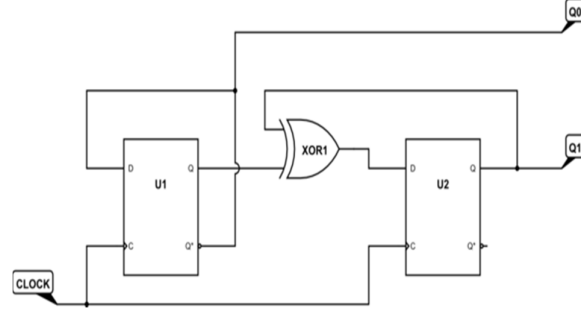


Fig. 8. 2-Bit Counter

IV. SIMULATION AND RESULTS

The circuits mentioned above have been designed and implemented using the 32 nm library in the HSpice tool. The Master-Slave and the PTL based circuits have been simulated at a frequency of 4 GHz and the TSPC based circuit has been implemented at a frequency of 100 MHz.

The waveforms of the TSPC based D Flip-Flop and the 2-Bit Counter have been indicated in fig. 9 and fig. 10, respectively.

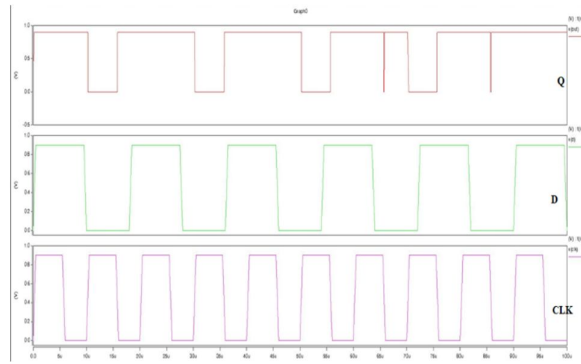


Fig. 9. Waveform of TSPC based D Flip-Flop

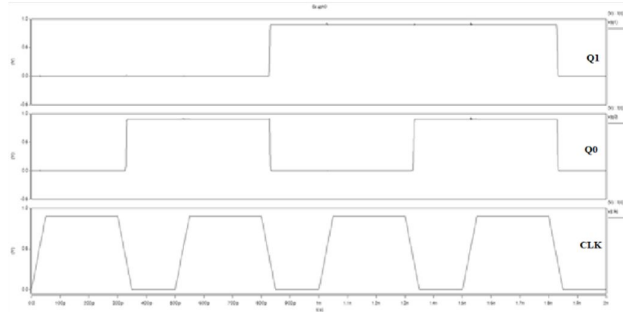


Fig. 10. Waveform of 2-Bit Counter

Post the completion of the simulation, the computation of the power, delay as well as the PDP is done, which opens up the case for mathematical proof as to why the GNR based circuits have a better performance in terms of both power and delay.

Table I contains the values of power, delay, as well as PDP for the CMOS and GNR implementation of Master-Slave and PTL based D Flip-Flop. It can be observed that the power in case of GNR implementation of both Master-Slave and TSPC based D Flip-Flops have reduced by 6.29 μ W and 3.499 μ W. The delay has correspondingly reduced by 66.64 ps and 37.69 ps respectively. This indicates that the PTL flop using GNR FET is the most efficient of the four implementations.

TABLE I. VALUE OF POWER, DELAY AND POWER-DELAY PRODUCT FOR MASTER-SLAVE AND PTL BASED D FLIP-FLOP

Architecture (32nm)		Power (μ W)	Delay (ps)	PDP
CMOS	34T DFF	10.87	82.6	897.862
GNR	34T DFF	4.58	15.96	73.0968
CMOS	PTL DFF	6.008	53.96	324.19168
GNR	PTL DFF	2.509	16.27	40.82143

TABLE II. VALUE OF POWER, DELAY AND POWER-DELAY PRODUCT FOR TSPC BASED D FLIP-FLOP

Architecture (32nm)		Power (μ W)	Delay (ns)	PDP
CMOS	TSPC DFF	3.577	124.6	445.6942
GNR	TSPC DFF	1.268	29.718	37.682424

In case of TSPC based flops, the tabulation been done separately as the simulation frequency is lesser and the delay is procured in terms of nanoseconds. Therefore, the comparison can be done with respect to CMOS and GNR implementations of the same. Table II has the values of the power, delay, and PDP. It can be observed that the PDP of the GNR TSPC flop has improved by 91.6 %.

Similarly, the tabulation has been done for the 2-Bit counters for all the 3 types of architectures. It is observed that the value of PDP for both Master-Slave and PTL flop based 2-Bit counters, in GNR based transistors is much lesser when compared to the CMOS based implementation.

TABLE III. VALUE OF POWER, DELAY AND POWER-DELAY PRODUCT FOR 2-BIT COUNTER USING MASTER-SLAVE AND PTL BASED D FLIP-FLOPS

Architecture (32nm)		Power (μ W)	Delay (ps)	PDP
CMOS	34T DFF	18.05	57.85	1044.1925
GNR	34T DFF	7.834	4.9218	38.5573812
CMOS	PTL DFF	10.338	45.8	473.4804
GNR	PTL DFF	5.309	14.68	77.93612

TABLE IV. VALUE OF POWER, DELAY AND POWER-DELAY PRODUCT FOR 2-BIT COUNTER USING TSPC BASED D FLIP-FLOPS

Architecture (32nm)		Power (μ W)	Delay (ps)	PDP
CMOS	TSPC DFF	6.095	102.6	625.347
GNR	TSPC DFF	3.012	33.56	101.08272

Finally, in case of the TSPC based CMOS and GNR counters, the Table IV. indicates that the PDP reduces by an amount of 83.84 % in case of GNR based counters, which when used in a much bigger block having multiple flops will increase the significance of the GNR implementation.

V. CONCLUSION

The existence of sequential elements in the real time applications necessitates the existence of the low power functioning of the circuits. Also, due to the shortcomings of CMOS transistors in case of the submicron technologies, such as the short-channel effects, the usage of GNR based transistors was necessary.

The work taken up in this project was to implement the basic gates and sequential elements such as the flip-flop and a counter, using the CMOS and GNR based transistors. Further, the improvement was to implement the flops using different techniques like the TSPC and PTL. After simulating all these circuits, the power, delay as well as the PDP was computed and the comparison was drawn between the different architectures of GNR and CMOS.

The TSPC based flops were simulated at a frequency of at 100 MHz. In case of Flip-Flops, there is a decrease of 90.17 % and 87.6 % of the PDP for the TSPC and PTL based flops. When the PDP has been computed for a 2-Bit counter, there has been a decrease of 83.7 %, 83.84 % in case of TSPC, PTL based GNR/FET implementations. It is hence desirable to use the GNR based implementation instead of pure CMOS circuits to

improve the performance of the circuit along with consumption of low power. Between the two architectures of the GNR implementations, the PTL based flops are more suitable since, they function properly at higher frequencies as well as are efficient in terms of power and delay.

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