Grenze International Journal of Engineering and Technology, June Issue

Implementation and Performance Analysis of Various Scan Compression Techniques

Shreya Patel[1], Urmila Pariya[2], Divyesh Nariya[3] and R.A. Thakker[4]
[1-2]Department of ECE, GTU – GSET, Ahmedabad, India
Email: shreya.sandy13@gmail.comurmilapariya081@gmail.com
[3]Lead Engineer, MicroCircuits Technology, Ahmedabad, India
Email: divyeshnariya009@gmail.com
[4]Adjunct Professor, GTU - GSET Ahmedabad, India
Email: rathakkar@gtu.edu.in

***Abstract*—In today's scenario, the number of transistors on a chip has increased to several millions. If number of scannable flops also increases in design; FULL-SCAN test patterns are very costly to use. They also require more memory to store the test data on Automatic test equipment and takes longer time to test. In this work, we have investigated two different scan compression techniques to compress the test data volume and reduce the testing time. First technique uses a Broadcast decompressor and second technique uses an Embedded Deterministic Test (EDT) logic. The experimental results show that how scan compression is effective than the traditional full-scan. For the second technique, we compare the performance parameters of same design having different scan compression ratio. Here, we observed that the design having more compression ratio requires more test pattern to detect the fault. So, we can say that, there must be some optimum value of compression ratio for a particular design to take maximum advantages of scan compression.**

***Index Terms*— Linear feedback shift register (LFSR), Phase shifter, Embedded deterministic test (EDT), Test data volume, Test application time, compression ratio, ATPG.**

I. INTRODUCTION

In digital circuits, we know that any chip contains billions of transistors and this number is also growing continuously. Testing this much number of transistors in a reasonable amount of time is a tedious task. Digital circuits are facing various testability issues like test time, test data volume, test coverage, area overhead, etc. Design for testability (DFT) helps in making the internal flip-flop easily controllable and observable. By adding controllability and observability, we can make testing easier. Therefore, DFT is very important to detect manufacturing defects. For testing any chip, test costs have to be kept as low as possible.

The main concern of testing any chip is minimum Test time, Test data volume, Pin counts, and Power dissipation with high Fault coverage. As designs become larger, the number of scannable flops significantly increases, making design testability even more important to catch silicon manufacturing defects. If number of scannable flops increases in design, FULLSCAN test patterns are very costly to use and require more memory to store the test data on ATE (Automatic Test Equipment). It also takes longer time to test. So, we need to compress the test data used for testing and reduce the testing time. For this purpose, we use on chip

Grenze ID: 01.GIJET.8.2.529

hardware, that is known as Scan Compression. In Scan Compression, existing long-scan chains between scan input and scan output pins are divided into smaller number of scan channels and connected to the compression and decompression logic interface. Fig. 1 shows the basic Scan Compression architecture.

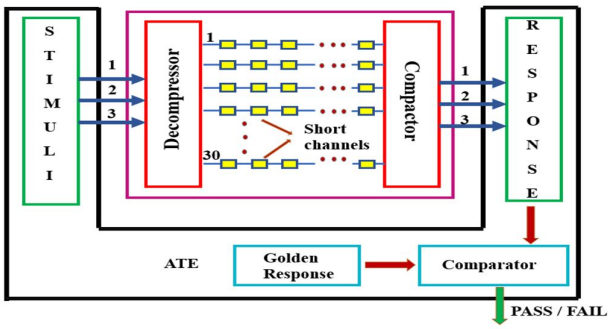

Fig. 1. Basic Scan Compression Architecture

Test data volume stored in ATE is known as test stimuli. In the decompressor, test stimuli coming from ATE is decompressed into large number of short scan channels and passes through each of the design core. Here, 3 scan-in channels coming from ATE are decompressed into 30 internal scan channels. Compressed test patterns are first decompressed into each core of design and then generated response from each of the core is compacted back. Compacted response is then compared with golden response coming from ATE. If there is any mismatch, chip is said to be faulty. One major issue is to handle with increased hardware area overhead due to the extra logic added.

At the compactor side, compactor compresses the test response back into 3 scan-out. finally, generated response is compared with the golden response coming from ATE. Pass or fail of the chip is decided by output of the comparator. In this paper, two types of decompressors are discussed and implemented.

1) Broadcast decompressor architecture
2) Ring-LFSR decompressor architecture

In the broadcast decompressor, the scan input pins directly load the data received from ATE onto the internal scan channels. That means simply broadcast the data. The number of internal scan channels are more than the number of scan input pins. So, the data is fanned out to the rest of the channels. This is also referred to as Illinois fan-out [6]. The number of unique values the channels receive is equal to the number of scan input pins [6].

Whereas in the second design, EDT (Embedded Deterministic Test) technology, extends ATPG (Automatic test Pattern Generation) with improved compression of scan test data and a reduction in test time [11]. EDT technology is based on traditional, deterministic ATPG [11]. It consists of Ring LFSR and phase shifter logic to decompress the test data. The compactor resides between the core scan chain outputs and the channel outputs connected to the tester. To compress the generated response EDT uses spatial compactors and gating logic. This technique is helpful to reduce the test data volume, test application time, area overhead as well as to improve the test coverage.

The paper is organized as follows. The literature review of existing scan compression techniques is discussed in Section 2. The architecture and methodology for implementing the two of the scan compression techniques is presented in Section 3. The experimental results are provided in Section 4, whereas conclusions are drawn in Section 5.

II. Literature Review

Quality of any VLSI device depends on Testing. There are many ways to achieve targeted quality but we also have to consider the cost as well. Costs include the cost of ATE (Automated Test Equipment), development CAD tools, test vector generation, test programming and the cost of extra hardware included [10]. Scan compression involves compressing the amount of test data that must be stored on ATE for testing. This is achieved by incorporating by on-chip hardware before the scan chains to decompress the test stimulus coming from the ATE. Compressor compresses the generated response before feeding to the ATE. Compression techniques introduce dependencies as many internal scan chains are fed from a few data bits of decompressor when target compression is increased [1]. This increased compression ratio reduces controllability and observability in the scan chains. This problem is attempted in [1] and New Scan Compression (NSC) Architecture

is proposed. This method includes a ranking of SFF's (Scan flip-flop) based on the specified values present in the test patterns. The SFFs having higher specified values are moved out of the compression architecture and placed outside in the scan chain. It decides the percentage of SFFs to be moved out of compression architecture and that is less than 0.5% of the total SFFs present in the design to achieve a better result. X-filling technique proposed in [2] replaces don't care bits and the filled test set with specified bits. This work is further encoded by Huffman encoding technique to give effective results compared to the other data compression techniques. This technique gives minimal time and memory requirement. Similarly, Run-Length encoded method combined with the compatible XOR decoder circuit is proposed in [3].
This technique is used to achieve higher compression ratio as well as reduce the test data, test power and test application time simultaneously with acceptable area overhead. To improve the diagnostic resolution of MISR (Multiple Input Signature Register), signatures are compared after regular intervals of time [5]. This architecture is enhanced by adding reset logic to improve the diagnosis further. It also improves the immunity against X-sources and also detect the fault early. To handle the issues related with power requirement during shifting of bits, Shift power group (SPG) architecture was proposed [6].

III. Design and Implementation

Scan compression techniques using broadcast and Embedded deterministic test (EDT) logic is discussed and implemented in this paper. Also, a comparison of different performance parameters of scan compression with respect to two different scan compression ratios are discussed. Using scan compression technique we reduced the test data volume, test time and increase the test coverage. By performing timing analysis, we also reduced the test area overhead. The major contributions of this work are presented as follows:
1. Implementation of scan compression using broadcast decompressor architecture and comparison of results with traditional Full-scan.
2. Implementation of the scan compression using EDT logic with compression ratio 60 and 30. Comparison of the performance parameters with respect to compression ratio.
3. A significant amount of reduction in chip area overhead.
4. Test coverage improvement.

A. Broadcast decompressor architecture

Table I shows the design specifications of scan compression using broadcast decompressor.

Table I. Design Specifications

Reset	2 (Functional reset and TP1500 rest)
Scan-in ports	8
Scan-out ports	8
Max. Chain length	100
Compressed chain count	43
Uncompressed chains	8
Extest chains	8
Compression Ratio	5.375

Fig. 2 shows the broadcast decompressor architecture. In the simulation of this design, we have used synopsy's Testmax and Tetramax tools. Scan Compression is implemented to understand how scan compression is beneficial than traditional scan. In design, it has 8 scan-in and scan-out. After performing scan compression, we decompress 8 scan chains into 43 internal scan channels using broadcast decompressor.
Fig. 3 shows the overall architecture of scan compressor for the design. On-Chip Clocking (OCC) is used to control the clock operations in scan mode. In stuck-at testing, it ensures only one clock pulse is generates in capture phase. Wrapper boundary register (WBR) provides a core isolation mechanism for modes like INTEST or EXTEST. It also provides full controllability and observability to all the core in the design. INTEST mode is used for testing the core's internal logic while EXTEST mode test the interconnect wires between core. So, in INTEST mode, WBR cells at input side act as primary inputs to the CUT (Circuit Under Test), while WBR cells at the output side act as primary outputs. In EXTEST mode output side WBR cells provide patterns and the WBR cells at the input side capture responses from the interconnect.

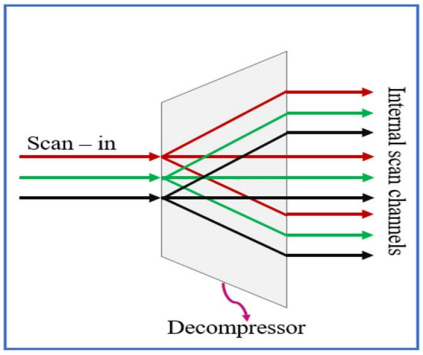

Fig. 2. Broadcast Decompressor Architecture.

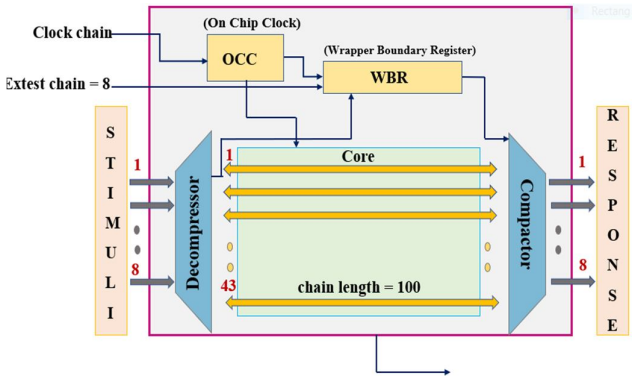

Fig. 3. Scan compression architecture using broadcast decompressor.

B. Ring – LFSR decompressor architecture (XOR decompressor)

Fig. 4 shows the decompression logic of Ring-LFSR (Linear Feedback Shift register) decompressor used in EDT. Scan inputs are given to the input of Ring-LFSR. In RING-LFSR; when clock is pulse, signal moves from one flip-flop to next. Some outputs are combined in exclusive -OR configuration to form a feedback mechanism. It is used for generating input test vector. Output of RING-LFSR is given as input to the phase shifter. It shifts the bit streams to create randomness in bit stream to increase the fault coverage. It consists of XOR network. Fig.5. shows the Scan compression architecture of Embedded deterministic test (EDT). Here, only one scan-in is given to the Ring-LFSR. It generates 60 EDT channels (internal scan channel) from one input. That means compression ratio is 60. Similarly, in next phase, we generate 30 EDT channel from one scan-in. So, here two designs with scan compression ratio 60 and 30 are proposed. To implement this design, we used Mentor graphics tools. Tessent TestKompress is used to generate the EDT channels.

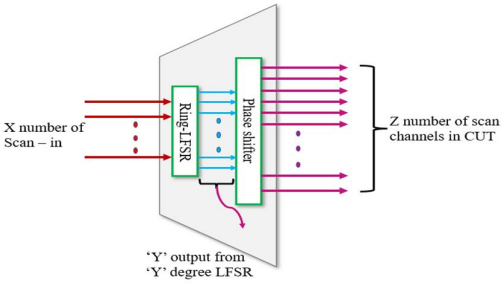

Fig. 4. Ring - LFSR decompressor architecture.

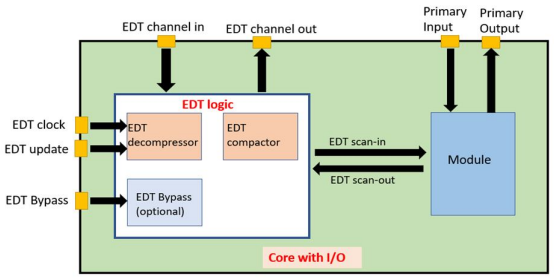

Fig. 5. Scan Compression Architecture using EDT logic.

Fig. 6 shows the LFSR architecture with one external scan chain. In the first clock cycle, values of S1, S4 and S7 is loaded serially into scan chain and then in the next clock cycle, values are shifted right. This continues for 3 clock cycles till all the values are loaded at its required position. And similarly, other scan chains are loaded.

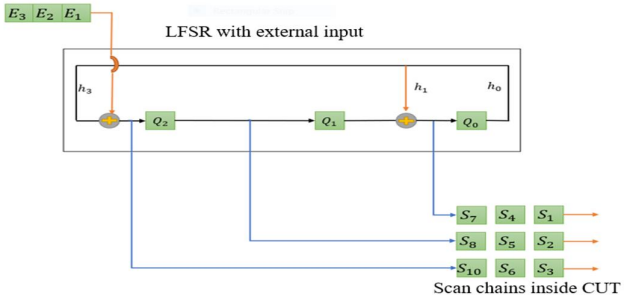

Fig. 6. LFSR architecture used in EDT

IV. Results and Discussion

Simulation results for broadcast compression technique is shown in Table II. It is compared with the simulation results of full-scan. It can be seen that test data volume as well as test time is significantly reduced in case of broadcast compression technique.

TABLE II. FULLSCAN AND SCAN COMPRESSION COMPARISION

Performance Parameters	Full-scan	Broadcast Decompressor
Scan chain length	538	100
Test data volume	688000	12800
Test time	4304	800
Scan channels	8	43
Compression ratio	-	5.375

A. Ring - LFSR Decompressor

We simulated this architecture for two different compression ratios. It is shown that the test coverage improves and area overhead reduces.

Performance parameters comparison

The comparative study of simulation results for two different compression ratios (1:60 and 1:30) is shown in Table III.

TABLE III. COMPARISION OF DIFFERENT SCAN COMPRESSION RATIO

Parameters	60 internal scans chains	30 internal scans chains
Types of faults	Stuck-at	Stuck-at
Clocking	Edge-sensitive	Edge-sensitive
Total faults	72310	72308
Test Pattern	1460	1243
Maximum scan chain length	47	49
Test coverage	97.10%	97.10%
ATPG effectiveness	99.99%	100%
Time (Sec)	35.8	26.1
Shift cycle	89	87
Scan cells	1525	1465

It can be observed that the number of required test patterns for almost same number of faults is more in case of compression ratio of 1:60. It results into reduction of effective compression which is obtained in case of 1:60 compression ratio compared to 1:30. It can also be seen from Table III that the test time is significantly less in case of 1:30 scan compression ratio.

On the basis of above results, it can be concluded that with increase in scan compression ratio; it is not necessary that the performance will improve. There will be some optimum value of scan compression ratio after which there may not be any further advantage. On the contrary, performance may degrade.

Area and Coverage Improvement

Fig. 7 shows the EDT logic inserted for the purpose of scan compression. All EDT channels are connected to the core via chain hooks.

It is nothing but flops required to meet the timing condition in design. By doing timing analysis on the design, it is observed that there is no need of chain hooks because, it has enough timing criteria for bit to pass on to the EDT channels. As well as, it does not impact any compression parameter. So, by removing those flops, we can reduce the area overhead on chip. By doing further analysis on design, it is observed that XOR network at the observation points helps to improve the test coverage.

Table IV, shows significant improvement observed in area overhead and test coverage. There is 0.33 % improvement in test coverage whereas 2.38 % improvement in area overhead.

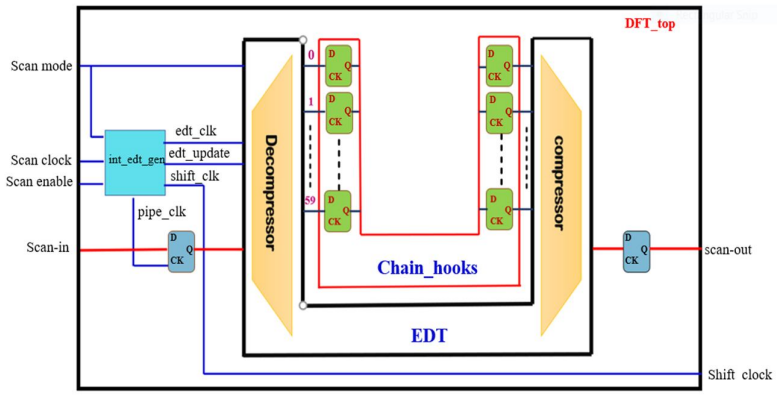

Fig. 7. Chain hooks in EDT

TABLE IV. IMPROVEMENT IN COVERAGE AND AREA OVER HEAD

Parameters	Before	After	Improvement
coverage %	99.45	99.78	0.33
Area (micron)	176741.036	173889.264	2851.264

V. CONCLUSION

In this paper, we implemented two different scan compression techniques. In the first technique, we used broadcast scan compression architecture and compared results with traditional full-scan. Result shows that using scan compression, we can reduce the test data volume and test time by 5X, compares to normal full-scan. Secondly, we implemented scan compression using EDT logic. By comparing the same design specifications for different scan compression ratios; it is observed that there must be some optimum value of compression ratio. Beyond which the test data volume and the test time increases instead of performance improvement. We also observed the improvement in test coverage and reduction in area overhead from the timing analysis.

REFERENCES

[1] Shantagiri, Pralhadrao V., Rohit Kapur, and Chandrasekar Shastry. "New scan compression approach to reduce the test data volume," IET Computers & Digital Techniques (2021): 251-262.
[2] Sivanandam, Lokesh, Sakthivel Periyasamy, and Uma Maheswari Oorkavalan. "Power transition X filling based selective Huffman encoding technique for test-data compression and Scan Power Reduction for SOCs," Microprocessors and Microsystems 72 (2020): 102937.
[3] Yuan, Haiying, et al. "An Efficiency Partially Compatible Test Decompression Technology Oriented RL-HC," 2021 IEEE 5th Advanced Information Technology, Electronic and Automation Control Conference (IAEAC). Vol. 5. IEEE, 2021.
[4] Shenoy, Jaidev, et al. "On-chip misr compaction technique to reduce diagnostic effort and test time," 2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID). IEEE, 2019.
[5] Solanki, Priyanka N., Nilesh Ranpura, and Yogesh D. Parmar. "DFT Methodologies for Reducing Shift Power of Compression Architecture for 28NM ASIC," 2018 2nd International Conference on Trends in Electronics and Informatics (ICOEI). IEEE, 2018.
[6] Nagaraj, Pradeep, and Senior Principal Product Engineer. "Choosing the right scan compression architecture for your design," Cadence Design Syst (2015).
[7] Sakrappanavar, Praveen, Siva Yellampalli, and Ashish Kothari. "Comparative analysis of scan compression techniques," 2014 International Conference on Electronics, Communication and Computational Engineering (ICECCE). IEEE, 2014.
[8] Rajski, Janusz, et al. "Embedded deterministic test," IEEE transactions on computer-aided design of integrated circuits and systems 23.5 (2004): 776-792.
[9] Chakravarthi, Veena S. A practical approach to VLSI system on chip (SoC) design. Springer International Publishing, 2020.
[10] Wang, Laung-Terng, Cheng-Wen Wu, and Xiaoqing Wen. VLSI test principles and architectures: design for testability. Elsevier, 2006.