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An Analysis in to CMOS 1-Trit Ternary Full-Adder Technology

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***Abstract*—The paper presents an overview of work done in VLSI CMOS (complementary metal oxide semiconductor) during the previous two decades on several types of adders, including ternary adders and others. The adders and designers devised effective methods for presenting their ideas. To provide context for the study, a variety of articles are reviewed and analysed. With the growing demand for battery operated, mobile, efficient systems, application-based processing is becoming more common as opposed to old-school technology-based gadgets. The biggest problem when dealing with high-speed functioning devices is power waste. As device transistor sizes shrink, we face the challenge of increasing the density of a single integrated circuit. Due to increased manufacturing complexity as well as other concerns such as capacitance and scaling constraints, high connection complexity makes VLSI/ ULSI extremely challenging. When compared to binary adders, ternary adders function efficient better in terms of information transmission. The quaternary data transmission rate is much higher than the binary and ternary data transmission rates.**

I. INTRODUCTION

A. Complementary Metal Oxide Semiconductor

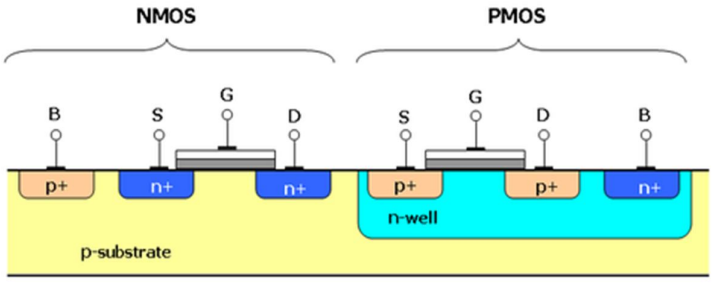

Figure 1 CMOS

In CMOS , P-type and N-type transistors are cast-off to design logic functions. It use in making integrated circuits chips and use in various digital devices and analog devices.[1]CMOS has the advantages that it does minimum power dissipation and gives an edge over better performance.[2] It uses both N and P type logic functions, which gets ON in one state and OFF on the otherwise.

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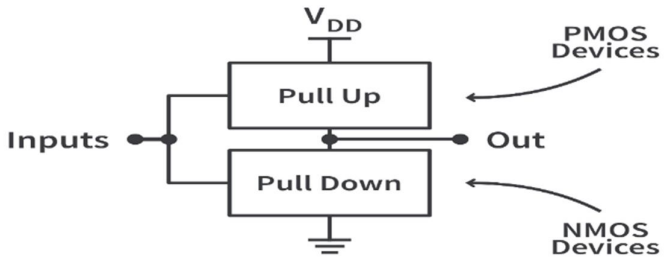


Figure 2 CMOS gate logic

The power consumption of CMOS circuits is a significant concern. They have a significant technological issue. As technology advances, numerous important difficulties arise, such as transistor oxide thickness, lower voltage, and increased transistor density, all of which increase the chip's power consumption. A family of circuit types for low-power design focuses on controlling transistors between pull-up and pull-down circuits, as well as between pull-up circuits/pull-down circuits. In addition, overhead latency and power consumption have increased. [3]Advantage of using it that it enhances the performance by increasing the speed and low power wastage and high noise margins.

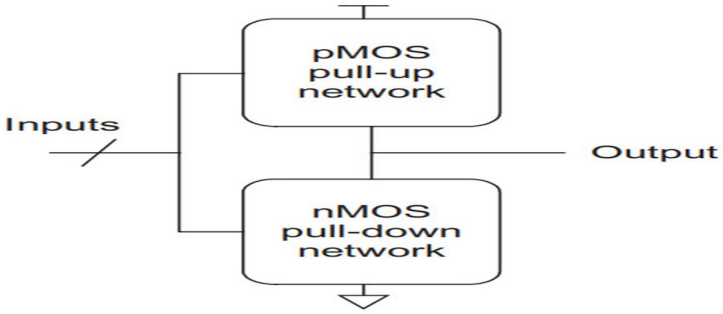
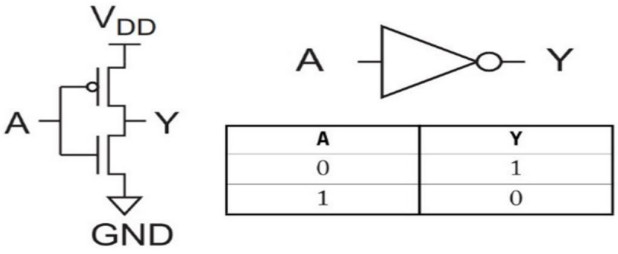


Figure 3 Inverter

Inverters can be design using CMOS0. It's also called NOT gate. It gives logic low when the input is high and low otherwise.



A	Y
0	1
1	0

Figure 4 CMOS Inverter

A. Adder

There are different adders on which throughout the last two decades different work has been proposed. Different technologies has been proposed and depending upon the number is the number of input given to the adders. The performance of adder Depends upon the operation and the technology they are designed in. Different researchers are carried out to reduce the propagation delay and increasing the optimization.[1]

B. Ternary adders

The following table shows the truth table of a ternary half adder circuit. A and B are two inputs that can have one of three values: 0, 1, or 2. There will be three tiers in the output as well. The projected outcome of the nine pairings is displayed.

C. Ternary full adder

The following table shows the expected output table of a ternary full adder circuit. Two inputs with three possible values: 0, 1, and 2. There will be three different scenarios of output in the incident.

II. BACKGROUND WORK

A. Ternary gate and Logic Circuits

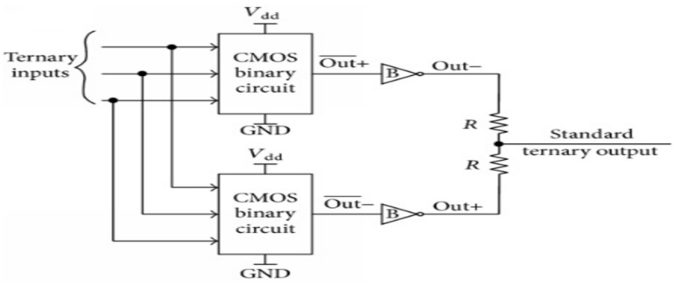


Figure 5 Ternary logic

Since the early 1980s, ternary sensing has been used in VLSI employing MOSFETs [5]. In the field of digital systems, ternary sense gives several an advantage over double sense. In VLSI implementation, MOS technology has a graphical operation. Half adders, complete adders, as well as various types of perpetration such as shift registers and multipliers, can be built (5). Ternary sense circuits offer benefits over double sense circuits in that they take up less space and have simpler interconnects. When a circuit is implemented in CMOS, it has fewer gates than when implemented in ternary mode, resulting in 1) reduced area usage 2) Propagation detention was abolished. 3) more noise tolerance (6). The arduous task of implementing ternary logics was made easier by using MOS transistors. However, CNFETs have recently been used to implement ternary logics (carbon nanotube filed-effect transistor). Ternary logics have been proven to be more efficient in conveying information than binary logic circuits, and they have also been found to be useful in lowering chip size. Because the estimated connectivity cost is lower, it receives greater attenuation. When compared to their ternary counterparts, binary circuits are more expensive. Ternary logics, which are used as ternary arithmetic units in microprocessors, communication, and digital signal processing systems, aid in the improvement of complicated circuits, which in turn aids in the improvement of the overall ternary system's efficiency.

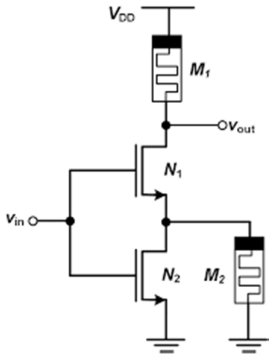


Figure 6 Inverter design using ternary logic

Digital signal processing applications can be benefitted from ternary logic. In 2018 [7], Ternary logic is made with the idea of having 2:1 multiplexers which showed great reduction in power consumption.

B. The reversible ternary full-adder

The main factor while designing a VLSI circuit is considering the amount of power utilization by the circuit and all the energy costs in it. Landauer used thermodynamic technology to show that the use of classical logic, sometimes known as irreversible logic, in the design of digital circuits results in an unintentional waste of

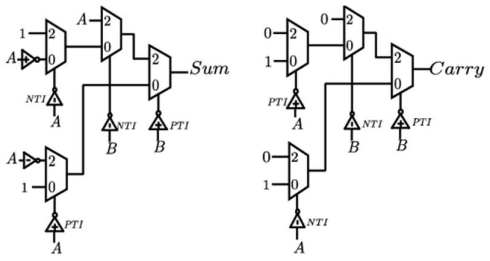


Fig 7 Half adder using 2X1 mux

electrical energy[8]. Circuit design has a significant difficulty in terms of high power consumption and energy losses. Even the tiniest accumulation of energy can reduce the circuit's life expectancy[8]. In comparison to standard computational circuits, Bennet demonstrated that reversible procedures aid to reduce energy losses. Reversible logic gates reduce energy losses while consuming no additional power. The gate is reversible if the number of inputs equals the number of outputs and there is a one-to-one connection between them, meaning that the input vector can be attained by the output vector.

C. Quaternary Logic Circuits

All industrial applications has been utilizing binary logics for a very long .Binary stands for two which means it utilize two states which are 0's and 1's to symbolize each state. As the binary logic utilizes two states, so to represent a number it utilized more bits. More power is required and it uses more area for its designing.

Therefore ternary logic is introduced . We discover that, as compared to binary logics, ternary logic needs less bits to represent, resulting in a smaller footprint. We can also reduce power usage by lowering the number of transistors. Ternary logics use three states to represent themselves. The quaternary system uses four states: 0,1,2,3, and 4. Quaternary logic helps to increase power by reducing the number of bits used. The comparison of the ternary and quaternary full adders reveals that the ternary full adder requires more area and power to complete the design, but the quaternary full adder requires less area and power[9].

D. Double Pass transistor logic circuits

Because of its greater logic capability, pass transistor logic has an advantage over CMOS logic. The propagation delay is an issue with series connections in pass transistors. For improving the performance of CMOS circuits, many pass transistor logic families have been present. Complementary pass transistor logic demonstrated exceptional speed when used as multiplier circuits in complete adders due to its reduced input capacitance and increased functionality. Essentially, double pass transistor logic is an improved version of complementary pass transistor logic that aids in the reduction of current power voltage designs. The performance perimeter of a circuit has been improved by using a double pass transistor.

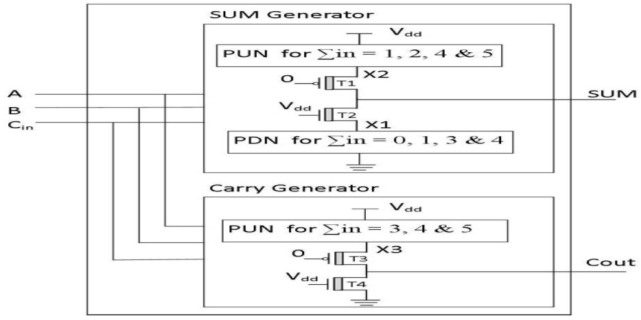


Figure 8 Carbon nanotube ternary field effective transistor based on TFA[10]

In [11], the idea is put forward to make ternary logic circuits using double pass transistor. Different gates have been proposed using it.

The idea proposed in [12],is that implementing the design circuits using has shown significant improvement in performance and decreased power consumption.

In the paper[14] proposed double pass transistor logic circuits is to use wave pipelining or time equalization. Double pass transistor based TXOR, TAND and TOR logic gates are design and are implemented in BISIM3

device model speed and power performance of the design of ternary logic are calculated and verified the result obtained is high in speed in ternary system model with lowered power in area.

E. Decoders

The idea is to implement ternary decoder in digital CMOS technology with the help of double pass transistor logic.[13] So, [14] put the idea to implement the decoder using ternary logic.

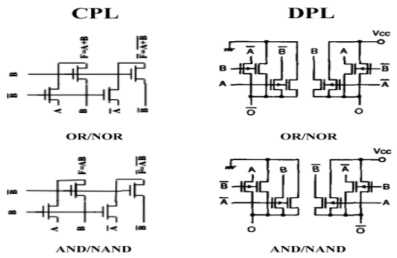


Figure 9 DPL gate design[14]

F. Full Adder

Adders are important in many applications as they can perform addition, subtraction ,multiplication other basic operations. The performance of adder Depends upon the operation and the technology they are designed in. Different researchers are carried out to reduce the propagation delay and increasing the optimization. In the year 2017,[15] Ternary full adder is put forward with the help of SET and MOS technology transistor. It was observed that Set showed a lead while saving the power use by the circuit. Full-adder (FA) are use as and elementary building block for most time-critical, high power consuming digital data-processing systems. Speed-power characteristic of FA is a concern in order to improve its system performance. The problem however becomes more when if ternary is in consideration to produce its inherent advantages in digital processing. These designs have issues on account of reliability, fabrication-complexity, yield and cost among others.

The following adders are simulated and analysed using CMOS, CPL, DPL.[16]. Many digital application use full adders as their most important arithmetic unit. To overcome the area and power wastefulness issues in MOSFET we implement it by means of carbon nanotube filed effect transistors(CNTFET) [16].Though the problem encountered with the using carbon nanotube field effective transistor is that it still requires a more number of transistors the main purpose of using ternary full adder is to minimize the power consumption of the circuit bio operating it both gradually and reversible in the given paper the full adder is proposed in 180nm CMOS technology.

Different types of adders are studied using CMOS technology, complementary pass transistor logic, and double pass transistor logic in the year 2017[17].

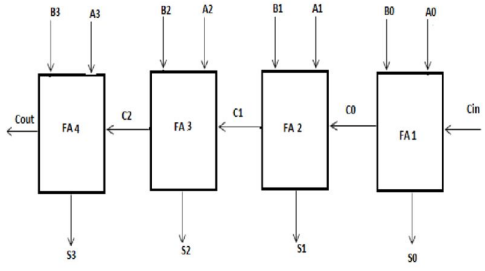


Figure 10 N-bit parallel adder[16]

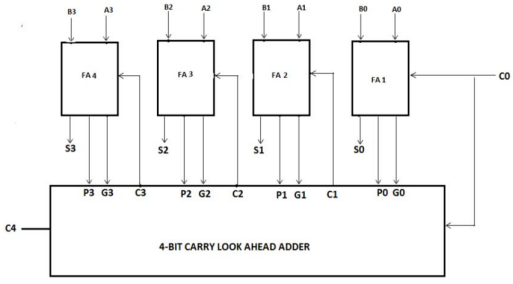


Figure 11 Carry look ahead adder[16]

Radix can be used to limit the complications put forward when multiple inputs are given to the logic circuits.[17] Radix 3 is the one we call ternary system. K-map based methods are to design the ideas forward. Cadence software is taken help of to prove the results. MOS neuron devices are used to implement the ternary inverter [18]. Duality and complementary ternary are used to make a dynamic DPL circuit. The gate in which fabricated using double poly layer. Different paper put up different idea to make TFA, and quantum computing is one of them [20]. Scaling down of transistor has its own challenges and FINFET has emerged out to be a way to deal

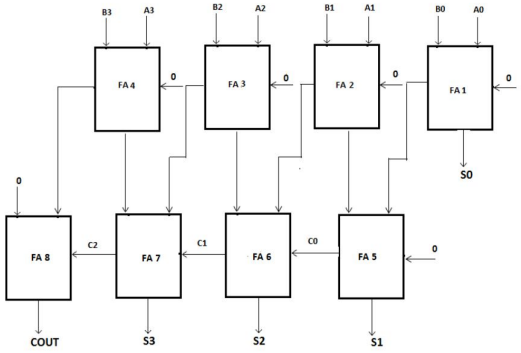


Figure 12 One level CSA[16]

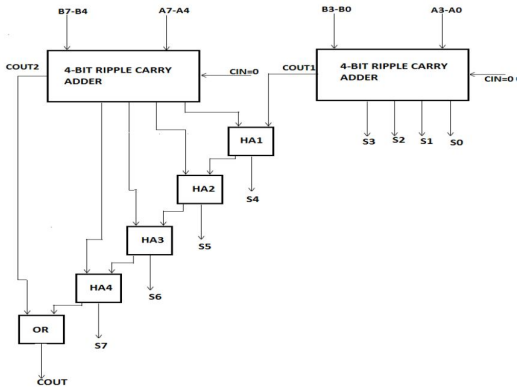


Figure 13 Increment adder using carry

with it. XOR or XNOR or their combinations are used to implement the TFA. The work proposed is in 45nm technology, using FINFET transistor has implemented the for the arithmetic logic designs. Inverter use both NMOS and PMOS transistor to component together the double gate pass transistor.

G. Hybrid full adder

Reduction in transistor size has emerged issues among VLSI circuits. To encounter such problems, engineers put forward the idea of hybrid CMOS[21]. CMOS scaling gives us an issue of sensitivity prone to radiation. Leakage in power with reducing the threshold voltage.[22].

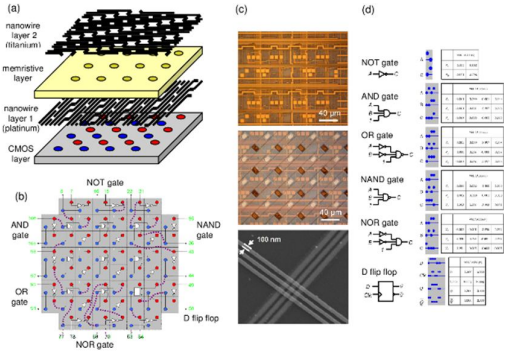


Figure 14 Hybrid CMOS circuit chip[21]

III. Conclusion and Future Scope

In this paper different Ternary Full-Adder (TFA) are compared and all the background work has been presented for high-speed, power efficient circuit. The circuit is designed with enhancement-type normal process MOS transistors, reducing manufacturing complexity. All input to output pathways were optimised and reported on for path delay equalisation. Adders are important in many applications as they can perform addition, subtraction ,multiplication other basic operations. The performance of adder depends upon the operation and the technology they are designed in. Different researchers are carried out to reduce the propagation delay and increasing the optimization. Ternary full adder is put forward with the help of SET and MOS technology transistor. It was observed that Set showed a lead while saving the power use by the circuit. Most time-critical, high-power-consuming digital data-processing systems employ full-adders (FA) as an essential building piece. In order to increase FA's system performance, its speed-power characteristic is a problem. However, when ternary is taken into account to create its inherent benefits in digital processing, the situation gets even worse. These designs have problems with dependability, fabrication complexity, yield, and cost, to name a few.

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