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A Miller Compensated Operational Amplifier with Improved Stability

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***Abstract*— Versatile and often used operational amplifier (op-amp) architecture, the two-stage op-amp is appropriate for a variety of analogue circuits and applications, including high-precision amplification and signal conditioning. It offers high gain, which is essential, good frequency response and stability, especially when used with cutting-edge hardware like Complementary Metal-Oxide Semiconductor (CMOS). For high-speed applications that require more bandwidth, this can be a drawback. The CMOS op-amp circuit may produce a consistent output dc offset voltage if improperly built. Modeling of transistors has become an important design procedure to obtain a better op-amp for greater performances. Here we proposed an op-amp compensated with miller capacitance to gain high parametric values such as Gain (AV), unity-gain frequency, Power dissipation, a supply voltage of 1.2V, Slew Rate (SR), Phase margin (PM). The op-amp is simulated using OrCAD Capture to obtain the improved stability and enhance the parameters. The proposed op-amp can be used in high-speed applications and signal conditioning.**

***Index Terms*— op-amp, stability, miller compensation, phase margin, unity-gain frequency, slew rate**

I. INTRODUCTION

An essential part of analogue integrated circuits is the operational amplifier (op-amp). Op-amps are widely used for different of tasks, including filtering, regulation, and the amplification of electrical impulses. When supply voltage and transistor channel widths fall, designing op-amps gets increasingly difficult. The traditional and widely used method for designing op-amps has been the two-stage op-amp structure. The two-stage op-amp can perform as well as systems using cascode stages for resistive loads. Modern technology has a channel length of 45 nm or less, making it challenging to increase the design performance of op-amps due to the inherent transistor performance constraints [1]. Irrespective of the intrinsic gain and supply voltage limitations in current CMOS technology, the two stage op-amp configuration can still provide a high gain and big output swing. The compensation problem is one of the major difficulties in operational amplifiers, one of the most popular analogue circuits.

In analogue circuits, accurate compensation involves modifying the dominant poles and zeroes to increase bandwidth, gain, and frequency response. High gain op-amps in the 22 nm Process can be produced by using current mirror structures with high output impedance [2]. Several compensation strategies based on traditional

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CMOS technology were given in several papers in the literature. This is a significant disadvantage of these compensation techniques since it necessitates a separate compensation circuit from the primary circuit. The amplifier's area and power consumption have significantly risen due to this new block. The key simulated parameters are Gain (AV), unity-gain frequency, Power dissipation, Slew Rate (SR), Phase margin (PM). The employment of two amplification stages results in a significant output signal swing and increased voltage gain in the second stage. The first stage provides strong voltage gain. Moreover, negative feedback frequency correction is used at each level to increase stability and bandwidth. Using two identical capacitors, Miller correction is applied around the second stage.

Stability should be taken into account while designing a circuit in order to guarantee that it will remain stable under the necessary operating circumstances. When the op-amp is designed with negative feedback, instability results, and under specific circumstances, the negative feedback turns positive. The output of the circuit then oscillates in the unstable scenario. Unconditionally or totally stable stability is stability under any input circumstance. A margin of stability, however, must be included if a system is not absolutely stable in order to guarantee steady functioning under the necessary operating conditions. The designer of the op-amp can intentionally limit the open-loop gain magnitude at higher signal frequencies by adding capacitance between specified nodes within the op-amp in order to achieve reliable closed-loop operation.

There are, however, a number of additional methods for op-amp compensation. When employing the single capacitor compensation method, adding a series resistor, a buffer, or a buffer and serial resistor can improve the op-amp performance. Although there are a number of Miller compensation procedures proposed in the literature [3], Ahuja [4], Ribner [5], and Nested Miller [6] are the most popular ones. This paper concentrates a Miller compensated op-amp that is enhanced in its stability and has improved phase margin and unity-gain bandwidth.

There are four more sections in this paper. The present approaches to compensation are covered in Section II, along with their design limits and other drawbacks. The proposed technique is qualitatively presented in Section III, and its relative advantages over the existing techniques are discussed in Section IV, which also includes implementation details for the two-stage op-amp using the proposed compensating technique. Section V brings the paper to a conclusion.

II. EXISTING METHODOLOGY

Miller op-amps in Class-AB are introduced that are small and power-efficient. The op-amp can drive a variety of resistive and capacitive loads with acceptable phase margin, significantly increased bandwidth, and high current efficiency by utilizing a telescopic input stage, traditional Miller compensation, and a straightforward auxiliary amplifier that consumes only modest additional power dissipation (15%). The device makes use of a basic auxiliary circuit to improve the gain-bandwidth product of the op-amp and aid in driving a variety of capacitive and resistive loads with good static and dynamic current efficiency. Stability under a variety of loading scenarios is achieved using basic Miller compensation.

NMOS and PMOS unit transistor sizes (W/L)N = 10 m/0.27 m and (W/L)P = 40 m/0.27 m, respectively, were used in the design of the proposed, conventional Class-A (Conv-A), and free-Class-AB op-amps shown in Figs. 1, 2, and 3. The same bias current IB = 15 A and supply voltage 1.2 V were used for each simulation.

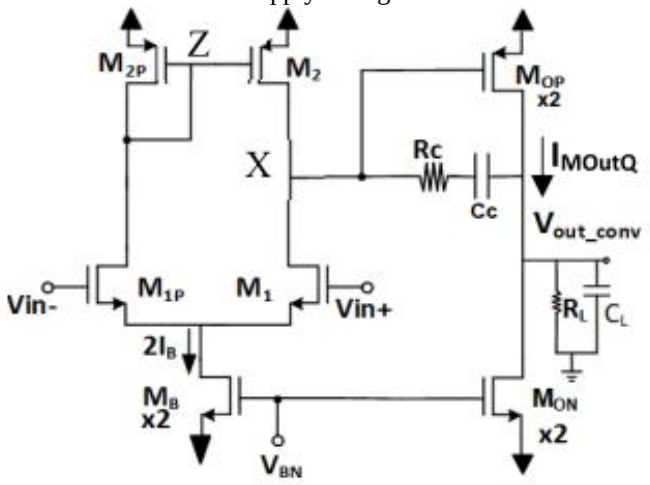


Figure 1 Conventional miller Class-A NMOS op-amp

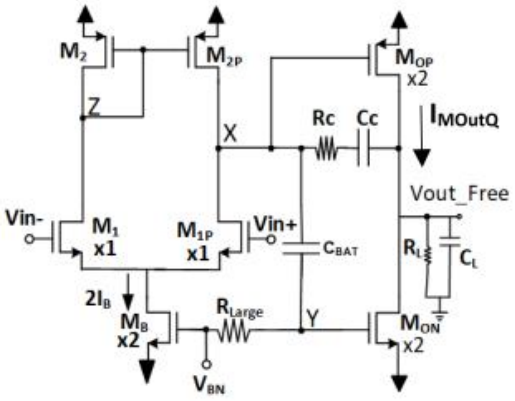


Figure 2 Free-Class-AB op-amp

Results from experiments and simulations attest to these qualities. The suggested op-amp is resistant to changes in supply, temperature, and process. The results of the op-amp simulation and testing are measured for strong inversion at 15µA of bias current and for sub-threshold at 250nA of bias current. Integration of additional circuit results in additional power dissipation and requires increased gain at the intermediate stage of the circuit to power the additional circuit.

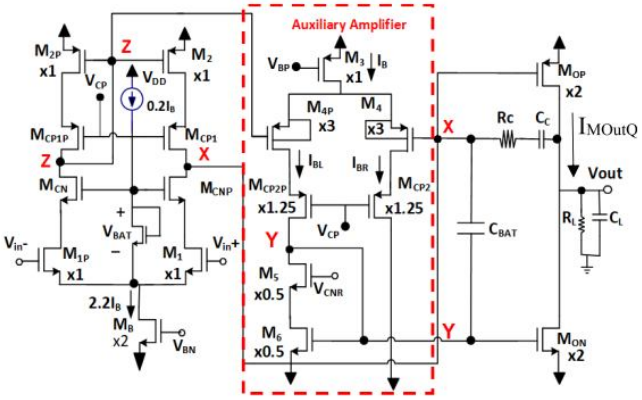


Figure 3 Op-amp of existing system

The simulation result of the existing op-amp is shown in Fig 4. The plot gives the transient analysis of the op-amp at CL=300pF in parallel with RL=250Ω for 100 KHz input pulse.

III. Proposed Op-Amp

To design a Miller compensated op-amp that is enhanced in its stability and has improved phase margin and unity-gain bandwidth. A two-stage miller compensated op-amp is designed using 0.13µm CMOS technology. The propose op-amp is shown in Fig 5. The op-amp is designed with a differential stage input and the second stage of the circuit is common source amplifier. A current mirror is given to have a constant bias current in input stage transistors. Sizing transistors carefully can help to increase the op-gain, amp's bandwidth, and power consumption. The width of the transistors is designed to fix 20µm for NMOS and 40µm for PMOS. The common-mode rejection ratio (CMRR) and the input impedance can be enhanced, in particular, by matching the transistors in the input differential pair and the current mirror. The method can greatly enhance the performance of the two-stage op-amp with Miller compensation, producing an op-amp with increased gain, bandwidth, and stability. The performance of the op-amp can be adjusted to ensure that it fulfils design requirements via a thorough simulation procedure.
The UGB is calculated using the expression given below.

$$\text{unity-gain bandwidth} = gm1/Cc \quad (1)$$

The slew rate is given by the following expression

$$SR = I/Cc \quad (2)$$

The common source stage is used to enhance the output swing of the first stage of op-amp as well as the gain of the amplifier which is shown in Fig 5. The phase margin for the amplifier is obtained at 60 degree in the plot during simulation.

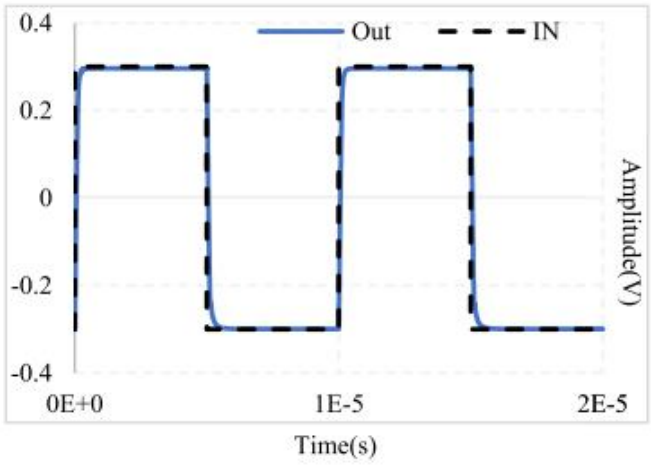


Figure 4 The transient analysis of the existing op-amp at CL=300pF in parallel with RL=250Ω for 100 KHz input pulse.

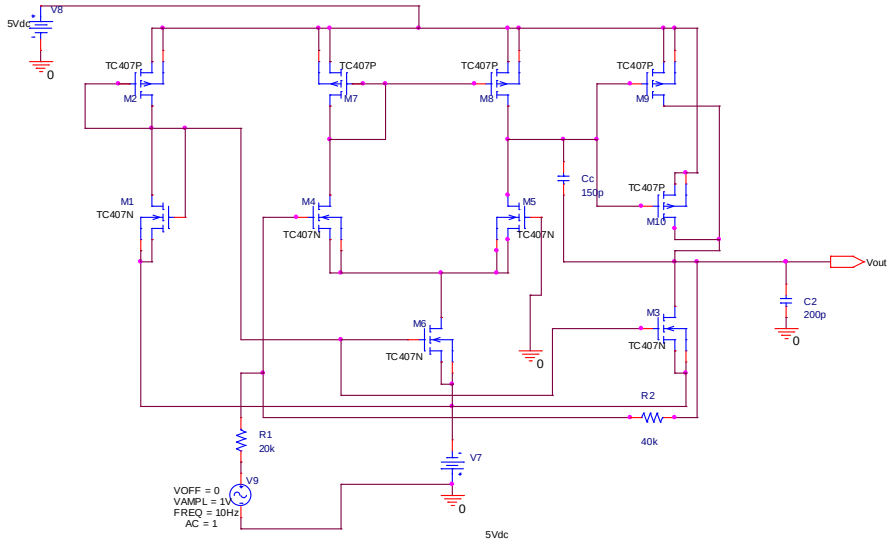


Figure 5 The proposed two stage op-amp

A. Design Parameters

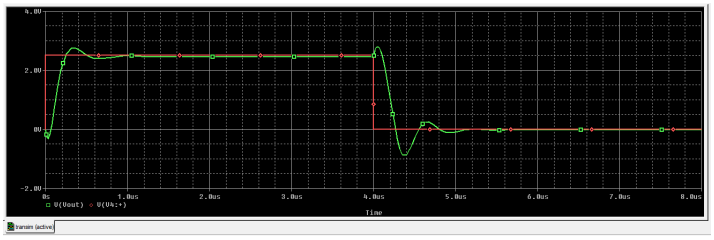
The following are the design parameters for the proposed op-amp.

TABLE I. DESIGN PARAMETERS

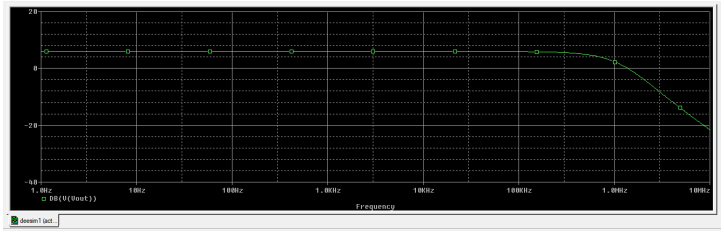
PARAMETERS	VALUE
Technology	0.13 µm
C_C (pF)	150
C_L (pF)	200
Power(µW)	140
Phase margin (deg)	>=60
Vss (V)	1.2

IV. Simulation Results

The op-amp was designed and simulated using Cadence OrCAD and Transient, DC sweep, AC analysis and Power Supply Rejection Ratio (PSRR) analysis were perfomed. The plots obtained are shown in Fig 6. The proposed op-amp was designed using CMOS 0.13 µm technology, with NMOS and PMOS unit transistor sizes of (W/L)N = 10 m/0.27 m and (W/L)P = 40 m/0.27 m, respectively. The bias current IB = 15µA and supply voltage 1.2 V were used to simulate it.



(a)



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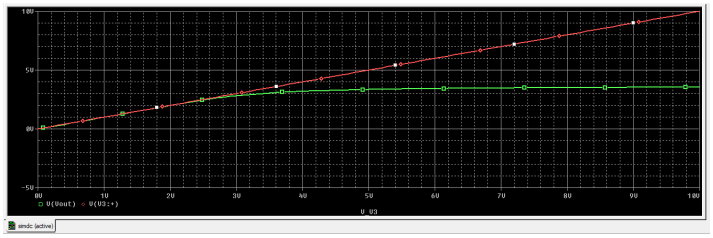

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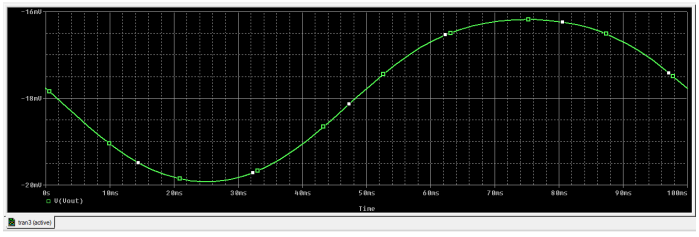

(d)

Figure 6 (a) Transient analysis at supply voltage 1.2V
(b) AC analysis of op-amp at 60(deg) to determine PM
(c) DC sweep at input stage to obtain power dissipation
(d) PSRR at 10 Hz freq.

The open loop gain responses are obtained from the AC analysis and the phase margin is obtained at 60° and the output obtained was 1.31 M. The DC gain from the AC analysis is 88.9 dB when the toggle cursor was placed at 3 dB of the plot. The slew rate for the proposed op-amp was 0.31 V/µs and was obtained from transient analysis of the op-amp. It can be observed that the proposed op-amp still offers a sizeable DC open-loop gain and a slightly high phase margin. Getting a greater UGB for the same phase margin as opposed to a better phase margin for the same UGB is another way to employ the suggested technique. Lowering the compensating capacitor CC will result in a greater UGB due to the 4.5-fold rise in gm2, but this won't improve the phase margin (PM). Table 2 gives the

parameters of the op-amp that is being compared to the existing system. The PSRR response is obtained to visualize the phase shift of op-amp at the inverting side of and the gain is obtained.

TABLE II PERFORMANCE

PARAMETERS	EXISTING SYSTEM	PROPOSED SYSTEM
Technology	0.13µm	0.13µm
Load Capacitance (C_L)	300 pF	200 pF
Slew Rate (V/µs)	5.4	0.31
Gain (dB)	88	88.9
Phase Margin (degree)	54	60
PSRR (dB)	86	76.3
Power (µW)	126	96
CMRR (dB)	93	80.895

V. CONCLUSION

A Miller compensated simple differential input stage op-amp is designed and simulated using Cadence OrCAD and the transient analysis, DC sweep and AC analysis were conducted to ensure the operation of the proposed op-amp. The gain of the proposed op-amp is increased by 0.9dB and the phase margin is obtained at 60° which is enhanced from the existing system. The slew rate is decreased to 0.31 V/µs which is to be improved in future scope. The power dissipation is 27.02% less when compared to the existing system. The stability analysis was performed and found that the stability is less when compared to the auxiliary amplifier integrated in the existing system.

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