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Design and Implementation of 16 Bit Manchester Carry Chain Adder with Domino Logic using Finfet Technology

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***Abstract*— The design and implementation of a 16-bit Manchester carry chain adder (MCCA) with domino logic using FinFET technology are presented in this paper, focusing on both 8-bit and 16-bit configurations. The Manchester Carry Chain Adder, known for its efficient carry propagation, is a crucial component in modern processors' arithmetic units. We conduct extensive simulations to compare the performance metrics of 8-bit and 16-bit MCCA designs implemented with FinFET technology. The evaluation includes key parameters such as power consumption, delay, and area utilization. Additionally, we explore the effects of varying operating conditions and supply voltages on the performance of these designs.**

***Index Terms*— MCCA; domino logic; finfet; cadence virtuoso**

I. INTRODUCTION

In recent years, the semiconductor industry has witnessed significant advancements in transistor technology, particularly with the emergence of FinFET technology. FinFETs offer improved performance characteristics such as higher drive currents, reduced leakage currents, and enhanced scalability compared to traditional CMOS transistors. Leveraging these advantages, researchers and designers are exploring the integration of FinFET technology into various circuit designs to achieve higher performance and energy efficiency. In this context, this study focuses on conducting a design and implementation of 8-bit and 16-bit Manchester Carry Chain Adders using Finfet technology. The choice of bit-width configurations, 8-bit, and 16-bit, is based on their relevance in modern computing systems, spanning from embedded applications to high-performance computing platforms.
The main goal of this study is to assess and contrast how well 8-bit and 16-bit Manchester Carry Chain Adder (MCCA) designs perform when using FinFET technology. Key parameters such as power consumption, delay, and area utilization will be analyzed to assess the efficiency and scalability of each design. Additionally, the impact of varying operating conditions and supply voltages on the performance of these adders will be investigated to provide comprehensive insights into their behavior under different scenarios. By conducting this comparative analysis, we aim to provide valuable guidance for designers and researchers in optimizing the design of arithmetic units for contemporary computing systems. Furthermore, this research contributes to advancing the understanding of the benefits and trade-offs associated with utilizing FinFET technology in adder designs of varying bit-width

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configurations. The discoveries from this research will lead to the creation of better and faster arithmetic units facilitating the continued evolution of computing technology.

TABLE 1: CHARACTERISTICS TABLE

CIN	Y	X	SUM	Cout	Carry status
0	0	0	0	0	Delete
1	0	0	1	0	Delete
0	0	1	1	0	Propagate
1	0	1	0	1	Propagate
1	1	0	0	1	Propagate
0	1	0	1	0	Propagate
0	1	1	0	1	Generate
1	1	1	1	1	Generate

II. FUNDAMENTAL DESIGN ASPECTS OF FINFET

FinFETs, represent a groundbreaking evolution in semiconductor technology, introducing a three-dimensional architecture that fundamentally differs from traditional planar transistors. In FinFETs, the conducting channel is formed by a raised fin structure, allowing for improved electrostatic control and mitigating short-channel effects. This three-dimensional design enables FinFETs to maintain superior performance characteristics even as transistor dimensions shrink to nanoscale levels. The FinFET's unique structure also facilitates better gate control, as the gate wraps around the fin on three sides, enhancing electrostatic integrity and reducing leakage currents compared to planar transistors.

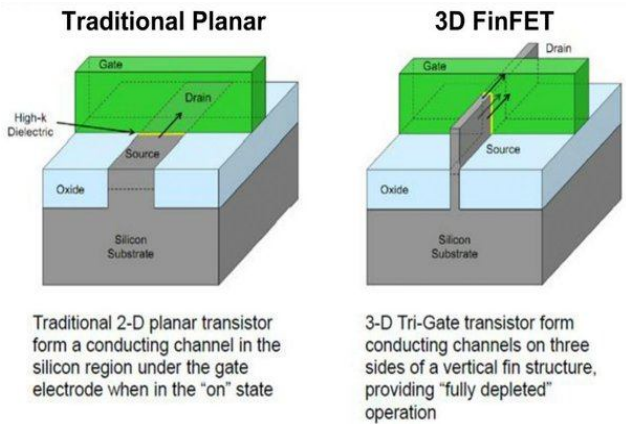


Fig. 1. Difference Between 2-D planar and 3-D Finfet

Gate All Around (GAA) architecture is a hallmark feature of FinFETs, contributing significantly to their superior performance. In this design, the gate surrounds the fin structure on all sides, providing enhanced control over the channel and minimizing undesirable leakage currents. The GAA architecture enables FinFETs to achieve steeper subthreshold slopes and improved subthreshold behavior, resulting in lower power consumption and improved transistor performance. By effectively surrounding the channel with the gate, FinFETs can achieve better gate control and electrostatic integrity compared to planar transistors, leading to higher drive currents and faster switching speeds. Furthermore, strain engineering and dielectric stack engineering are crucial aspects of FinFET design that further optimize transistor performance. Strain engineering techniques involve introducing mechanical strain into the semiconductor material, which can enhance carrier mobility and increase drive currents in FinFETs. By carefully tailoring the strain profile of the transistor, designers can fine-tune its performance characteristics and improve overall device efficiency. Additionally, dielectric stack engineering focuses on optimizing the insulating layers surrounding the fin to minimize parasitic capacitance and improve transistor speed and efficiency.

III. PROPOSED ADDER DESIGNS

A. 16-bit manchester carry chain (mcc) adder

The 16-bit manchester carry chain (mcc) adder optimizes circuit delay and boosts operational speed. By using the 16- bit mcc adder as a foundational component designers have the flexibility to develop highly efficient and rapid adder implementations, moving away from the traditional 8-bit MCC adder. The 16-bit MCC Adder features two sets of 16-bit inputs: P15 through P0 and G15 through G0, with circuit operation controlled by a clock signal. Input values originate from carry generation (Gi) and carry propagation (Pi) signals. Upon the CLK signal assuming a logic 0 or Low state, the circuit enters a precharge mode, ensuring that all outputs remain at logic 0. As the signal shifts from 'Low' to 'High', the output values adjust accordingly to mimic the inputs. Signals from Gi and Pi move through the circuit, resulting in carry outputs labeled C15 through C0.
The 16-bit MCC Adder operates similarly to the 8-bit MCC Adder, with inputs Pi and Gi processed at each stage.

$$Pr_{15}=X_{15} \oplus Y_{15} \quad Gr15=X_{15}.Y_{15}$$

$$Pr_{14}=X_{14} \oplus Y_{14} \quad Gr_{14}=X_{14}.Y_{14}$$

$$Pr_{13}=X_{13} \oplus Y_{13} \quad Gr_{13}=X_{13}.Y_{13}$$

$$Pr_{12}=X_{12} \oplus Y_{12} \quad Gr_{12}=X_{12}.Y_{12}$$

$$Pr_{11}=X_{11} \oplus Y_{11} \quad Gr_{11}=X_{11}.Y_{11}$$

$$Pr_{10}=X_{10} \oplus Y_{10} \quad Gr_{10}=X_{10}.Y_{10}$$

$$Pr_{9}=X_{9} \oplus Y_{9} \quad Gr_{9}=X_{9}.Y_{9}$$

$$Pr_{8}=X_{8} \oplus Y_{8} \quad Gr_{8}=X_{8}.Y_{8}$$

$$Pr_{7}=X_{7} \oplus Y_{7} \quad Gr_{7}=X_{7}.Y_{7}$$

$$Pr_{6}=X_{6} \oplus Y_{6} \quad Gr_{6}=X_{6}.Y_{6}$$

$$Pr_{5}=A_{5} \oplus B_{5} \quad Gr_{5}=A_{5}.B_{5}$$

$$Pr_{4}=X_{4} \oplus Y_{4} \quad Gr_{4}=X_{4}.Y_{4}$$

$$Pr_{3}=X_{3} \oplus Y_{3} \quad Gr_{3}=X_{3}.Y_{3}$$

$$Pr_{2}=X_{2} \oplus Y_{2} \quad Gr_{2}=X_{2}.Y_{2}$$

$$Pr_{1}=X_{1} \oplus Y_{1} \quad Gr_{1}=X_{1}.Y_{1}$$

$$Pr_{0}=X_{0} \oplus Y_{0} \quad Gr_{0}=X_{0}.Y_{0}$$

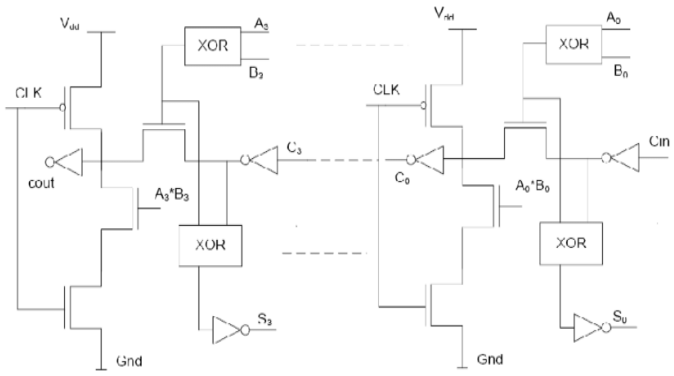


Fig. 2. 4-Bit mcc adder without keeper circuit using high speed domino logic

B. 8-bit mcc adder

The system consist of two sets of 8-bit inputs: G7 through G0 for the carry generate signals and P7 through P0 for the carry propagating signals. At each and every stage, these inputs are based on the outputs of carry propagation

and carry generation signals. The circuit's functionality is controlled by a clock signal. While the clock signal is at a Low state or logic 0, the circuit stays in a precharge mode, with all outputs set at logic '0'. Once the clock signal switches from logic 0 to logic 1, the output is determined by the input conditions. The carry propagation and carry generation inputs shift from the initial stage to the final stage, producing corresponding carry outputs: C7 to C0.

$$Pr_7=X_7 \oplus Y_7 \quad Gr_7=X_7.Y_7$$

$$Pr_6=X_6 \oplus Y_6 \quad Gr_6=X_6.Y_6$$

$$Pr_5=X_5 \oplus Y_5 \quad Gr_5=X_5.Y_5$$

$$Pr_4=X_4 \oplus Y_4 \quad Gr_4=X_4.Y_4$$

$$Pr_3=X_3 \oplus Y_3 \quad Gr_3=X_3.Y_3$$

$$Pr_2=X_2 \oplus Y_2 \quad Gr_2=X_2.Y_2$$

$$Pr_1=X_1 \oplus Y_1 \quad Gr_1=X_1.Y_1$$

$$Pr_0=X_0 \oplus Y_0 \quad Gr_0=X_0.Y_0$$

Pr= Propagation ; Gr= Generation Below are cases when the CLK="1" or the circuit is in evaluation mode *Scenario 1:*If X = logic 0 and Y = logic 0, then... Pr=XLY = logic0andGr = X.Y = logic0thenCout = logic0. In this scenario, the outputs of PROP, GEN, and Cout are consistently at logic 0.
Scenario 2: If X=logic 1 and Y=logic 0, then... Pr=XLY = logic1andGr = X.Y = logic0 When the propagation output (Pr) is 'logic 1', the carry output (Cout) equals the carry input (Cin), indicating a direct transfer of the carry input to the carry output. This state of the circuit is referred to as the Carry PROP state.
Scenario 3: If X=logic 1 and Y=logic 0, then... Pr=XLY = logic1andGr = X.Y = logic0 In this scenario, if the propagation output (Pr) equals 'logic1', then the carry output (Cout) equals the carry input (Cin), indicating a direct transfer of carry input to carry output. This condition signifies that the state of the circuit is "Carry PROP".
Scenario 4: If X=logic 1 and Y=logic 1, then... Pr=XLY = logic0andGr = X.Y = logic1 The generation output Gr be 'logic 1' in this case, Cout will be set to 'logic 1', denoting that the circuit is in the carry generation state. Conversely, whenever Clk is 'logic 0', Cout will remain 'logic 0'. This rule is valid for all the bits of mcc adders.

IV. The Standard Model Results

A. 16-bit manchester carry chain adder

The 16-bit manchester carry chain (MCC) adder is implemented utilizing FinFET technology and is illustrated in the below figure. Additionally, the necessary configurations for the inverter, XOR and AND gate modules are also designed using FinFET models. Moreover, signal propagation and generation symbols are generated, employing multiple n-LVT (LowVoltage Threshold) and p-LVT transistor

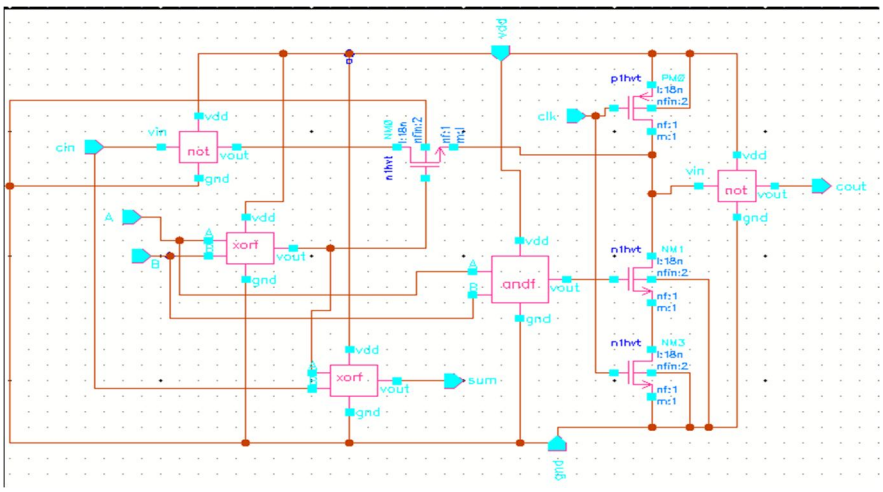


Fig. 3. 1-Bit mcc adder

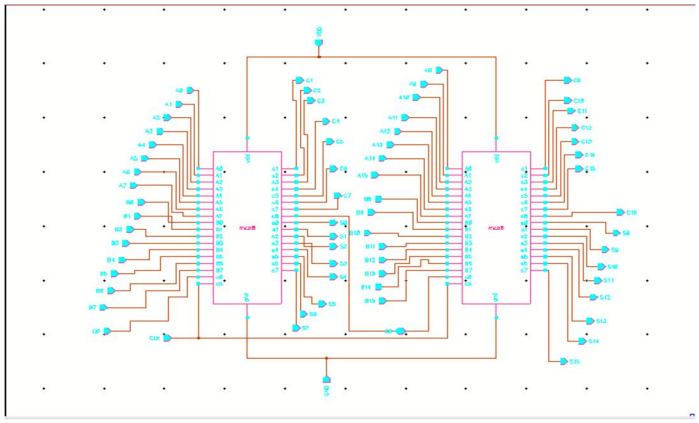
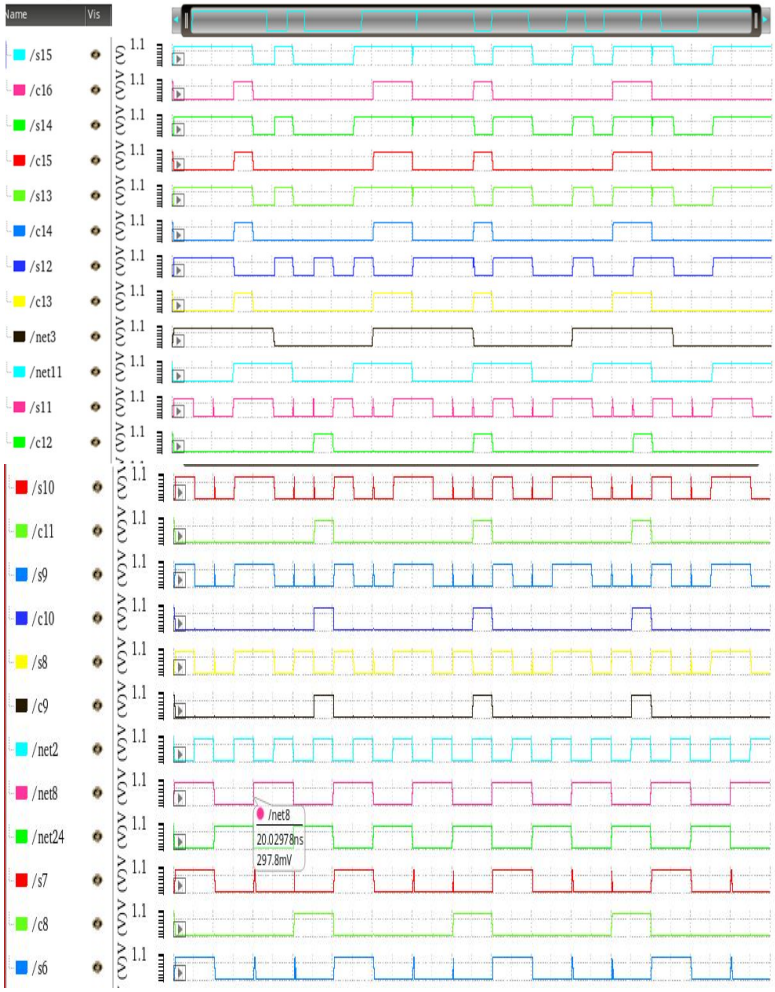


Fig. 4. Schematic view of 16-Bit mcc adder

B. Simulation Results

The transient behaviour refers to the system's behavior when it deviates from its stable state. It encompasses any condition affecting the system's equilibrium, not just on or off states. Using Cadence software and FinFET technology, schematic diagrams of 8-bit and 16-bit Manchester Carry Chain (MCC) Adders are simulated to study their transient responses. In these simulations, 0V represents logic '0' or an 'OFF' state, while 1V signifies logic '1' or an 'ON' state. It's important to note that in FinFET technology, the maximum voltage considered is 1V, with VDD set at 1V and GND at 0V, reflecting the characteristics of FinFETs.



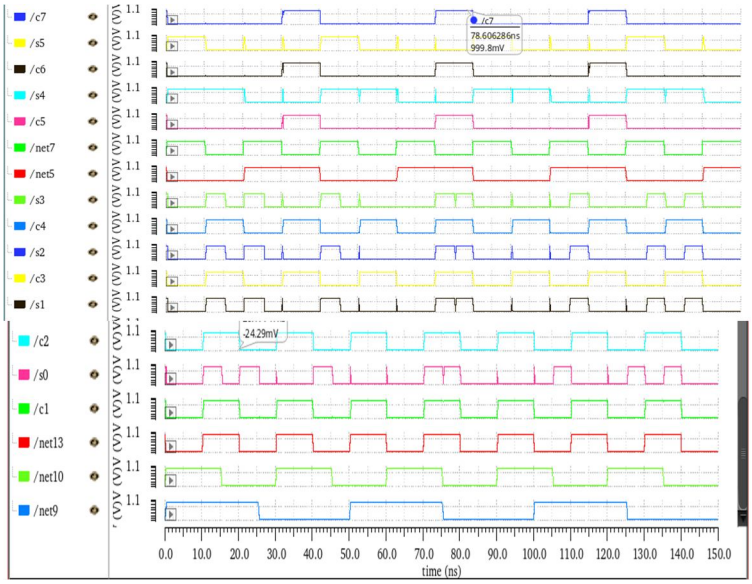


Fig. 5. Transient behaviour of 16-bit MCC Adder

V. Insights From Experimental Analysis

Using Cadence virtuoso FinFET technology, We observed the following analysis for 8-bit MCC Adders.

8 Bit MCCA(CMOS)	8 Bit MCCA(FINFET)
30ns	7ns

Fig. 6. COMPARISON OF DELAY BETWEEN 8-BIT CMOS AND 8-BIT FINFET MCC ADDER

The delay will be decreased rapidly. Specifically, the 8-bit CMOS MCC Adder demonstrates a delay of 30 ns, whereas the 8-bit FINFET MCC Adder exhibits a delay of 7 ns.

VI. Conclusion

Cadence Virtuoso is used as the main tool for designing and simulating Manchester Carry Chain (MCC) circuits. The software significantly improves circuit delay reduction, leading to enhanced overall performance and speed. Transient behaviour output shows the delay values reduced for both 8-bits CMOS and 8-bits FINFET MCC Adders. The 8-bit CMOS MCC Adder exhibits a 30 ns delay, whereas the 8-bit FINFET MCC Adder has a significantly lower delay of 7 ns, highlighting the enhanced efficiency of the suggested 8-bit FINFET MCC Adder. Future research will focus on designing for more than 16 bits, such as 32 or 64 bits by increasing the performance, delay and power concumption.

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