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Single-Ended Sub-Threshold FinFET based 8T SRAM Cell

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***Abstract*—In modern IC's scaling the supply voltage aggressively in SRAM which minimizes the active and leakage power. In the energy constrained application performance requirements are not an important factor, SRAM offers a read and write operation at the lowest supply voltage? In previous work, high -density bit cells are failed to operate at low voltage. In this project, high- density FINFET based 8T SRAM cell is designed with a single bit line which operates at the lower supply voltage. This is also used to achieve the parameter a low leakage power. The parameter is measured in the proposed system is leakage power. The proposed FINFET based 8T SRAM design and simulated using tannertool.**

***Index Terms*— Cache memories, CMOS memory circuits, leakage currents, low-power electronics, SRAM chips, FINFET.**

I. INTRODUCTION

Scaling of transistor dimension results in increased integration density and improved device performance. Increased density causes the increased leakage current which necessities ultra-low power operation. By reducing the supply voltage reduces the dynamic power and leakage power linearly. Hence, supply voltage scaling has a major focus on low-power design. This has resulted in circuits in operation at an offer voltage lower than the threshold voltage of a transistor [1]. The sensitivity of the circuit parameters to process variation increases due to the reduction in supply voltage. In a system on a chip, cache memories occupying a 90% of total die area. NanoscaleSRAM bit cells having a minimum sizedtransistor[4].

Coupled with inter-die and intra-die process variations, lower supply voltage operation results in various memory failures, i.e., read failure, hold failure, access time failure, and write failure [4].

Memory failure probability is predicted to be higher in future technology nodes [5]. Adaptive circuit techniques such as source biasing, and dynamic have been proposed to improve the process variation tolerance [6]. Self-calibration techniques to achieve low-voltage operation while keeping the failure probability under control have also been proposed [7]. The 6- transistor (6T) cell which uses a cross-coupled inverter pair is the de facto memory bit cell used in the current SRAM designs. Different types of SRAM bit cells have been proposed to improve the memory failure probability at a given supplyvoltage.

A Fin Field-effect transistor (FinFETs) is aMOSFET built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double gate structure. The name FinFETs implies the source/drain region forms fins on the silicon surface. The FinFETs devices have significantly faster

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switching times and higher current density than the mainstream CMOS technology. the Thicknessof the device implies the length of thechannel.
FinFETs is classified into two types: shorted-gate (SG) and independent-gate (IG). SG FinFETs are also called as three-terminal (3T) FinFETs and IG FinFETs as four-terminal (4T) FinFETs. In SG FinFETs, the front and back gates are physically shorted, whereas, in IG FinFETs, both the gates are physically isolated. Thus, in SG FinFET, shorted gates are jointly used to control.
Electrostatics of the channel.Hence, SG FinFETs show higher on-current and also higher off-current compared to IG FinFETs. Different signals or voltages are applied in IG FINFET. This enables the use of the back-gate bias to modulate the front gate linearly.IG FinFETs occupies a high area coverage due to the need for placing two separate gatecontacts.
Static random-access memory is a typeof semiconductor memory that uses bistable flip- flops to store each bit. SRAM exhibits a dataremanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.it does not need to berefreshed.
SRAM stores a bit of data on four transistors using two cross-coupled inverters. The two stable states characterize 0 and 1. During read and write, operations another two access transistors are used to manage the availability to a memory cell. To store one memory bit it requires six metal-oxide-semiconductor-field-effect transistors (MOSFET). MOFSET is one of the two types of SRAM chips; the other is the bipolar junction transistor. The bipolar junction transistor is very fast but consumes a lot of energy. MOFSET is a popular SRAMtype.
The SRAM is differentiating from DRAM which must be periodically refreshed.SRAM become faster and more expensive than DRAM. SRAM is typically used for cache memory in CPU while DRAM is used for a computer's mainmemory.
The proposed 8T has one cross-coupled inverter pair, in which each inverter is made up of three cascaded transistors. These two stacked cross-coupled inverters: M1–M2–M4 and M8–M6–M5 retain the data during hold mode. The write word line (WWL) controls only one nMOS transistor M7, used to transfer the data from the single write bit line (WBL). A separate read bit line (RBL) is used to transfer the data from cell to the output when read word line (RWL) is activated. Two columns biased feedback control signals: FCS1 and FCS2 lines are used to control the feedback cutting transistors: M6 and M2, respectively.

II. 6T FINFET BASED SRAM

An SRAM cell has 3 completely different states: standby (the circuit is idle), reading (the information has been requested) or writing (updating the contents).SRAM in operation in scan mode and write modes ought to have "readability" and "write stability", severally. The three different states work as follows:

A. Standby

If the word line isn't declared, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters shaped by M1 – M4will still reinforce one another as long as they're connected to the provision.

B. Reading

In theory, reading only requires asserting the word line WL and reading the SRAM cell state by a single access transistor and the bit line, e.g. M6, BL. Nevertheless, bit lines square measure comparatively long and have massive parasitic capacitance. To speed up reading, an additional advanced method is employed in practice: The scan cycle is started by pre-charging each bit lines BL and BL, i.e., driving the bit lines to a threshold voltage (midrange voltage between logical one associated 0) by an external module (not shown within the figures). Then declarative the word line WL allows each the access transistors M5 and M6, that causes the bit line BL voltage to either slightly drop (bottom NMOS semiconductor money supply is ON and top PMOS transistor M4 is off) or rise (top PMOS transistor M4 is on). It ought to be noted that if BL voltage rises, the BL voltage drops, and vice versa. Then the BL and BL lines will have a small voltage difference between them. A sense electronic equipment can sense that line has the upper voltage and so verify whether or not there was one or zero hold on. The higher the sensitivity of the sensitive electronic equipment, the faster the readoperation.

C. Writing

The write cycle begins by applying the worth to be written to the bit lines. If we tend to want to write down a zero, we'd apply a zero to the bit lines, i.e. Setting BL to 1 and BL to 0.This is the same as applying a reset pulse

to associate SR latch, which causes the flip flop to vary state. A one is written by inverting the values of the bit lines.WL is then declared and also the price that's to behold on is barred in. This works as a result of the bit line input drivers square measure designed to be abundant stronger than the comparatively weak transistors within the cell itself so that they will simply override the previous state of the cross-coupled inverters. In apply, access NMOS transistors M5 and M6 have to be stronger than either bottom NMOS (M1, M3) or top PMOS (M2, M4) transistors. This is simply obtained as PMOS transistors square measure abundant weaker than NMOS once same sized. Consequently, when one transistor pair (e.g.M3 and M4) is simply slightly overridden by the write method, the alternative transistors try (M1 and M2) gate voltage is additionally modified. This means that the M1 and M2 transistors can be easier overridden, and so on. Thus, cross-coupled inverters magnify the writing process.

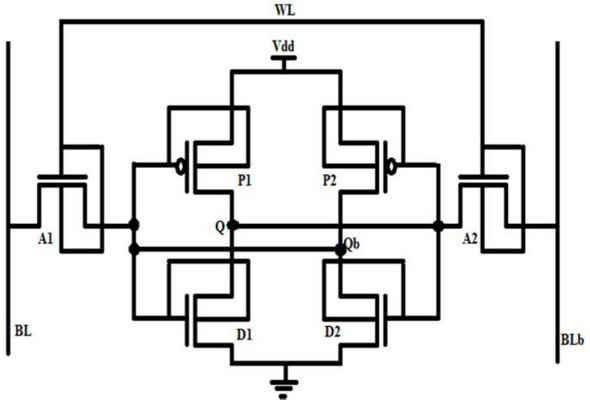

Fig 2.1. Structure of ternary FinFET SRAM cell

III. PROPOSED 8T BASED FINFETSRAM

To make a cell stable in all operations, Single-ended with dynamic feedback control (SFC) cell is presented in Fig. The single-ended design is used to reduce the differential switching power during reading–write operation. The power consumed during switching/ toggling of data on a single bit line is lesser than that on differential bit line pair. The SE-DFC enables writing through single nMOS in 8T. It also separates the read and writes path and exhibits read decoupling. The structural change of cell is considered to enhance The immunity against the process–voltage– temperature (PVT) variations. It improves the static noise margin (SNM) of the 8T cell in the subthreshold/near-threshold region. The proposed 8T has one cross-coupled inverter pair, in which each inverter is made up of three cascaded transistors. These two stacked cross-coupled inverters: M1– M2–M4 and M8–M6–M5 retain the data during hold mode. The write word line (WWL) controls only one nMOS transistor M7, used to transfer the data from the single write bit line (WBL). A separate read bit line (RBL) is used to transfer the data from cell to the output when read word line (RWL) is activated. Two columns biased feedback control signals: FCS1 and FCS2 lines are used to control the feedback cutting transistors: M6 and M2, respectively.

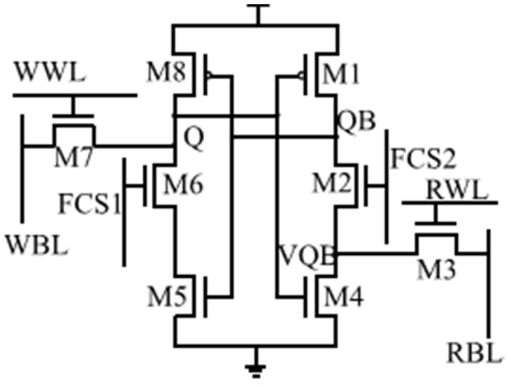

Fig 2.2.Proposed 8T. (a) Schematic

The feedback cutting scheme is used to write into 8T. In this scheme, during write 1 operation FCS1 is made low which switches OFF M6. When the RWL is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to a word bit line (WBL) is 1 and WWL is activated (Table II), then current flows from WBL to Q and creates a voltage hike on the letter of the alphabet via M7-writing one into the cell. Moreover, once the letter changes its state from zero to one, the inverter (M1– M2–M4) changes the state of QB from 1 to 0. To write a 0at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can visit a little negative price, and then the current from pull-up pMOS M1 charges QB to 1. The WT is measured asthe time Taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other. The simulations for WT were performed at all process corners. The WT (for write one and write 0) for 8T will increase with the decrease in the power supply. The WT is highest for slow nMOS and slow pMOS (SS) worst case corner. During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS (FF) process corner dominated by the fast switching activities. As write 0 operations is faster than write one, the write 0 power consumption during write zero is additional as compared therewith of write1.

A. Read Operation

The read operation is performed by pre-charging the RBL and activating RWL. If 1 is stored at node letter of the alphabet then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to the ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation, therefore, there is no direct disturbance on true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original zero prices when winning read operation. If Q is high then, the size ratio of M3 and M4 can govern the scan current and therefore the voltage difference on RBL. During read 0 operations, Q is 0 and RBL holds precharged high value and the inverted sense amplifier gives 0 at an output. Since M2 is OFF so virtual QB (VQB) is isolated from QB and this prevents the possibility of a disturbance in QB node voltage which ultimately reduces the read failure probability and improves the RSNM. During the read operation, if FCS1/FCS2 turns one before RWL is turned zero then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and Q, and any disturbance in QB will not affect Q. After that, if RWL goes low, the positive feedback will restore the respective states (Q = one and QB =0).

IV. Simulation Results Existingsystem

A. Output waveform for a write operation

SRAM Cell writes operation Consider that bit ’2’ is stored in the back to back FinFET inverter forwrite ’0’ operation. During this operation, D2 and P1 transistors are operating in the linear mode, while D1 and P2 transistors are turned off and the voltage at node Q = VDD and at node Qb = 0V before the access transistors are turned on which is shown in figure 4.2. When the access transistors A1 and A2 are turned on at that time voltage at node Q becomes 2.5V or 5V and the voltage at node Qb becomes 2.5V or 5V according to BL line. During this operation transistor, D1 operate in saturation and cut off regionrespectively.

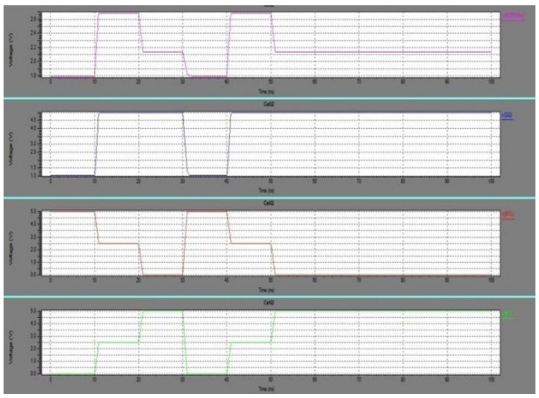

Fig 4.1 output waveform for a write operation

Above simulation, the result shows the output for a write operation. The first waveform for the word line and second for the output of write operation.Third and fourth for bit line bar and the bitline.

B. Output waveform for a read operation

Consider that bit '0' is stored in the back-to-back FinFET inverter. During the operation transistors, D1 and P2 operate in the linear mode, while D2 and P1 transistors are turned off.

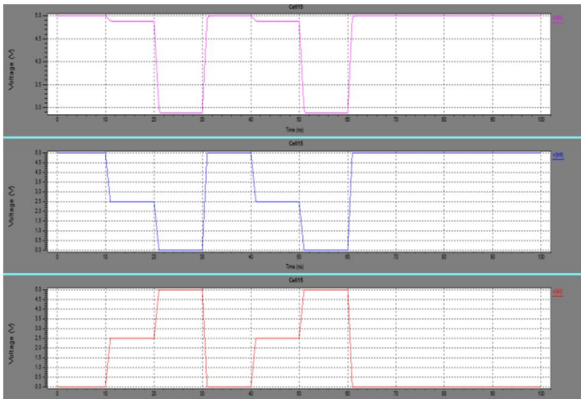

Fig 4.2 output waveform for reading Operation

Simulation result for SRAM read operation is shown in above first waveform shows the output for the read operation. The second and third waveform shows the waveform for bit line bar and bit line respectively.

V. THE PROPOSED SYSTEM OUTPUT WAVEFORM

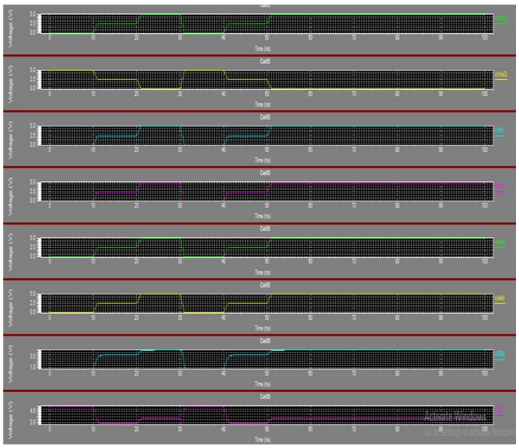

Fig 4.3 output waveform for 8t FinFET based SRAM cell

Above figure shows the output waveform for 8t FinFET based SRAM cell. Which gives the low power consumption compared with the 6t FinFET based SRAM.

TABLE I. AVERAGE POWER FOR READING AND WRITE OPERATION

System	Power dissipation in Write (µw)	Power dissipation in reading (µw)
Existing system	6.2E-7	9.45E-7
Proposed system	4.5E-7	8.6E-7

VI. CONCLUSION

Voltage scaling is an effective strategy for minimizing the power consumption of SRAMs. Further, as SRAMs continue to occupy a dominating portion of the total area and power in modern ICs, the resulting total power savings are significant. Unfortunately, however, conventional SRAMs, based on the 6T bit-cell, fail to operate at Low voltages, because of reduced signal levels and because of increased variation. To address these limitations, an 8T bit-cell is incorporated, it achieves full read and writes functionality. The advantage of reduced power consumption of the proposed 8T cell enables it to be employed for battery operated SoC design. Future and applications of the proposed 8T cell can potentially be in low/ULV and medium frequency operation like the neural signal processor, subthreshold processor, wide-operating-range IA- 32 processors, fast Fourier transform core and low voltage cache operation.

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