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Design and Reliability Assessment of ABCD to 7-Segment Converter with Emphasis on Noise Margins

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***Abstract*— The design and performance evaluation of a BCD-to-7-segment code converter circuit is presented with particular emphasis on its noise margin characteristics. Noise margin is a critical parameter that determines the reliability of digital circuits by quantifying their tolerance to electrical disturbances. To determine the Noise Margin High (NMH) and Noise Margin Low (NML) values for each of the seven output segments, the converter circuit was developed and examined in this study. The results show that NMH values range between 0.6526–0.8635 V, while NML values fall within 0.7785–0.8301 V. These findings confirm that all outputs exhibit strong immunity to both high- and low-level noise, with only minor variations across segments due to differences in their underlying Boolean logic functions. Notably, segment a demonstrated the lowest NMH, while segment e exhibited the highest NML, highlighting the balanced yet distinct behavior of individual outputs. The overall uniformity of the results indicates stable switching characteristics across the circuit, thereby ensuring dependable performance in practical display applications. The study concludes that the proposed BCD to 7-segment code converter achieves robust noise tolerance and is well-suited for reliable implementation in digital systems operating under noisy environments.**

***Index Terms*— BCD to 7-segment converter, Noise margin, Digital circuit reliability, Noise immunity.**

I. INTRODUCTION

The requirement for VLSI circuits with the high noise margin has grown as a result of the continuous development of wireless technologies, which have a limited power supply [1]. Noise margin is has become a major concern in contemporary digital circuits. Therefore, Maximizing the Noise margin is the main objective of VLSI designers. Every digital design is built on top of the inverter [2]. Creating increasingly intricate CMOS architectures after its characteristics and function are fully understood. One major obstacle to the creation of high performance circuits is the signal's generation, distribution, and propagation delay [3].

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The author of the study discusses a number of high-speed, low-power integrated circuit design techniques, including substrate biasing. By using this technique, device power consumption can be reduced without compromising speed [4].
It requires a lot of work to create precise, analytical formulas for timing models of basic circuits because noise margin is one of the biggest performance issues in CMOS digital circuits. Transistor-level simulators, like SPICE, that continuously simulate the devices can be quite expensive in terms of computation time and storage expenses. [5]. Because of this, a significant amount of earlier research has concentrated on developing analytical delay models without requiring expensive numerical iterations. To maintain a temporal relationship between functional blocks, gate-level safety characterization in the design space is necessary when designs become closer to the gates' complexity [6].
A lot of effort has gone into creating precise and practical models for CMOS-level transistor circuits in cadence libraries. These models are essential for managing or directing design options, technology migration, and process evolution. They are employed to evaluate certain structures' performance [7, 8]. In standard two-term delay modelling, a constant "inertial" characteristic of delay in the cell is linked to an output-load related delay characteristic of the cell's size and structure. In terms of overstated process dispersion, this picture could help designers focus their skills. Apparently, this is not enough in the submicron region where second-order effects are more prominent. The coupling effects of inputs and outputs pertaining to the speed saturation of the carriers provide non- linearity for the propagation delays, as is frequently observed. A thorough standard cell performance evaluation should take these effects into account because they are significant enough [9]. As a result, by changing the circuit design, the noise margin of the gate influences not only the environment and operation but also the wave shape of the input-switching signal, which is generally understood to be the time it takes for regulating gate's output and voltage to fluctuate between suitable voltage levels. These signal's rise and fall durations also have a considerable impact on the margin, resulting in a nonlinear change in the actual margin values. As a result, gate margin must be described while taking noise and output- transition lengths into consideration [10].
The present study examines the noise margin characteristics of each output segment of a BCD-to-7-segment code converter. By determining the noise margin high (NMH) and noise margin low (NML) values for all seven outputs, this work provides a comprehensive assessment of the circuit's resilience against electrical disturbances. The results not only highlight the variation of noise margins among different segments but also confirm the overall robustness of the design, thereby establishing its suitability for reliable operation in practical digital display applications.

II. EXPERIMENTAL

A. Simulation design

Cadence Virtuoso is a sizable, expert EDA (Electronic Design Automation) program that can implement nearly every aspect of layout design, experimental simulation, electronic design, etc. Software like Mentor Graphics and Synopsys, among others, have comparable features. However, Cadence Virtuoso offers more robust functionality for circuit modelling, circuit diagram design, layout design, and wiring than other EDA tools. Additionally, Cadence creates a process library for simulation and exchanges data with other semiconductor businesses, making it easy for customers to perform simulations. The process flow for conduction of this research work is based on the flowchart illustrated in Fig. 1.

Fig. 1. Process flow for simulation used in this research.

In terms of the process flow, the circuits for the BCD to 7-segment converter circuit after the schematic is implemented in the Cadence Virtuoso tool using gpdk090 technology. A single-stage BCD to 7-segment circuit is implemented with four inputs, which correspond to 4-bit BCD inputs B3B2B1B0, with B3 being the most significant bit (MSB) and B0 being the least significant bit (LSB). In addition, there are seven outputs, i.e., a, b, c, d, e, f, and g, which correspond to the 7-segments of the BCD to 7-segment circuit. The noise margins of all the outputs of the BCD to 7-segment circuit are determined and analysed. The DC analysis of the circuit was done to determine the noise margins of the circuit.

B. Static CMOS BCD to 7-segment circuit design

A BCD to 7-segment circuit is a combinational digital circuit that takes a 4-bit BCD input (representing decimal digits 0 to 9) and converts it into a 7-bit output to drive a 7-segment display. The 7-segment display consists of seven individual LED segments labelled a through 'g', which are arranged in a way to form decimal digits when specific segments are illuminated. Each segment is controlled by a separate output from the circuit. The BCD input, typically given as 4 bits (B3B2B1B0), can represent values from 0000 (Decimal 0) to 1001 (Decimal 9). The circuit contains logic gates, which map each valid BCD combination to the corresponding segment outputs needed to form the digit on the display. For example, to display the digit "7", segments a, b and c are turned ON. The circuit ignores or handles invalid BCD inputs (i.e., from 1010 to 1111) depending on the design. As mentioned earlier, a single-stage BCD to 7-segment circuit is implemented in the Cadence Virtuoso tool. A single-stage BCD to 7-segment converter circuit is implemented as a single complex static CMOS logic. The static CMOS circuits for the 7-segment a through g are designed using the Boolean expressions shown in Equations (1) through (7). Fig. 2(a) through 2(g) shows the schematic circuit for all 7-segments of a single-stage BCD to 7-segment converter. The details of the voltage sources used for BCD input are summarised in Table I.

$$\text{Segment a} = \overline{B_2}\,\overline{B_0} + B_1 + B_3 + B_2B_0 \quad (1)$$

$$\text{Segment b} = \overline{B_2} + \overline{B_1}\,\overline{B_0} + B_1B_0 \quad (2)$$

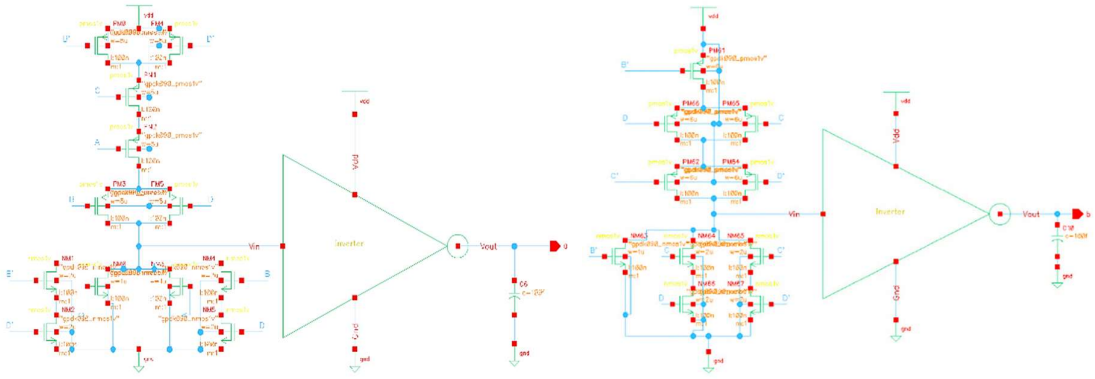
$$\text{Segment c} = \overline{B_1} + B_0 + B_2 \quad (3)$$

$$\text{Segment d} = \overline{B_2}\,\overline{B_0} + \overline{B_2}\,B_1 + B_2\overline{B_1}\,B_0 + B_1\overline{B_0} + B_3 \quad (4)$$

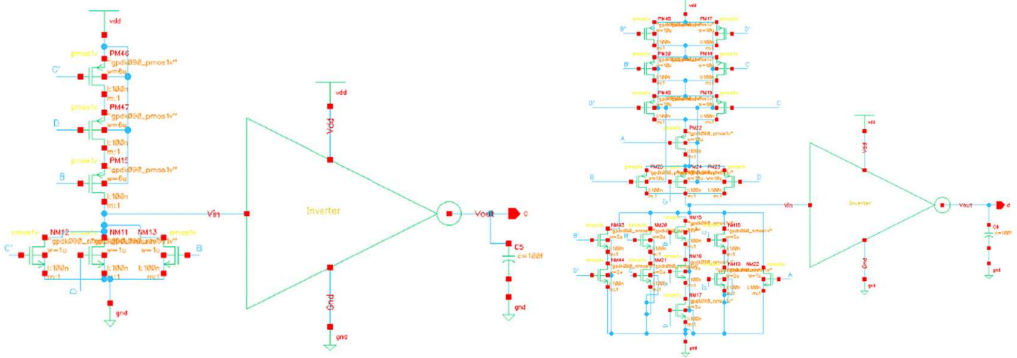
$$\text{Segment e} = \overline{B_2}\,\overline{B_0} + B_1\overline{B_0} \quad (5)$$

$$\text{Segment f} = \overline{B_1}\,\overline{B_0} + B_2\overline{B_1} + B_2\overline{B_0} + B_3 \quad (6)$$

$$\text{Segment g} = \overline{B_2}\,B_1 + B_2\overline{B_1} + B_2\overline{B_0} + B_3 \quad (7)$$



(a) (b)



(c) (d

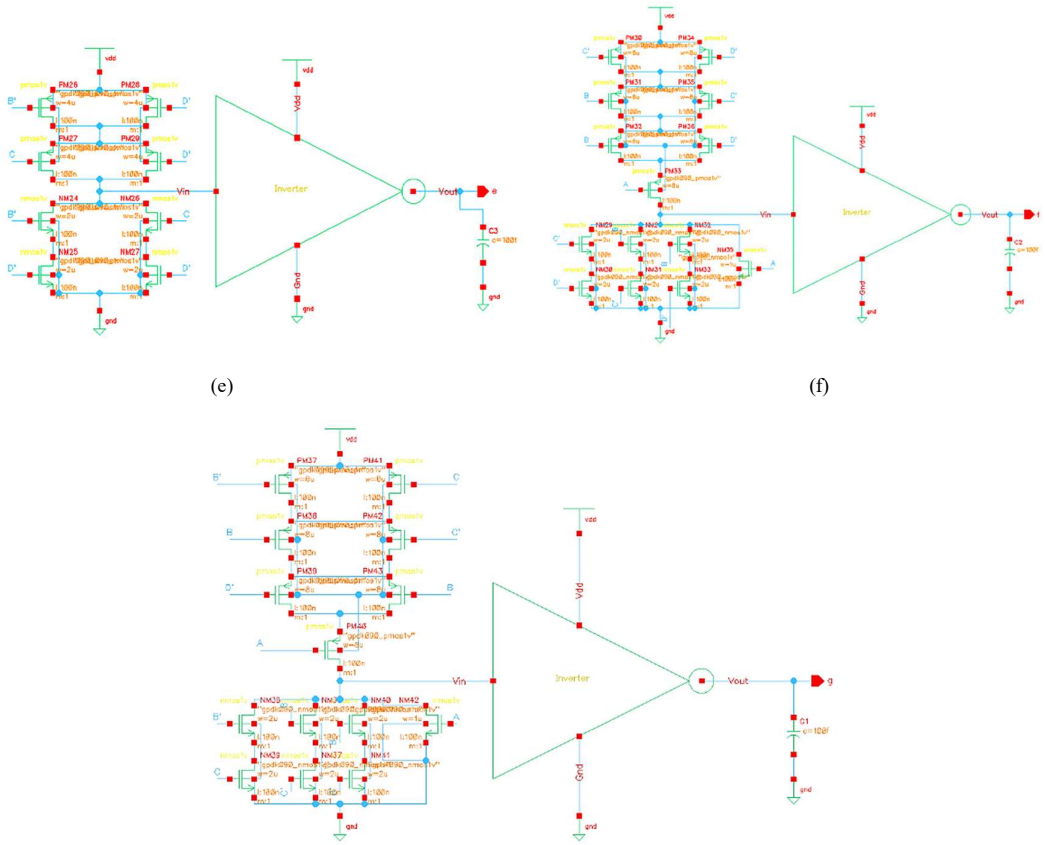


Fig. 2. Static CMOS schematic of a) Seg a, b) Seg b, c) Seg c, d) Segt d, e) Segt e, f) Seg f, and g) Segt g, of the BCD to 7-segment code converter implemented in Cadence Virtuoso gpdk090 technology.

TABLE I. DETAILS OF VOLTAGE SOURCES USED FOR BCD INPUTS

Voltage source	Period (ns)	Pulse width (ns)	Rise time (fs)	Fall time (fs)	Initial voltage (V)	Final voltage (V)
B3	10	5	50	50	0	1.8
B2	20	10	50	50	0	1.8
B1	40	20	50	50	0	1.8
B0	80	40	50	50	0	1.8

C. Noise Margin Calculation

This research focuses on the analysis of the noise margin of the 7-segment output in the single-stage implementation of the BCD to 7-segment converter circuit. Noise margin is the measure of a digital circuit's tolerance to unwanted electrical disturbances without causing an error in interpreting logic levels. In digital systems, a logic '1' and a logic '0' are represented by specific voltage ranges, and each device has defined threshold voltages for recognising these levels. The noise margin indicates how much the actual signal voltage can be disturbed by noise before it crosses these thresholds and is misinterpreted. There are two types: the high-level noise margin, which represents the safety gap between the minimum output voltage for logic '1' and the minimum input voltage recognized as logic '1', and the low-level noise margin, which represents the gap between the maximum output voltage for logic '0' and the maximum input voltage recognized as logic '0'. A larger noise margin means the circuit can handle greater noise levels without malfunction, making it an important factor in ensuring reliable operation of digital electronics. The DC analysis of the designed circuit is conducted to obtain the voltage transfer characteristics (VTC) curve. The VTC curve is a plot of Vout vs Vin of any given circuit. Fig. 3 shows the VTC curve illustrating the points V_{OH}, V_{OL}, V_{IL}, and V_{IH}. Here, V_{OH} is the minimum voltage output when the circuit is producing a logic 1, V_{OL} is the maximum voltage output when the

circuit is producing a logic 0, V_{IL} is the maximum voltage at which an input is still recognized as logic 0, and V_{IH} is the minimum voltage at which an input is recognised as a logic 1. The NM_H and NM_L are calculated using Equations (8) and (9), respectively.

$$NM_H = V_{OH} - V_{IH} \quad (8)$$

$$NM_L = V_{IL} - V_{OL} \quad (9)$$

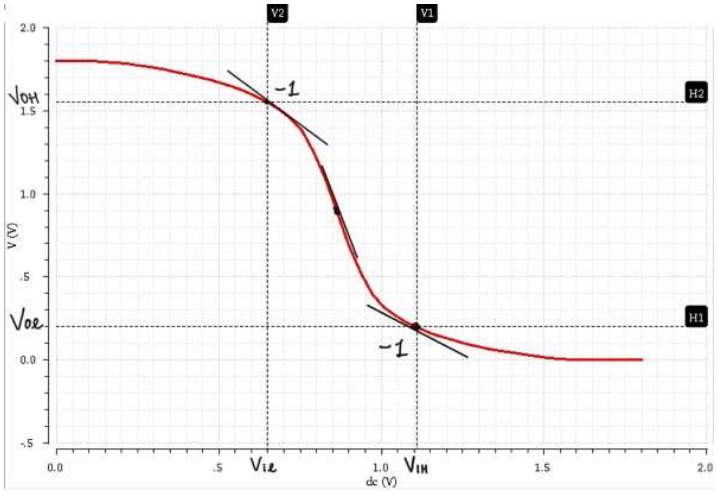
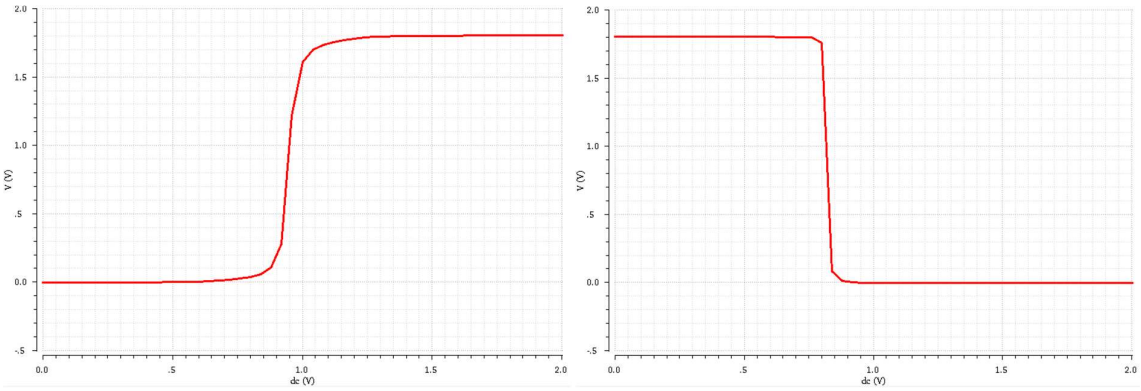


Fig. 3. Generalised VTC curve showing the points VOH, VOL, VIL, and VIH used in the calculation of the noise margin of circuits.

III. Results and Discussions

The primary goal of this work is to study the noise margin of all 7-segments of the BCD to 7-segment converter circuit. Noise margin is the parameter that is considered for this research. Noise margin is calculated as per the procedure described earlier. Switching transients, which disrupt the power supply or create crosstalk between nearby wires on the chip or circuit board, are the primary source of noise in digital systems. These disruptions can either add or subtract from the current signals, which alters the voltage that appears at the output. They can be transmitted to the input or the output. A valid logic level may become an illegal value if the noise level is high enough. The noise margin, which is defined for both logic high and logic low circumstances, is the amount of voltage needed to achieve this illegal state. It shows the highest noise voltage that can be present on an output prior to the output level being considered unlawful. Our research focuses on determining the noise margin of the BCD to 7-segment converter circuit. NMH and NML values are determined using Equations (8) and (9), respectively. As mentioned earlier, the noise margin of all 7-segment outputs of the BCD to 7-segment converter is determined by DC analysis of the circuit. Figs. 4(a) through 4(b) show the DC analysis of segment a through segment g, respectively. The summary of noise margin values for all the inverter circuits is illustrated in Table II.



(a) (b)

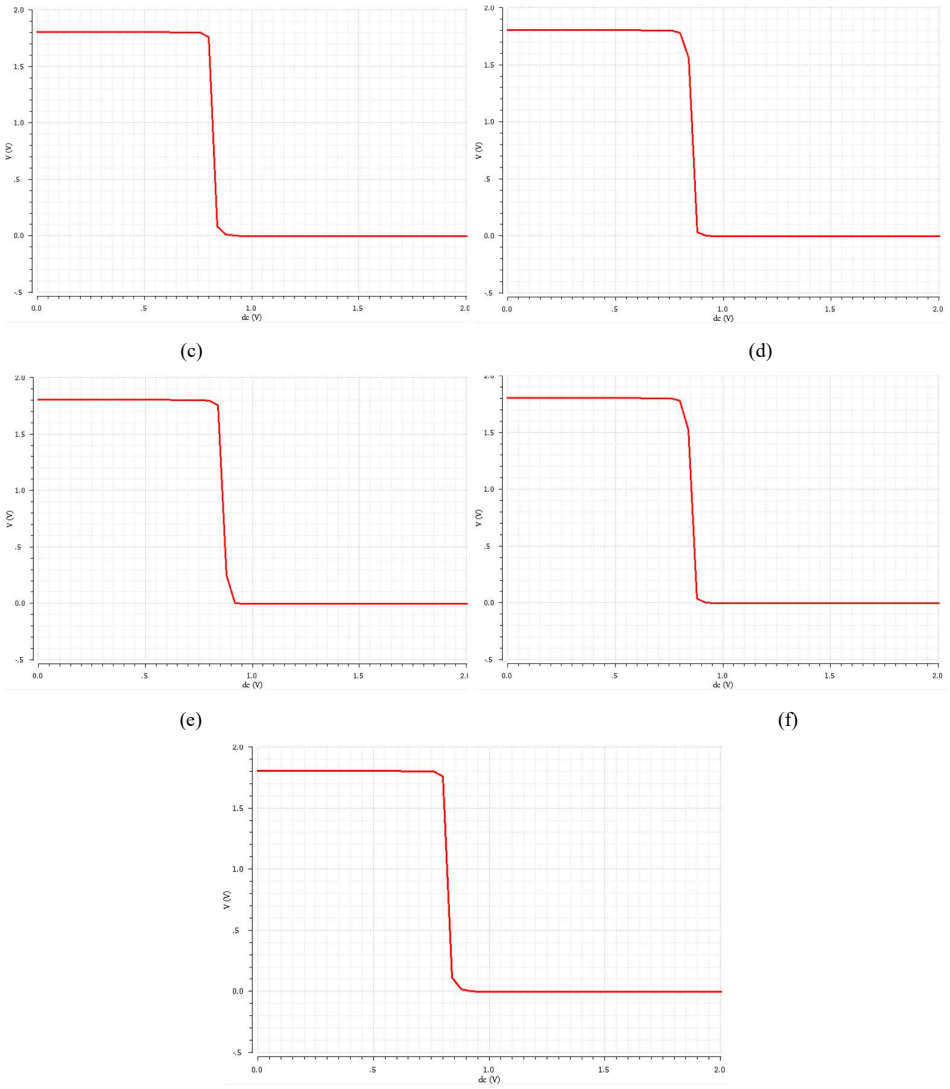


Fig. 4. DC analysis showing VTC curves of outputs, a) Segment a, b) Segment b, c) Segment c, d) Segment d, e) Segment e, f) Segment f, and g) Segment g obtained in Cadence Virtuoso tool.

TABLE II. SUMMARY OF NOISE MARGINS FOR ALL 7-SEGMENTS OF BCD TO 7-SEGMENT CODE CONVERTER CIRCUIT

Output	Noise margin	
	NM_H (V)	NM_L (V)
Segment a	0.6526	0.7785
Segment b	0.8635	0.7873
Segment c	0.8635	0.7873
Segment d	0.8368	0.7971
Segment e	0.8204	0.8301
Segment f	0.8356	0.7957
Segment g	0.8609	0.7856

Table II summarises the noise margins for each of the seven output segments of the BCD to 7-segment code converter circuit. As is well established in digital circuit theory, noise margins are critical indicators of circuit robustness, representing the limit to which a logic signal can tolerate unwanted electrical disturbances before it is incorrectly interpreted. As mentioned earlier, the noise margin high, i.e. NMH, quantifies the immunity of a

logic “1” against noise, while the noise margin low, i.e. NML, reflects the immunity of a logic “0.” Higher values of NMH and NML correspond to improved circuit reliability, as they indicate a greater tolerance for voltage fluctuations in the respective logic states. From the results, it is evident that the noise margins across all seven outputs fall within a relatively narrow range, with NMH values spanning from 0.6526 V to 0.8635 V and NML values lying between 0.7785 V and 0.8301 V. This uniformity indicates that the designed converter exhibits consistent switching characteristics across its outputs, even though each segment is governed by a distinct Boolean function. The close agreement of the values also demonstrates that the overall design ensures balanced performance, which is essential for driving display elements in noisy environments.

Among the outputs, segment a displays the lowest NMH of 0.6526 V, suggesting that it is relatively more vulnerable to high-level noise compared to the other segments. Nevertheless, its NML of 0.7785 V remains sufficiently high, ensuring reliable operation under low-level input conditions. On the other hand, segments b and c exhibit the highest NMH values of 0.8635 V, together with NML values of 0.7873 V. These results suggest that these two outputs possess the strongest resistance against noise in the logic “1” state, which can be attributed to the structural similarities in their underlying logic design. Segment e is particularly noteworthy because it demonstrates the highest NML value of 0.8301 V, indicating superior immunity against low-level noise disturbances. Although its NMH (0.8204 V) is slightly lower than that of segments b, c, and g, the overall balance of its noise margins highlights its reliability. Similarly, segments d and f present closely aligned NMH and NML values (0.8368 V/0.7971 V and 0.8356 V/0.7957 V, respectively), further reinforcing the consistency of the circuit’s behaviour. Finally, segment g also shows strong performance, with an NMH of 0.8609 V and NML of 0.7856 V, ranking it among the more robust outputs with respect to noise immunity.

Overall, the analysis demonstrates that the BCD to 7-segment code converter maintains NMH and NML values above 0.65 V and 0.77 V, respectively, across all segments. These values are well within the acceptable range for reliable digital operation, confirming that the converter can withstand moderate electrical noise without functional degradation. The relatively small variation between the outputs indicates that the design methodology ensures stable performance, with no single segment exhibiting a significant weakness. Such robustness is highly desirable in practical applications, particularly when the circuit is employed in digital display systems exposed to environmental noise and switching transients. In summary, the findings presented in Table II confirm that the designed BCD to 7-segment code converter is characterised by strong and well-balanced noise margins for all seven outputs. The minor variations observed across the segments are consistent with the logic-level differences inherent to each Boolean function and do not compromise the overall performance. These results validate the suitability of the circuit for reliable implementation in real-world digital display applications.

IV. Conclusions

The present work has investigated the noise margin characteristics of a BCD to 7-segment code converter circuit, with a particular focus on evaluating the robustness of its seven outputs against electrical disturbances. The analysis revealed that all outputs exhibit noise margin high (NMH) values in the range of 0.6526–0.8635 V and noise margin low (NML) values between 0.7785–0.8301 V, thereby confirming reliable operation across both logic states. Although minor variations were observed between individual segments—for example, segment a showing the lowest NMH and segment e achieving the highest NML —these differences remain within acceptable limits and do not compromise the overall performance of the circuit. The uniformity of the results demonstrates that the converter maintains consistent voltage transfer characteristics across all outputs, despite differences in their Boolean logic formulations. This ensures balanced and predictable behaviour when driving display elements, which is essential for practical implementation in digital systems. Importantly, the observed margins comfortably exceed the minimum thresholds required for noise immunity in standard logic families, reinforcing the suitability of the design for real-world applications. In conclusion, the BCD to 7-segment code converter exhibits robust noise immunity, stable operation, and reliable switching performance across all its outputs. These findings validate the effectiveness of the design methodology and confirm its applicability in digital display systems that demand both accuracy and resilience in noisy environments.

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