

Ternary Adder and Multiplier Design using GNRFETs

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Abstract—The ternary logic systems offer significant improvements in terms of bandwidth, operation, interconnect length and so on compared to two-valued logic. This work presents the proposal of novel digital circuits with ternary combination that decrease delay at lower power VLSI (Very Large Scale Integration) devices. The complicated circuits like multiplier and adder can be developed using GNRFET (Graphene Nano Ribbon Field Effect Transistor) without decoders and encoders circuits. The ternary adder, multiplier circuits based on GNRFET can be created and emulated utilizing the HSPICE (Hewlett Simulation Program with Integrated Circuit Emphasis) software. Also, it is examined the proposed circuits delay, EDP (Energy Delay Product), PDP (Power Delay Product) and Energy respectively. In order to show proposed design efficacy, performances of the proposed adder and multiplier designs are compared with CNTFET (Carbon Nanotube Field Effect Transistor)-based adder and multiplier designs.

Index Terms—Ternary logic, GNRFET, ternary multiplier and half adder.

I. INTRODUCTION

Conventionally, the binary logics are used for designing the digital logic circuits. Now-a-days, ternary logic circuits have more significance over the binary circuits because it minimizes the energy consumption, reduces the area and degrades the interconnect complexity [1-3]. The ternary logic is a three valued system represented the logics in voltages V_{dd} , $V_{dd}/2$, 0V for logic 2, logic 1, logic 0, respectively [4-6]. The design of three-valued logic circuits utilizing technology of CMOS is discussed in [7, 8].

Designing CMOS ternary circuits faces the hurdles like high current leakage and slow operation. Considering these problems, scientists proposed numerous transistor technologies like spin-wave, single-electron FETs, FinFET (Fin Field-Effect Transistor), CNTFET and GNRFET [9]. Out of all these transistor technologies, GNRFET has the better performance because of the excellent properties. In [2] the comparisons of CNT and GNR is shown. From the [2], it reveals that the GNR has superior qualities to the CNTs. Therefore, creating ternary circuits utilizing GNRFETs is a better method of creating future integrated circuits. [2, 10, 11] presents the design of GNRFET-based ternary logic circuits.

To create the ternary inverter, universal logic gates, full adder and half adder circuits in [2], GNRFETs are used. The performances are afterwards examined and contrasted with circuits of CNTFET. Ternary logic adder and multiplexer is designed using GNRFETs in [10]. The GNRFET adder and multiplexer's latency, PDP and power are compared to those of the currently used technology-based circuits. In [11], ternary basic and half adder circuits are presented. A comparative study is carried out for the GNRFET based circuits and existing circuits to show the

performance improvements. It is worth noting that all the existing papers on GNRFETs have high transistor count. Hence, in work, we have designed GNRFET based half adder and multiplier circuits with reduced transistor count. Furthermore, the performance is investigated in power, delay, PDP and EDP, respectively. The results are then contrasted with CNTFET ternary circuits in terms of performance.

The following lists the paper's main contributions

- Complex circuits based on GNRFETs are created using ternary logic.
- Numerical expressions are provided to evaluate the band gap, width, threshold voltage of GNRFETs.
- The performance of the proposed GNRFET-based circuits is examined, including delay, power, PDP and EDP and it is compared to the CNTFET-based circuits.

Rest of the paper is organised as follows: In Section-2, a thorough overview of GNRFETs and the proposed ternary is provided. TheSection-3 describes the simulation results and performance of the proposed circuits. The conclusions are discussed in Section-4.

II. DESIGN METHODOLOGY

The detailed discussion on the GNRFET structure is presented in this section. Then the discussion on unary operators is presented. In addition, a detail description about the ternary logic inverters and combinational circuits, half adder and multiplier are presented in this section.

A. GNRFET structure

The GNRs are atomically thin strips of graphene, typically whose width is less than 50nm, that have been shown to possess superior electrical properties. GNRFETs are composed of a semiconducting GNR channel, source, drain electrodes and a gate electrode. The electrical behavior of GNRFETs is strongly influenced by their band structure. Due to its planer structure, the GNRFET is more appropriate because it can be used in the current planer CMOS production process. GNR acts as semiconductor when dimer line value is $n=3p$ or $n=3p+1$ and acts as conductor for dimer line value $n=3p+2$ [2].

TABLE I: DESCRIPTION OF PARAMETERS FOR THRESHOLD VOLTAGE

Parameters	Description	Values
e	electron charge	$1.602 \times 10^{-19} \text{C}$
h	Planck's constant	$6.5 \times 10^{-16} \text{eV.s}$
a	C-C bond distance	0.142nm
v_f	Fermi velocity	10^6 m/s
n	number of dimer lines	$3p, \alpha=0.27$ $3p+1, \alpha=0.4$ $3p+2, \alpha=0.066$ Where p is an integer

GNRFET threshold voltage is calculated by

$$V_{th} = \frac{E_g}{3e} (1)$$

The GNR's (E_g) bandgap can be written as

$$E_g = 2|\alpha|\Delta E (2)$$

$$\Delta E = \frac{\hbar v_f \pi}{W} (3)$$

$$W = (n+1) \frac{\sqrt{3}}{2} a (4)$$

Where W and E_g are the GNR width and bandgap, respectively. The rest of the parameters are covered in Table 1. The structure of GNRFET is shown in Fig. 1. The GNRFET has undoped GNR layers underneath the gate terminal and highly doped GNR layers beneath the source and drain terminals. Donors or acceptors are doped for the GNRs under the source and drain regions in GNRFETs. The process of injecting donors into reservoirs is known as n-channel GNRFET, while the process of injecting acceptors into reservoirs is known as p-channel GNRFET.

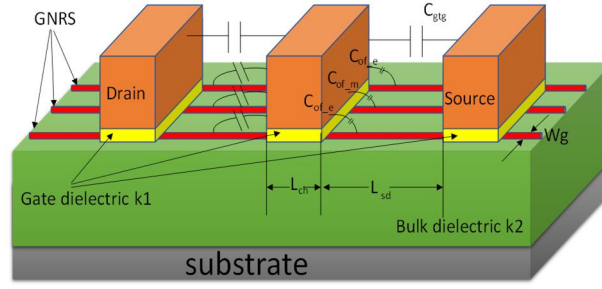


Fig. 1. Structure of GNRFET.

B. The proposed unary operators

Unary functions operate on single operands. In a two-valued binary system there are (2^2) four unary functions ('00', '01', '10', '11') but in the ternary system there are (3^3) twenty-seven unary functions ('000', '001', ..., '222'). Table 2 shows the eight unary functions that are needed to design the THA and TMUL.

TABLE II: UNARY OPERATORS OF TERNARY LOGIC

Ternary Input P	PTI P_p	NTI P_n	Cycle P^1	Operators P^2	$\overline{P^2}$	Decisive literal P_1	$1.\overline{P_n}$	$1.\overline{P_p}$
0	2	2	1	2	0	0	0	0
1	2	0	2	0	2	2	1	0
2	0	0	0	1	1	0	1	1

The P is the ternary input, positive ternary inverter (PTI) is the first function, the second function is a negative ternary inverter (NTI), the fifth function P^2 is the complement of $\overline{P^2}$ while the third and the fourth functions P^1 is $P+1$ and P^2 is $P+2$ are cycle operators. The final two unary functions are $1.\overline{P_n}$ and $1.\overline{P_p}$, while P_1 is the decisive literal.

C. Ternary logic inverters

Using six GNR-FETs, an STI circuit is designed and shown in Fig. 2 (a). By changing the width, the multi-threshold devices are controlled. When V_{dd} is set to 0.9, logic level 2 represents voltage level 0.9V, logic level 1 represents voltage level 0.45V and logic level 0 represents voltage level 0V. The main advantages of the STI circuit are robustness, less static power dissipation with minimal power usage and stays away from using big resistors. In the SPICE model, the transistors X1, X2 and X3 are placed by considering the value of n as 12, 6 and 9. The transistors' width of X1, X2 and X3 is calculated as 1.59nm, 0.86nm and 1.23nm and threshold voltages are 0.23V, 0.43V and 0.30V, respectively. The threshold voltages of p-GNR-FETs transistors X4, X5 and X6 are -0.30V, -0.23V and -0.43V. By increasing channel width, the transistors' switch state is decreased. In the above STI circuit, when the input voltage is $<0.23V$, X1 and X2 transistors become OFF state, X5 and X6 become ON state, since X4 and X3 are diode-connected transistors, they attain a drop in the voltage from node 2 to OUT and OUT to node 1. So, logic 1 is the voltage at the output. If the input voltage is $>0.45V$, the X5 and X6 transistors become OFF state and X2 becomes ON state. So, this discharges the output voltage to ground (GND).

In the PTI circuit, 0.43V and -0.23V are threshold voltages of transistors X1 and X2. When the voltage supply is $<0.45V$, X2 becomes ON state and X1 becomes OFF state, then V_{dd} is the output. If the input voltage increases $>0.45V$, then the output becomes 0V. In the NTI circuit, the transistors X2 and X1 threshold voltages are -0.43V and 0.23V, respectively. The output is changed to 0.9V and 0V if the input voltage drops to 0.23V. Fig. 2 (b) and Fig. 2 (c) shown in the below are the circuit diagrams of PTI and NTI respectively. The truth table of STI, NTI and PTI is shown in Table 3.

TABLE III. TRUTH TABLE OF STI, NTI, PTI

Input (P)	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

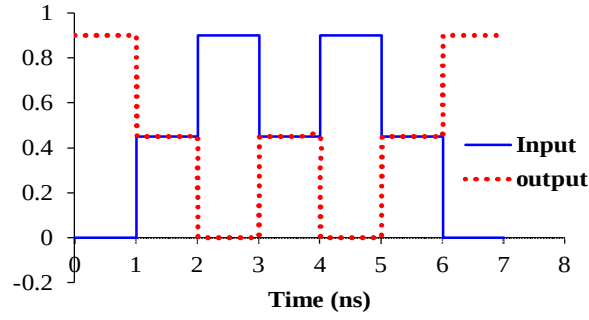


b) Ternary multiplier

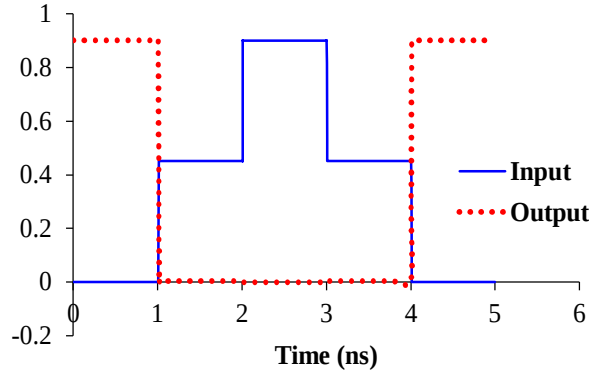
The designed TMUL with 26 GNRFETs utilizes transmission gates, dual voltages (V_{dd} , $V_{dd/2}$) and four unary operators. Ternary inputs (P , Q) of 1-trit TMUL multiplies and generates product, carry as outputs which are shown in the Table 4. In Fig. 4, the multiplier circuit diagram is displayed.

III. RESULTS AND DISCUSSION

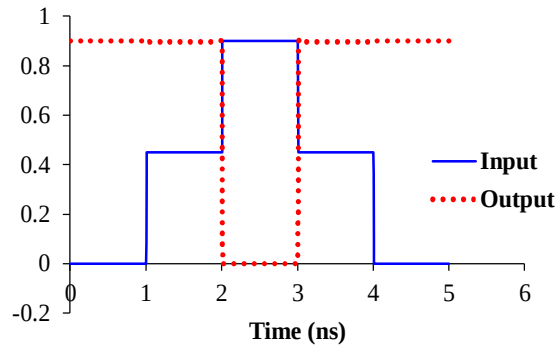
In this results discussion section, the proposed ternary circuit simulations and comparisons with circuits based on CNTFETs are shown. The HSPICE tool is utilised to simulate the proposed ternary logic inverters, TMUL and THA, respectively. The figures Fig. 5, 6 and 7 shows the output waveforms of inverters, THA and TMUL, respectively. The proposed ternary circuits are created using the GNRFET SPICE model that was presented in [12, 13].



(a)



(b)



(c)

Fig. 5. Waveforms of inverters (a) STI, (b) NTI, and (c) PTI

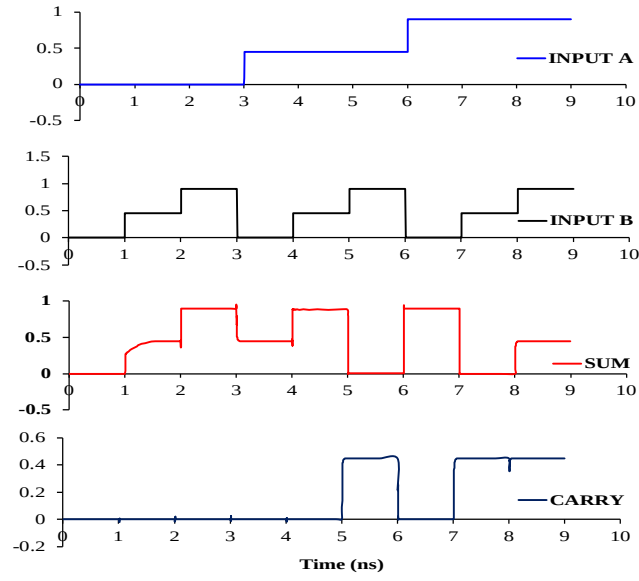


Fig. 6. Waveforms of THA with 35 GNRFETs

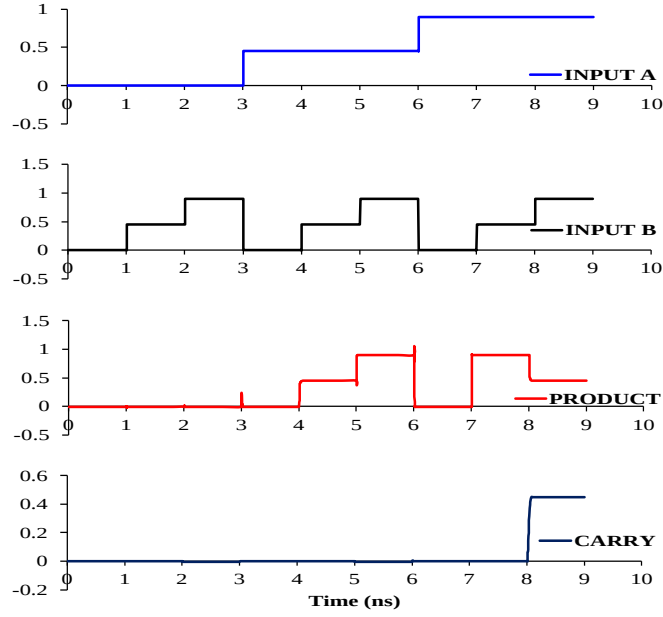


Fig. 7. Waveforms of TMUL with 26 GNRFETs

Table 5 compares the proposed GNRFET-based circuits with CNTFET-based circuits in a comparative analysis. According to the analysis, the GNRFET-based circuits outperform CNTFET circuits in terms of reduced delay, PDP and EDP. However, the power consumption of GNRFET circuits shows high compared to the CNTFET circuits due to the substantial driving capacity of the current. It is worth to note that the CNTFET SPICE model presented in [14, 15] is utilised to create the CNTFET ternary circuits.

TABLE V: COMPARISONS OF THA AND TMUL

Performance	THA		TMUL	
	CNTFET	GNRFET	CNTFET	GNRFET
Delay (ns)	20.557	2.1042	21.574	1.6426
Power consumption (μ s)	13.985	25.242	12.085	16.781
PDP (ps)	0.2874	0.0531	0.2607	0.0275
EDP (zs)	5.9099	0.1117	5.6248	0.0452

IV. CONCLUSION

The unique logic gates and circuits of ternary logic are shown using the GNRFETs technology. Number of dimer lines was found to alter the threshold voltage of the GNRFETs. This analysis leads to the proposal of multi-threshold GNRFETs. To create ternary logic gates like inverters and universal gates, GNRFETs are employed. Additionally, ternary half adders and multipliers are created without the need of decoders and encoders. In the HSPICE tool, the designed circuits are simulated. The comparative results shows that GNRFET circuits have reduced delay, PDP and EDP. It is found that the GNRFET based designs show reduced delay, PDP and EDP compared to CNTFET based designs. Thus, the presented GNRFET based design is more efficient than the CNTFET.

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