

A Wideband Low Noise Amplifier for 5G Applications using 45nm CMOS Technology

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Abstract— This paper presents the design of a wideband Low Noise Amplifier (LNA) for 5G applications operating in the frequency range of 28 to 32 GHz. --- The LNA uses a two-stage cascode (CS-CG) topology with inductive source degeneration -- The simulated peak gain is 21dB. The noise figure is less than 2dB with input and output port reflection coefficient less than -10dB. The LNA consumes significantly lesser DC power making it suitable for low-power applications. The circuit is implemented with 45nm low-power CMOS technology and simulated in Keysight Advanced Design System (ADS).

Index Terms— Low Noise Amplifier, 5G application, 45nm CMOS technology, wideband.

I. INTRODUCTION

The LNA is the primary component of a receiver front-end with the function to amplify the received signal without significantly degrading its signal-to-noise ratio. Since, LNA is the first block in a receiver it should have high gain characteristics and a low minimum noise figure. The performance of LNA is characterized by its gain, noise figure, stability, power consumption, input return loss, input, and output port reflection coefficient. The 5G short wavelength consisting of the frequency range 30GHz to 300GHz provides a solution for increasing bandwidth requirements and to overcome the shortcomings of existing frequency bands. The stated frequency band is called millimeter waves as the wavelength is in the range of 1 to 10mm. 5G millimeter wave covers only a small radius with higher data transfer rates thus they find applications in IoT and industrial automation. When employed in the cellular network it offers high speed and high capacity.

II. LITERATURE STUDY

Reference [1], they designed the LNA with three stages and achieved a peak gain of 23dB with a noise figure below 3dB. They have adopted the inductive source degeneration technique to achieve better noise performance. To achieve a lower noise figure, they have used a common source for the first stage followed by two cascode stages to target higher gain and better reverse isolation.

Reference [2], the circuit is designed with a 45nm bulk CMOS process for low-power 5G applications. The proposed circuit simulation results show it achieved a peak gain of 32dB with a noise figure of 3.3dB. The circuit requires low DC power of 7mW. Here, they have designed a transformer-based g_m boosted cascoded CG stage followed by a CS cascode amplifier stage.

Reference [3], the LNA is designed in a 22nm FDSOI process technology. They have designed for the frequency range of 20 to 30 GHz achieving a peak gain of 22dB with a noise figure between 2.77 to 3.4dB. They have used a drain to source capacitive feedback with their two-stage amplifier to have better stability.

Reference [4], an auxiliary amplifier method is used for wideband input matching, it also uses cascode spiral inductors to increase SRF while simultaneously taking into account impedance matching and gain peaking for operating frequency extension. This results in low-power broadband operation.

III. CIRCUIT DESIGN

In our work, we have used the 45nm low-power CMOS technology. This work can be split into three parts the Input Matching Network (IMN), the core amplifier stage, and the Output Matching Network (OMN). The LNA circuit is illustrated in Fig. 1 and the equivalent circuit of the LNA is given in Fig. 2.

The input and output impedance of the LNA should be matched to $50\ \Omega$ for maximum power transfer. For input matching and output matching, we have used filter-based LC networks, since they offer low sensitivity to component variations. The inductor L1 matches the circuit to $50\ \Omega$ on the input side and the inductor L7 and capacitor C1 match the circuit to $50\ \Omega$ on the output side.

For the core amplifier, we have designed a two-stage cascode amplifier. A cascode amplifier offers high output resistance, intrinsic gain, and large bandwidth, and reduces the Miller effect which suits our target for designing a wideband amplifier. Both stages employ the inductive source degeneration technique to achieve better noise characteristics. The first cascode stage consists of a common source followed by a common gate through an inductor to achieve gain flatness. The inductor L4 is used as a shunt-peaking inductor to enhance bandwidth. The second cascode stage is connected through an inductor L5 which is used for series peaking to enhance bandwidth. Inductive source degeneration is designed with the inductors L2 and L6.

The design flow for our work starts with the design of the core amplifier stage. Firstly, DC analysis was performed and the transfer characteristic curve was analyzed to determine the DC bias voltages. For the core amplifier, we employed cascode topology. With the DC circuit completed, we proceeded with designing the impedance-matching networks. The gain achieved did not meet our requirements. Thus, we designed a second cascode stage to achieve higher gain. With the core amplifier now being a two-stage cascode amplifier, the input matching network was designed. Finally, the output matching network was designed using a filter-based LC network.

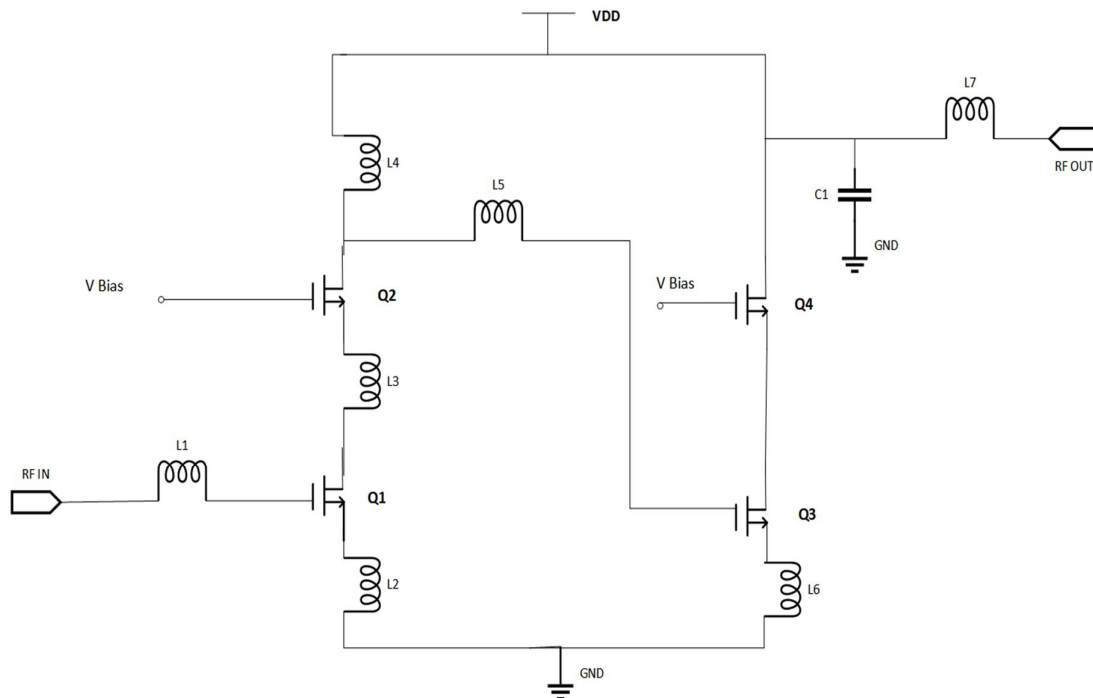


Figure 1. Two-stage cascode LNA (bias circuit not included)

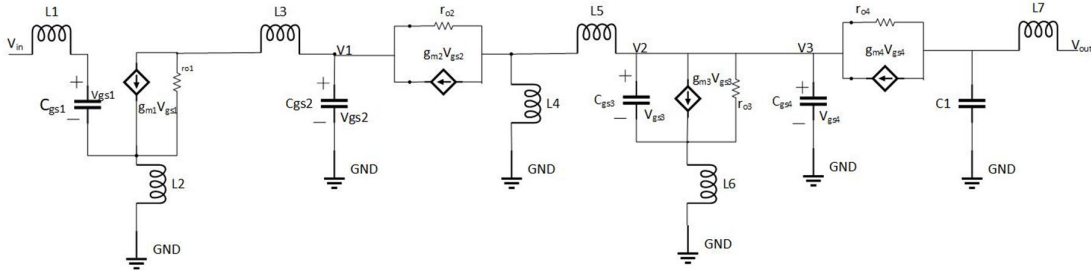


Figure 2. Equivalent circuit for the two-stage cascode LNA

The input impedance and output impedance can be derived from the equivalent circuit and equated as given in (1) & (2).

$$Z_{in} \approx sL_1 + \frac{1}{sC_{gs1}} + \left(1 + g_{m1} \left(sL_1 + \frac{1}{sC_{gs1}}\right)\right) sL_2 \quad (1)$$

$$Z_{out} \approx r_{o4} || gm \left(sL_7 || \frac{1}{sC_1}\right) \quad (2)$$

The total voltage gain is expressed as given in (3).

$$A_{VTotal} \approx A_{V1} \times A_{V2} \times A_{V3} \times A_{V4} \quad (3)$$

Here, the voltage gain obtained by transistor (M1) is A_{V1} , given in (4) and the voltage gain obtained by transistor (M2) is A_{V2} , given in (6).

$$A_{V1} \approx \frac{-gmZ_{L1}}{1 - gmZ_{L1}(sL_2)} \quad (4)$$

$$\text{where, } Z_{L1} \approx r_{o1} || \left(sL_3 || \frac{1}{sC_{gs2}}\right) \quad (5)$$

$$A_{V2} \approx gm_2 Z_{L2} \quad (6)$$

$$\text{where, } Z_{L2} \approx r_{o2} || sL_4 \left(sL_5 + \frac{1}{sC_{gs3}}\right) \quad (7)$$

Here, the voltage gain obtained by transistors (M3) and (M4) in the second stage are A_{V3} , and A_{V4} their respective voltage gains are given in (8) and (10).

$$A_{V3} \approx \frac{-gmZ_{L3}}{1 - gmZ_{L3}(sL_6)} \quad (8)$$

$$\text{where, } Z_{L3} \approx r_{o3} || \frac{1}{sC_{gs4}} \quad (9)$$

$$A_{V4} \approx gm_4 Z_{L4} \quad (10)$$

$$\text{where, } Z_{L4} \approx r_{o4} || \frac{1}{sC_1} (sL_7) \quad (11)$$

IV. SIMULATION RESULTS

The LNA was simulated in Keysight Advanced Design System. The performance was characterized based on the input and output port reflection coefficient (S_{11} and S_{22}), transconductance gain (S_{21}), reverse isolation (S_{12}), Noise Figure (NF_{min}), DC power consumption (P_{DC}), and stability factor (K). A 1.1-volt DC power supply is used to give proper bias voltage. The circuit when simulated achieved a gain of 20dB in the frequency range of 28 to 32 GHz with a peak gain of 21.2dB at 28 GHz as illustrated in Fig. 3. The gain is flat in the designed bandwidth which reduces distortion. The input and output port reflection coefficients are illustrated in Fig. 4. S_{11} is below -10dB from 28 to 32 GHz and S_{22} is below -10dB from 28 to 32 GHz.

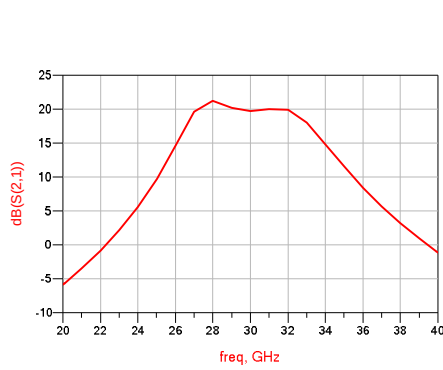


Figure 3. Forward Voltage Gain S_{21}

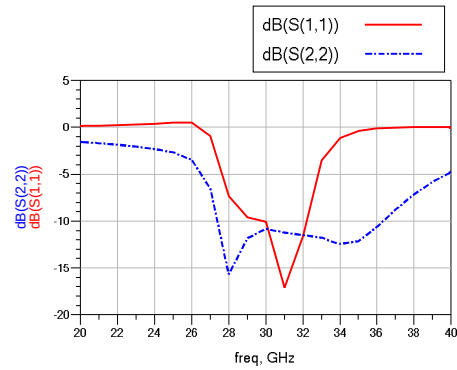


Figure 4. Input and Output Port Reflection Coefficient (S_{11} & S_{22})

The reverse isolation, S_{12} is well below -30dB over the entire frequency band of operation as shown in Fig. 5. The Noise Figure is less than 2dB throughout the designed frequency range as shown in Fig. 6. The input and output matching were done using passive components to achieve a lower noise figure. The DC power consumption is 3.35 mW which makes it suitable for low power applications. The LNA is stable with Delta less than 1, and K greater than 1 across the complete range of the proposed operating bandwidth. Equation (12) gives us Rollet's stability factor [6].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (12)$$

$$\text{where, } |\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \quad (13)$$

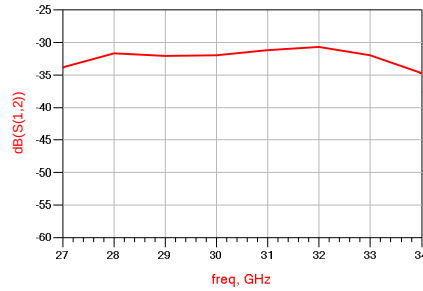


Figure 5. Reverse Isolation S_{12}

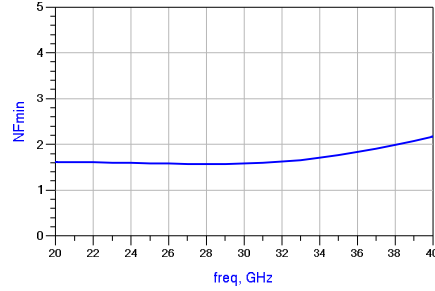


Figure 6. Minimum Noise Figure

A figure of merit is used to compare our work with other LNA designs of similar frequency range and it is shown in Table 1. The use of less noisy components for improved noise performance and the use of a significantly lower DC power supply helps our design in having a good figure of merit. The figure of merit (FoM) is formulated as given in (14).

$$\text{FoM} = \frac{\text{Gain (dB)} * \text{BW (GHz)}}{P_{DC} \text{ (mW)} * \text{NF}_{min} \text{ (dB)}} \quad (14)$$

TABLE I. PERFORMANCE COMPARISON

	Our work	[1]	[2]	[3]	[4]
Technology used	45nm LP CMOS	45nm SOI	45nm	22nm FDSOI	28nm
Center frequency (GHz)	30	29	28	25	41
Bandwidth (GHz)	4	6	3	10	43
Noise Figure (dB)	1.57	2.7	3.3	3.2	3.83
DC Power Consumption (mW)	3.35	28	7	35	13.74
Gain (dB)	21.2	23	32	22	18.4
FoM	16.12	1.82	4.16	1.96	15.03

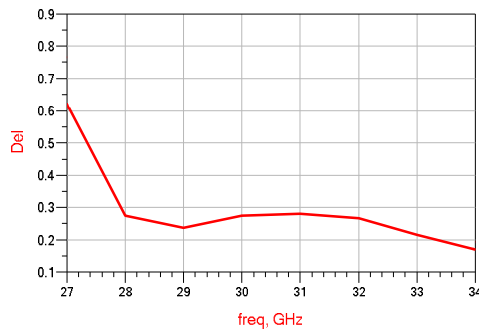


Figure 7. $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$

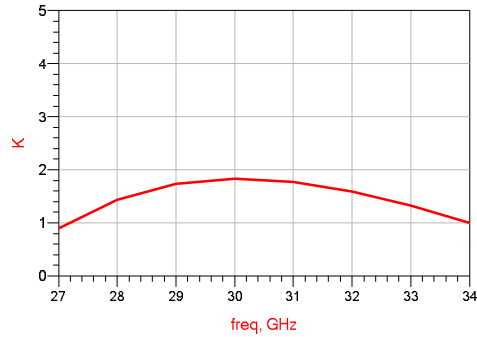


Figure 8. Stability factor K

V. CONCLUSION

A wideband LNA with high gain using 45 nm LP CMOS technology is presented. The proposed LNA circuit finds application in 5G communications operating at 30GHz. To achieve higher gain, a two-stage cascode configuration was employed. For improved noise performance inductive source degeneration was used and for bandwidth enhancement shunt and series peaking inductor, techniques were utilized. Collectively a peak gain of 21 dB with a minimum noise figure below 2dB and lower power consumption meets the requirements of mmWave communication.

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