

Design of 4-Bit Flash ADC using 28nm Technology in Cadence Virtuoso

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Abstract— The Flash analog to digital Converters (ADC) are known for their high-speed conversion and simple architecture, making them ideal for time-critical applications. This article provides the schematic-level design and simulation of a 4-bit Flash ADC in 28 nm CMOS technology in Cadence Virtuoso. The design includes a resistor ladder, an array of comparators made from pre-amplifier based comparators, and a thermometer encoder. The purpose of using pre-amplifier stages in the comparator array is to improve the sensitivity and reduce the offset of the comparator, ultimately enhancing speed and accuracy. This work shows that pre-amplifier based comparator designs have a significant improvement for their application to ADCs in advanced CMOS nodes, which may be useful for creating low-complexity and low-power analog-to-digital interfaces. Each sub-block was simulated, in isolation, to verify its working functionality. The test results show that the design operates at a clock frequency of 80 MHz, consuming a total power of 508.6 μ W, which is most effective for low-power, high-speed applications.

Index Terms— Flash ADC, Pre-amplifier comparator, 28nm CMOS Technology, Cadence Virtuoso.

I. INTRODUCTION

The Flash ADC is the fastest ADC architecture because it uses a fully parallel structure to generate its digital values. Flash ADCs may not be the best architecture from an area and power perspective when it comes to higher resolutions. Still, it will remain the architecture of choice for time-critical applications like high speed data acquisition, imaging, and many broadband communications systems [1-3]. A Flash ADC offers a 4-bit architecture that may not provide the best resolution, but it provides an ideal framework for high-speed ADC design concepts. The 4-bit Flash ADC uses a fundamental architecture based on a resistor ladder network feeding a bank of comparators and a thermometer-to-binary encoder. [4-5]. The flash architecture also allows its conversion to take place in parallel, leading to a prompt response time, important to applications where speed is favoured over resolution [6]. Advances in semiconductor technology have continually pushed the boundaries of possible operating speeds and functionality in the deep submicron scale technology nodes, resulting in faster speed and increased energy efficiency [8]. In recent years, attempts at designing analog components at this resolution have revealed new challenges, including increased process variability, greater mismatch, increased routing complexity, and spirit differences in design layout methodologies that need to be strategically addressed [9]. Therefore, schematic design must be developed in an exacting manner [10]. This work involves the full-custom schematic design of a 4-bit Flash ADC using a 28nm CMOS technology node.

The schematic design process began with the design of the key building blocks, which included the resistor ladder, the comparator array containing pre-amplifier based comparators, a thermometer-to-binary encoder, and an output buffer. Each block was designed to operate at full functionality, with careful attention to signal integrity and power consumption. The design shows a usable process for high-speed ADC design in advanced technology nodes, while indicating potential performance trade-offs that need to be assessed when designing analog circuits in deep submicron CMOS technologies.

II. LITERATURE SURVEY

Several advancements have been made in the design and optimization of Flash ADCs, focusing on achieving high speed, low power consumption, and reduced silicon area.

The authors Nampally Saikiran Varma et al. [1] introduce a low-power, high-speed Flash ADC. Specifically, they use energy-efficient comparators to achieve faster conversion while not significantly increasing total power consumption. They approached the study to determine how to optimize analog building blocks, including comparators and overall relevant design, to reduce dynamic power and preserve accurate conversion. Similarly, Tawan Chrysther dos Santos et al. [2] designed a 4-bit, 20-MS/s Flash ADC based on 65nm CMOS technologies that utilizes rail-to-rail comparators. Their new design extends the input dynamic range, in addition to adding transistor design with adjusted biasing to allow lower power surges, making it appropriate for low-voltage, low-power design.

The author Laxmi Koutanali et al. [3] built a small 3-bit Flash ADC based on Threshold Inverter Quantization (TIQ), where they rely on the inverter threshold instead of the resistor ladder, essentially preserving the area occupied by the resistor ladder on the Flash ADC, decreasing the total amount of components, and maintaining an efficient design without additional deviations or bad outcomes in smaller resolution. Finally, Ying Li et al. [4] studied low-noise, low-offset comparators in comparison to other types of comparators. They concluded StrongARM latch-based architecture with preamplifiers using floating inverters outperformed them in terms of speed, offset control, and noise.

Ajay Kumar Kapaka et al. [5] provide a complete Flash ADC design and verification workflow using Cadence and SystemVerilog RNM - it's an effective way to incorporate high-speed analog blocks into digital SoCs. The authors Arshiya Sadath et al. [6] have developed a new thermometer-to-binary encoder using full adders to minimize transistor count and delay, thus speeding up the overall speed and reducing the area of the ADC. The authors Hong-Hai Thai et al. [7] developed an 8-bit Flash ADC using double-tail comparators with TIQ-based encoding in 180nm CMOS. This structure not only minimizes the total number of comparators and the total power, but also provides a compact layout implementation. P. Vijaya Lakshmi et al. [8] developed a dynamic comparator using Cadence in 180nm CMOS. They were able to have ultralow power operation, 6.33uW with short delay, and suitable for low-power high-speed circuits. The authors Shanmukha Sai P. et al. [9] implemented a 4-bit Flash ADC with a two-stage open-loop comparator with a heterogeneous encoder, with reported power consumption and delay such that power is effectively balanced with speed (6.6 ns delay and 15.31 mW power). Nirali Hemant Patel [10] concentrates on biomedical applications in her work by developing a simplified, low-power 4-bit Flash ADC in 0.18μm CMOS utilizing an optimized comparator and an optimized encoder block in Cadence Virtuoso. Khatak et al.

The proposed work differs by designing the 4-bit flash ADC using the combination of a preamplifier-based comparator and a mux-based thermometer encoder, and focuses mainly on reducing the overall power consumption. The integrated approach enhances the efficiency and speed of the ADC.

III. BLOCK DIAGRAM

A. Block Diagram

Figure 1 depicts an architecture of a Flash ADC, which is typically implemented as an extremely fast type of ADC. A flash ADC performs its analog-to-digital conversion in a single clock cycle, which gives the ADC the capability for high-speed conversion needed for time-critical applications, such as video signal processing, high-speed data acquisition, or communication systems. The architecture consists of a resistor bank at the front-end (input stage), which acts as a voltage divider, and produces a set of linearly spaced reference voltages across the input signal range. The reference voltages would then be used for the comparator array. For an n-bit flash ADC, the resistor bank typically produces $2^n - 1$ reference voltages (distinct voltage levels) from the resistor network, where each tap from the resistor bank corresponds to the input threshold voltage used in the next stage. The next stage is an array of $2^n - 1$ comparators, where each comparator compares the input analog signal to one of the

reference voltages. The outcome of this stage is that the output of this comparator array, the output is a thermometer code, which is a unary code. A thermometer code will be in the form of a unary code where all the comparators that correspond to reference voltages lower than the input signals will output a '1', whereas the rest produce a complete '0'. The thermometer code will always uniquely represent the range in which the analog input lies. The output from the thermometer code can be processed into binary format using the thermometer-to-binary encoder. The encoder takes the transition location in the thermometer code (where the value changes from a '1' to a '0') and formulates this to an equivalent binary value. This allows for an effective and non-ambiguous transition from analog domain information, a thermometer code, to a compact digital code (a bit stream). The final digital output is buffered through an output buffer. This isolates the core logic circuits from the load at the output and will help ensure that the digital signals D3 to D0 are robust for digital processing in the next step. The final result will be a parallel digital output of the equivalent voltage to the initial analog input signal.

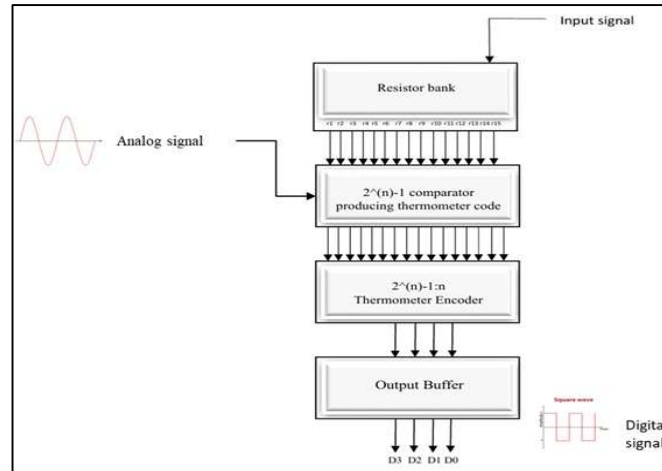


Figure 1. Block Diagram 4 Bit Flash ADC

IV. PROPOSED METHODOLOGY

This methodology proposes the design of a 4-bit flash ADC using 28nm CMOS technology in Cadence Virtuoso. The flow has a logical structure with steps starting from defining the system architecture, where a Flash ADC is composed of a resistor ladder network, 15 comparators, and a thermometer to a binary encoder. A comparator was designed based on a preamplifier topology that allowed greater resolution with reduced kickback noise due to a differential input stage, the decision circuit, and a dynamic latch design. The resistor ladder is made of matched poly resistors used to create 15 equally spaced reference voltages from a constant input voltage. To form the digital output, a transmission gate based encoder is used to convert the 15-bit thermometer code into a 4-bit binary output and accounting for the correct digital encoding. The Output from the thermometer encoder is given as the input to the driver circuit, which is also called the Output buffer. This output buffer is responsible for giving the high swing voltage.

A. Resistor Bank

The resistor bank, as shown in Figure 2, is one of the most critical parts in a 4-bit Flash ADC, since it provides 16 evenly spaced reference voltages for the comparator array. In this case, there are 15 resistors connected in series between two reference nodes, V_{ref+} (high reference) and V_{ref-} (low reference). The intermediate tap points, $r1$ to $r15$, are evenly and linearly spaced voltage levels between V_{ref+} and V_{ref-} and act as static thresholds for the 15 comparators in the ADC. With the proper reference voltages, when compared against the input analog signal, the comparators can establish the quantization range in which the input signal falls. It is, therefore, important for the resistor bank in an ADC to possess accuracy and linearity concerning these voltage levels, since this would ultimately lead to an accurate digital output. This means that resistor matching and the symmetrical layout of the resistors become somewhat important things to look at in practical design. The voltage difference at each tap can be mathematically calculated using “(1).”

$$V_n = V_{ref-} + [(n/N) * (V_{ref+} - V_{ref-})] \dots\dots\dots (1)$$

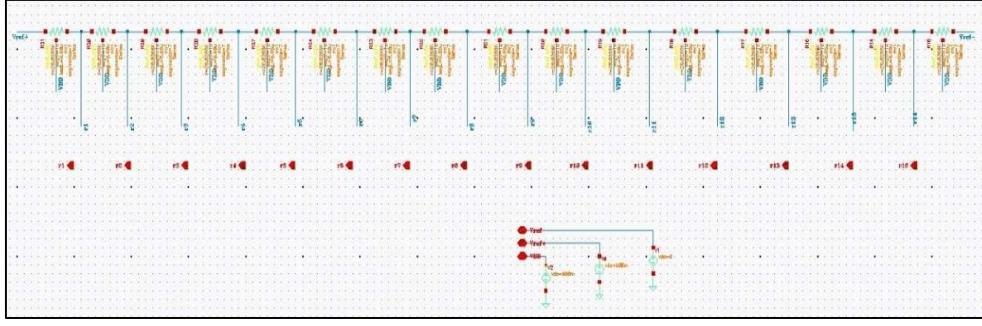


Figure 2. Resistor Bank Schematic

TABLE I: TAP VOLTAGE CALCULATION

Tap Index (n)	Output Voltage V_n (mV)
15	56.25
14	112.5
13	168.75
12	225.0
11	281.25
10	337.5
9	393.75
8	450.0
7	506.25
6	562.5
5	618.75
4	675.0
3	731.25
2	787.5
1	843.75

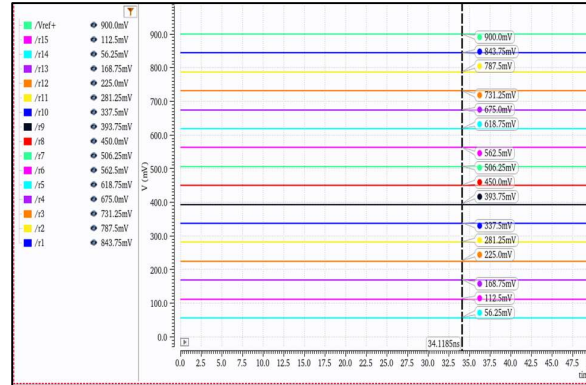


Figure 3. Transient analysis of Resistor Bank

The transient analysis of the resistor ladder network shown in Figure 3 indicates that the simulated voltage values correspond well to the values shown in Table 1. The outputs of the resistor ladder are then applied as the V_{in-} inputs of the comparators in the next stage.

B. Pre-Amplifier Based Comparator

The pre-amplifier based comparator, shown in Figure [4], is designed using 28nm CMOS technology and consists of three major stages: a differential pre-amplifier, a regenerative latch, and a CMOS buffer output stage. The differential amplifier is constructed using NMOS transistors biased using a current mirror to amplify the small voltage difference between V_{in+} and V_{in-} . It provides additional input sensitivity as well as decouples the input from the kickback noise caused by the latch stage that stems from the output transition when the logic has changed. The amplified signal is presented to the regenerative latch that is made up of cross-coupled PMOS and NMOS transistors, which can provide strong positive feedback which ensuring that the latch inverts rapidly

based on the polarity of the inputs. The output from the latch is passed through an analog CMOS inverter buffer stage to get an output that is a sharp digital signal with a full swing at the output node V_{out} , and helps to keep output load recognition isolated. The biasing currents needed for the comparator are sourced and generated using diode-connected devices and current mirrors, which helps maintain the comparators operational even as temperature-related to device parameters change. Figure [5] illustrates the transient simulation of the pre-amplifier comparator. The output voltage (V_{out} , red) provides full-swing digital transitions between 0 mV and 900 mV, which confirms that the comparator is operating correctly. The waveform demonstrates two well-defined transitions, which indicate that the comparator has detected the precise moment that the input differential voltage transitions between positive and negative voltage levels due to the regenerative positive feedback action of the cross-coupled latch stage.

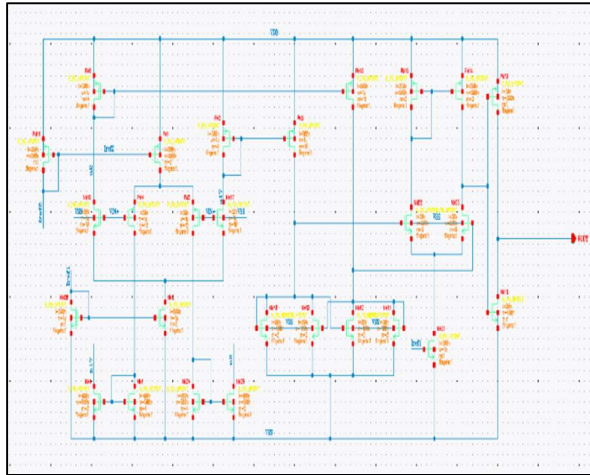


Figure 4. Pre-amplifier Based Comparator Schematic

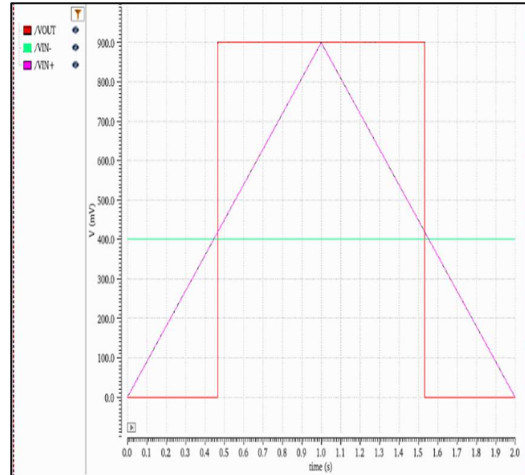


Figure 5. Transient Analysis of Comparator

C. Thermometer Encoder

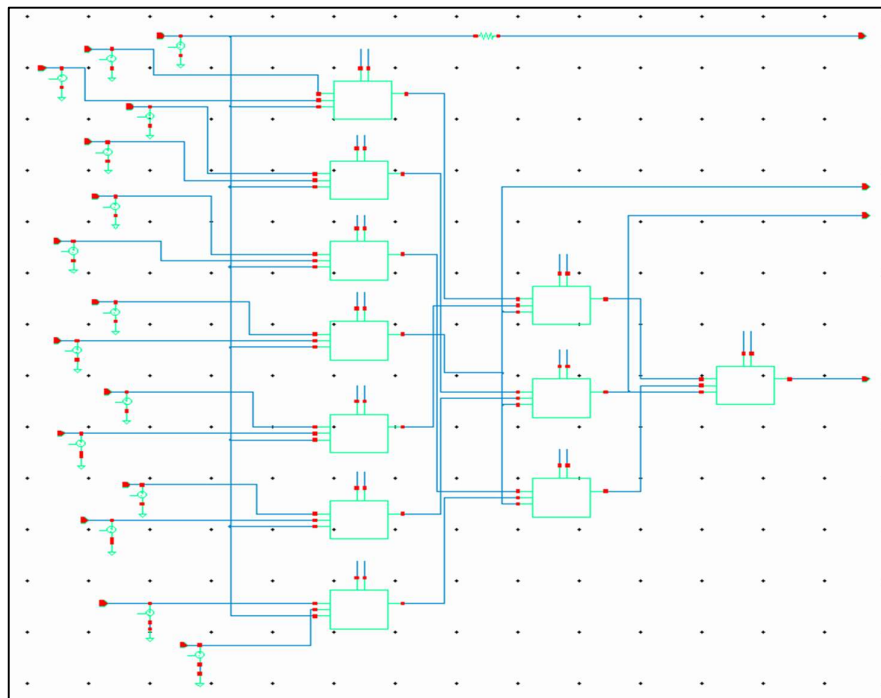


Figure 6. Thermometer Encoder Schematic

Figure 6 depicts the schematic of a thermometer-to-binary encoder using a hierarchical structure of transmission gate multiplexers (TGMUX). The encoder outputs a 4-bit binary representation of a 15-bit thermometer code taken from the comparator circuit array of a 4-bit flash ADC. Each 2:1 multiplexer takes the form of CMOS transmission gates, which can achieve full voltage swing operation while maintaining low propagation delays and low static power consumption. The thermometer code exhibits a pattern of '1's in a sequence always followed by '0's; thus, the encoder uses multiple levels of cascaded multiplexers to discern the location of the last active bit. The encoder employs priority detection, resolving the logic and data flow of the multiplexer hierarchy to find the last index of high logic in the thermometer input. Compared to traditional gate-based encoders, this structure lowers complexity and provides added benefits of cleaner logic flows with consistent incidental signal delays, and maintains a structure in CMOS technology that is more appealing for high-speed operation, as in 28nm processing. The TGMUX architecture further enhances area efficiency and avoids static contention, while maintaining very good performance in low-power, high-speed CMOS-based ADC architectures. The output of the encoder feeds directly into the digital output register to complete the analog to digital conversion process.

TABLE II: TAP VOLTAGE CALCULATION

Thermometer Code (15-bit)	Binary Output (4-bit)
0000 0000 0000 000	0000 (0)
0000 0000 0000 001	0001 (1)
0000 0000 0000 011	0010 (2)
0000 0000 0000 111	0011 (3)
0000 0000 0001 111	0100 (4)
0000 0000 0011 111	0101 (5)
0000 0000 0111 111	0110 (6)
0000 0000 1111 111	0111 (7)
0000 0001 1111 111	1000 (8)
0000 0011 1111 111	1001 (9)
0000 0111 1111 111	1010 (10)
0000 1111 1111 111	1011 (11)
0001 1111 1111 111	1100 (12)
0011 1111 1111 111	1101 (13)
0111 1111 1111 111	1110 (14)
1111 1111 1111 111	1111 (15)

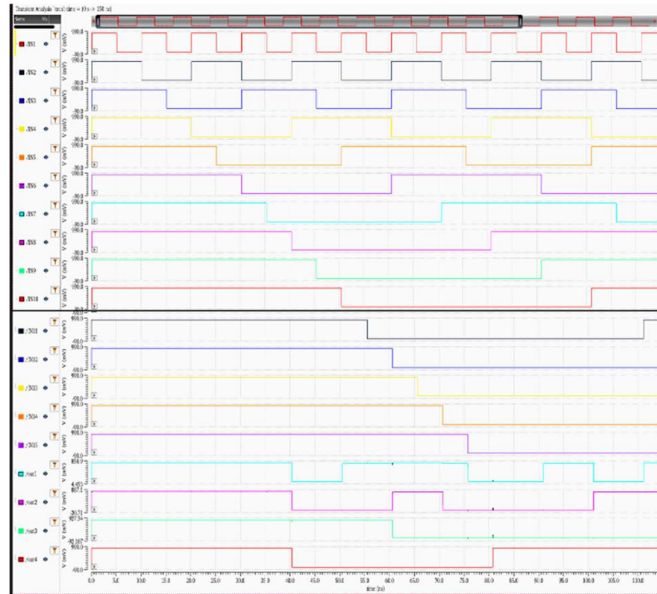


Figure 7. Transient Analysis of Thermometer Encoder

Table 2 shows how the expected output of the thermometer encoder has to be when the thermometer code from the comparator is given as the input to the encoder. Figure 7 shows the transient analysis of the thermometer encoder circuit, and the waveform is verified for its correctness and functionality.

D. Output Buffer Circuit

Figure 8 shows the schematic of the output buffer circuit. This output buffer is an optional circuit. Its main operation is to give the signal a boost, which is the high swing at the output terminal. The schematic involves two buffers connected in series, forming a two-stage buffer circuit at each pin.

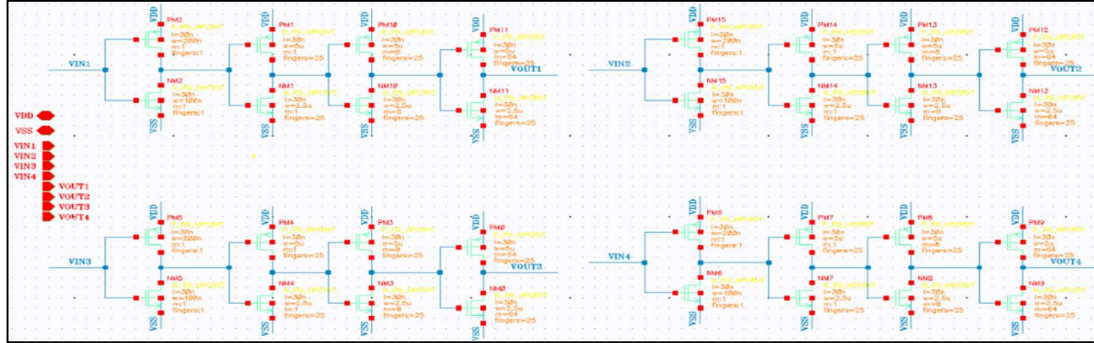


Figure 8. Output Buffer Circuit

V. RESULTS

Figure 9 is a top-level view of the full 4-bit Flash Analog-to-Digital Converter (ADC) architecture. This design incorporates 16 comparators running in parallel, each having a unique reference voltage that is received from the resistor ladder network. By doing this, the following 16 reference voltages will utilize the full-scale input range from 0 to 900 mV in 16 steps of 56.25 mV for each comparator. All comparators are comparing the input analog signal to the reference simultaneously, producing a thermometer code. A digital encoder block is then responsible for producing a 4-bit binary code from the thermometer code. Figure 10 displays the transient analysis of the 4-bit Flash ADC, depicting its functionality in real-time. As seen, the analog input signal varies sinusoidally from 0 mV to 900 mV, sampled, and represented in digital format. This analog input signal will fall into the specific voltage ranges as specified, for example, when an input is at 0-56.25 mV will output 0000, and an input at 843.75 mV-900 mV will produce an output code of 1111.

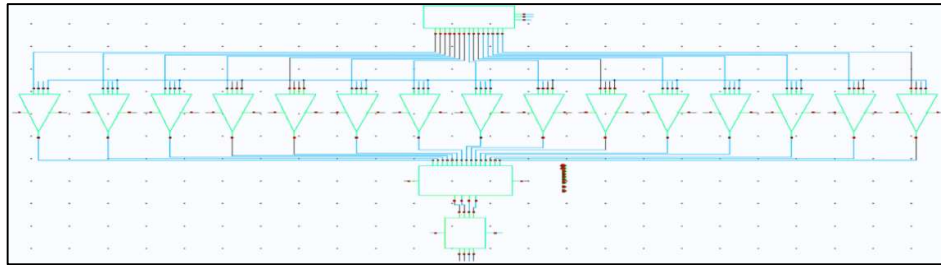


Figure 9. Top Level View of 4-Bit Flash ADC

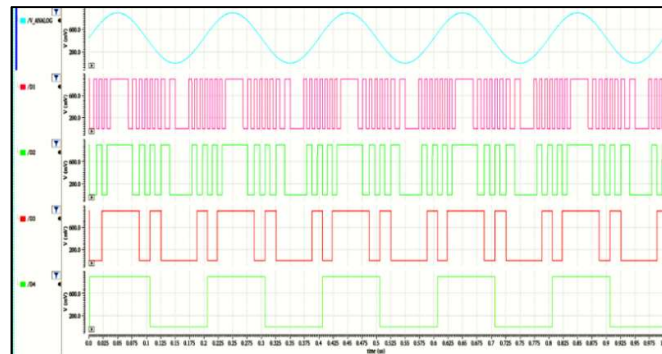


Figure 10. Transient analysis of 4-Bit Flash ADC

TABLE III: BINAY VALUE FOR I/P VOLTAGE

Input Voltage Range (mV)	Binary Output (4-bit)
0 – 56.25	0000
56.25 – 112.5	0001
112.5 – 168.75	0010
168.75 – 225	0011
225 – 281.25	0100
281.25 – 337.5	0101
337.5 – 393.75	0110
393.75 – 450	0111
450 – 506.25	1000
506.25 – 562.5	1001
562.5 – 618.75	1010
618.75 – 675	1011
675 – 731.25	1100
731.25 – 787.5	1101
787.5 – 843.75	1110
843.75 – 900	1111

VI. CONCLUSION

This paper describes the design of a 4-bit Flash Analog-to-Digital Converter (ADC) in 28nm CMOS technology, which was successfully designed utilizing a preamplifier-based comparator. Furthermore, the ADC operated successfully at 80 MHz with a power consumption of 508.6 μ W, with delays approaching 89.86 ns, demonstrating extremely reliable performance for many high-speed and low-power applications. The results of the ADC support the use of pre-amplifier stages in future high-speed sensors, demonstrating improved accuracy and noise performance, further showing their effectiveness when comparing previous results in deep-submicron encounters.

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