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An Area and Power Efficient Kogge Stone Adder using Gate Diffusion Input Logic

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***Abstract*— Gate Diffusion Input Logic (GDI) is utilized to build a novel design method for an area and efficient Kogge Stone adder, a widely used high-speed parallel adder. The aim of this is to reduce the space required for the circuit while maintaining the same degree of performance by utilizing the Gate Diffusion Input Logic (GDI). The study gives a thorough examination of the circuit architecture, power estimation, area estimation, and delay analysis of the GDI logic-based Kogge Stone adder. The proposed design is compared in terms of area, power, and delay to the Kogge Stone adders, which use CMOS (Complementary Metal-Oxide Semiconductor) and Pass Transistor Logic (PTL). The findings suggest that the GDI logic-based design may be beneficial for digital signal processing and other applications requiring compact, low-power and low-area calculations. This analysis makes use of the Tanner EDA Tool.**

***Index Terms*— PTL, KSA, Area consumption, VLSI, PPA.**

I. INTRODUCTION

Two n-bit binary values can be added efficiently and in high parallel using a class of digital circuits called parallel prefix adders. They are regularly used in high-performance computing applications where speed and efficiency are crucial factors. The traditional method for adding two n-bit values consists of a chain of full adders coupled in a ripple-carry arrangement. Due to each complete adder depending on the carry signal from the previous step, this approach has a high latency. Parallel prefix adders use a carry-look ahead technique to get around this restriction, which enables several complete adders to operate at once without having to wait for the carry signal from earlier stages. Parallel prefix adders use a carry-look ahead technique to get around this restriction, which enables several complete adders to operate at once without having to wait for the carry signal from earlier stages. Due to the demand for faster and more efficient arithmetic operations in digital signal processing and VLSI applications, various adder designs have been created. One of these systems, the Kogge Stone Parallel Prefix Adder (PP-KSA), has demonstrated its ability to operate quickly and efficiently while consuming little power. However, the Kogge Stone PPA design's space consumption could be an issue for specific applications.
Using DSP and VLSI-CMOS technology, we describe a Gate Diffusion Input Logic architecture for an area-efficient Kogge Stone Adder in this paper. This Kogge Stone Adder is created using pass transistor and CMOS logic, and its performance is compared to that of GDI logic in terms of size, power, and delay. By reducing the

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number of transistors, GDI also reduces the chip size, providing the designs an advantage over CMOS and PTL Logic. The Kogge Stone PPA's area consumption is intended to be decreased by the GDI Logic design while retaining its quick and effective operation.

II. LITERATURE REVIEW

A design and implementation of an area-power efficient hybrid parallel-prefix Ling adder was put forth by authors in [1]. In the hybrid adder architecture, even-indexed bits are handled by the Ladner-Fischer approach, whilst odd-indexed bits are handled by the Kogge-Stone structure. The most popular adder architecture is parallel-prefix because it enables a variety of design possibilities for achieving area, power, and delay efficiency as well as the ability to optimise trade-offs. Authors in [2] proposed a 32-bit design for a number of Parallel Prefix adders, and the performance results were compared in terms of area, latency, and power. The prefix computation, which can be used in a variety of applications, is one of the fundamental problems. The width of the circuit is assumed to be equal to the size of the input in the majority of suggested parallel prefix circuits. A family of parallel prefix circuits that work well when the input size 'n' is greater than the circuit width 'm' is introduced in this study [3]. In other words, when n>m, the suggested circuit's speed is almost optimum in these conditions. The most significant and effective circuit for binary addition has been invented, and it is called the Parallel Prefix Adder. They are particularly attractive for VLSI implementation due to their distinct structure and execution efficiency. The Kogge Stone Parallel Prefix Adders were introduced in this article by authors in [4] along with their design, performance, and implementation strategies. The various design methodologies used in this study included GDI (Gate Diffusion Input) and CMOS (Complementary Metal Oxide Semiconductor).

Ajith Ravindran et al.'s paper [5] compares and contrasts a hybrid 4-bit CMOS-based complete adder with a 4-bit Kogge stone adder. The Ripple Carry Adder, Carry Look Ahead Adder, Carry Select Adder, and Prefix Adder are high-performance adders that are more prone to mistakes than the Kogge Stone Adder. The Kogge stone adder is a more complex version of parallel prefix adders that also takes less time to construct due to its smaller component count. With the aid of the traditional Vedic mathematics. Authors in [6] created a revolutionary architecture for performing high-speed multiplication. The adder used to implement the paper is a Kogge stone adder, a popular adder in modern industries and a parallel prefix form of the carry look-ahead adder. As a result of producing the carry signal in O(logn) time, it is widely considered that the used adder is the fastest adder design available. In a work that was published by S. Daphni et al. [7], the design and analysis of numerous Parallel Prefix Adders (PPA) were described, along with a comparison of how well these adders performed in terms of area, delay, and power. The investigation's findings indicate that the Kogge stone adder (KSA), which automatically accelerates the addition process but requires more room and electricity, is preferred for the delay process. Amy Mariam George and colleagues [8] created a Parallel Prefix Radix 2 8-bit Comparator with Constant Delay (CD) for this work. Through a PMOS transistor with a critical path clock, the output of the constant delay logic is first pre-discharged to logic zero before switching to logic one. Dynamic logic cannot compete with CD logic's speed in its D-Q mode of operation. In this study [9], the authors examined the performance of a few parallel and conventional adders. This study also looked at the performance of the KSA, BKA, HCA, and HHCA. The main contribution of this research is the understanding of the structure and performance characteristics of the Parallel Prefix Adders. There are several different parallel prefix networks that are available, each with their own special features including the number of operators, depth, and allowed operator fanout. In this research, Mary Sheeran [10] combines search with functional programming approaches to provide a detailed investigation of parallel prefix network design. Networks are developed that perform better than the most well-known historical discoveries. An area-efficient Kogge Stone PPA that performs parallel arithmetic operations in CMOS systems is designed in this study by S. Daphni et al. [11], and the design is then evaluated based on factors like area and power individually. In the suggested area-efficient KSA design, the Pass Transistor Logic (PTL) was used to examine a device's performance. The performance results of PTL with PP-KSA design needed fewer MOS devices and utilised less space when compared to the fundamental 4-bit PP-KSA design. In this paper by Mineo Kaneko [12], along with its implementation in the structural optimisation of Parallel Prefix Adder using search techniques like the Simulated Annealing Algorithm, the minimal structural transformation of the Parallel Prefix Tree was proposed.

Dixit and Nagaria [13] compare four logic styles for low power design: conventional CMOS, Domino CMOS, Transmission Gate CMOS, and GDI. The authors conducted experiments using benchmark circuits and found that GDI logic consumes the least power, but has a higher delay than conventional CMOS and Domino CMOS. The paper concludes that designers can combine different logic styles to achieve optimal power consumption and delay in digital circuits. E. Haghparast et.al [14], presents a design methodology for combinational circuits based on

Gate Diffusion Input (GDI) logic. The authors provide a brief literature review that highlights the importance of low-power and high-speed design techniques for digital circuits, and the limitations of traditional CMOS logic in achieving these goals. They discuss the advantages of GDI logic, including its low-power consumption and high-speed operation, and review some previous works on GDI based circuit design. The authors also describe the limitations of previous GDI based designs and propose a new methodology that overcomes this limitation. Sheng-Lyang Jang et.al [15] presents a novel design methodology for combinational circuits based on GDI logic. The authors provide a literature review that emphasizes the importance of low-power design techniques for digital circuits, and the limitations of traditional CMOS logic in achieving these goals. They discuss previous works on low-power design techniques, such as voltage scaling and clock gating, and describe their limitations. The authors then introduce GDI logic as a promising alternative for low-power circuit design, and review some previous works on GDI-based circuit design. They also provide a detailed description of the GDI logic structure and its advantages over traditional CMOS logic. Finally, the authors present several experimental results that demonstrate the effectiveness of their GDI-based methodology for reducing power consumption in combinational circuits.

III. Design Of A Kogge Stone Adder Using Cmos Logic

Using CMOS logic and the Grey Cell-Black Cell (GC-BC) approach with AND and OR gates, a space-saving Kogge-Stone adder is created. The adder is divided into Grey Cells and Black Cells as part of the GC-BC method. Black Cells produce the ultimate carry signal, while Grey Cells produce the partial sums and propagate signals. In the GC-BC technique, the adder is divided into a number of stages, each containing a group of Grey Cells and Black Cell. The Grey Cells generate partial sums and propagate signals in the first half of each stage, while the Black Cell generates the final carry signal in the second half of each stage. The Grey Cells and black cells in this technique are composed of a combination of AND and OR gates. The AND gates are used to generate the propagate signals, while the OR gates are used to generate the partial sums. CMOS logic can be used to create an area-efficient Kogge-Stone adder by utilizing the GC-BC approach with AND and OR gates. A design that minimizes the amount of logic gates necessary while preserving the correct functionality is produced by combining AND and OR gates in the Grey Cells and the Black Cells, as well as a minimal connecting topology. Here each block is implemented using CMOS logic.

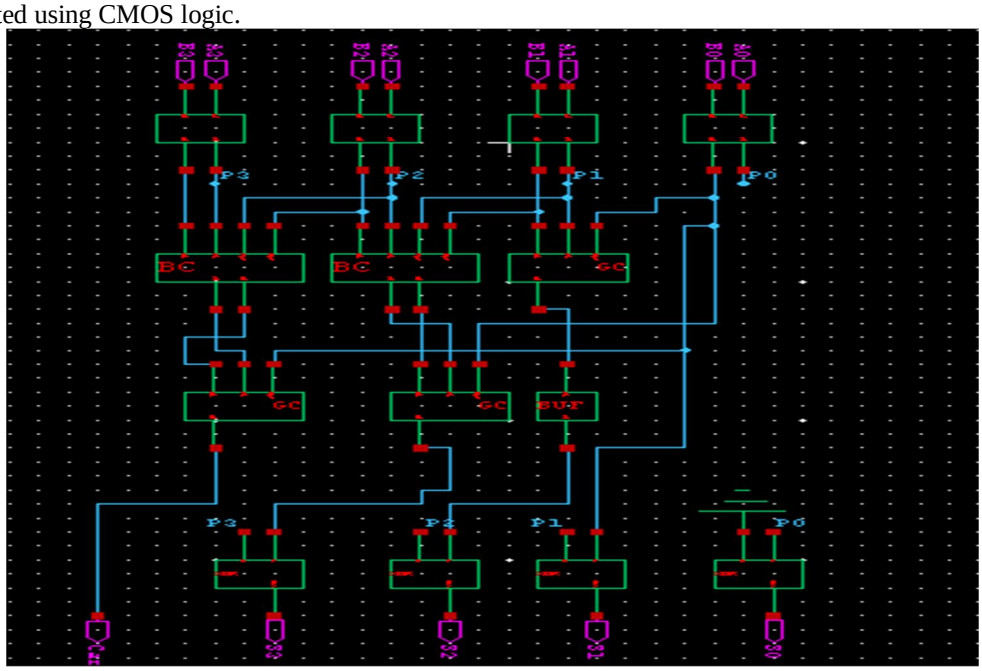
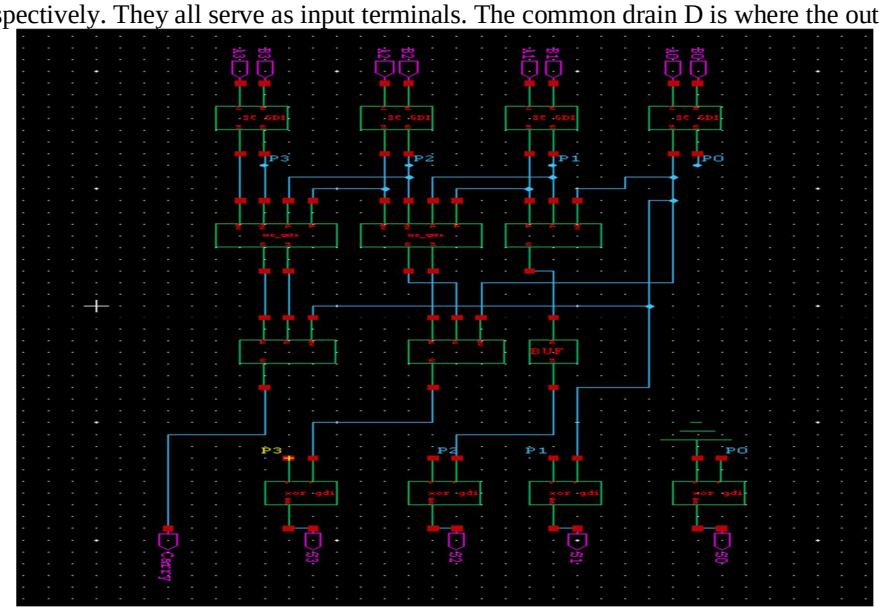


Figure 1. Schematic of KSA using using CMOS Logic

V. Design Of A Kogge Stone Adder Using Gate Diffusion Input Logic

The "gate diffusion input" (GDI) technology, a unique method for building circuits, considerably reduces the power requirements. The designs also have a benefit over conventional methods since GDI leads to fewer

transistors as well as a smaller chip area. An NMOS and a PMOS transistor are the only two components of a simple GDI cell. However, the swing problem with GDI method is a serious drawback. It occurs as a result of the NMOS and PMOS each producing a weak logic. This issue is resolved by making some adjustments to the current GDI method. It turns out that the modified GDI method is more effective than PTL and CMOS. Additionally, an XOR gate can be created using just 3 transistors utilizing the m-GDI approach. More than three transistors are utilized in the various traditional XOR gate configurations. 28 transistors are needed to create a CMOS complete adder. The CMOS implementation of the inverter circuit is comparable to the fundamental GDI primitive cell. But it's actually much more powerful than that. The functionality of the circuit changes depending on the inputs provided to G, N, and P. G is the NMOS and PMOS's shared gate. P and N are the source terminals for the NMOS and PMOS, respectively. They all serve as input terminals. The common drain D is where the output is gathered



VI. RESULT

Kogge Stone Adder implemented in CMOS logic, Pass Transistor logic and Gate Diffusion Logic are compared in terms of area, power and delay which is shown below in the table. As seen in the table, PTL performs better than CMOS logic when using existing designs in terms of area and power, although PTL has a longer delay. We came up with a new design leveraging GDI logic for that, and it is obvious that it uses lesser space and power than previous solutions. However, when GDI logic is compared to PTL, delay is decreased, but not when GDI logic is compared to CMOS logic. Even though CMOS logic has more transistors than other types of logic, it appears to have a higher delay in this instance even though it actually has the lowest delay. The performance of a digital circuit is influenced by many factors, including the number of transistors used, the circuit topology, and the layout design. While it is generally true that adding more transistors in a CMOS logic circuit can increase delay, this is not always the case. In some cases, the use of additional transistors can actually help reduce delay by improving the circuit's overall performance. This is because more transistors can be used to optimize the circuit for specific performance parameters, such as power consumption, area, and speed.

TABLE I. COMPARATIVE ANALYSIS TABLE

TYPES OF LOGICS USED	POWER	DELAY	AREA (NO OF TRANSISTORS)
CMOS LOGIC	5.721033×10^{-4} watts	-6.1436×10^{-10} s	196
PTL	4.320054×10^{-4} watts	9.5534×10^{-9} s	116
GDI LOGIC	9.675×10^{-5} watts	6.6645×10^{-10} s	79

It is also possible to access the kogge Stone Adder's output waveform, which was created utilizing CMOS, Pass Transistor, and Gate Diffusion Input logic. All of this indicates that the Kogge Stone Adder, when used with Gate Diffusion Logic, is both area and power efficient.

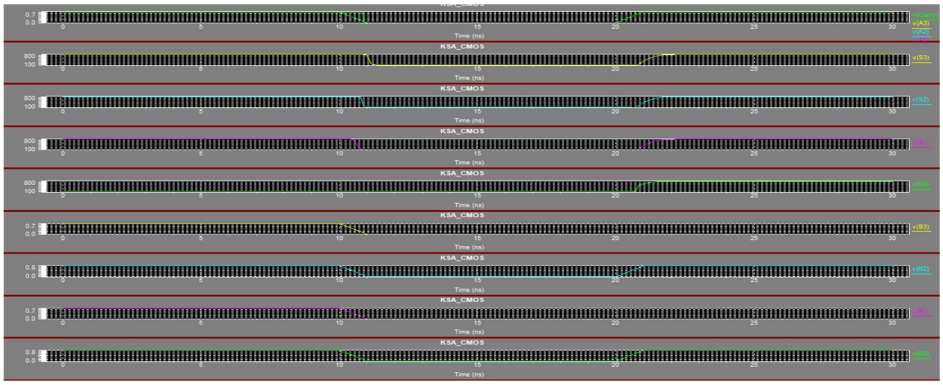


Figure 4. Output Waveform of KSA in CMOS Logic

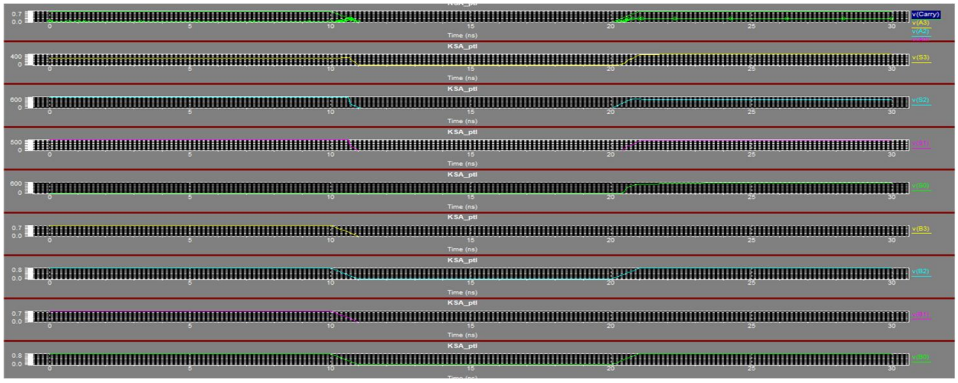


Figure 5. Output Waveform of KSA in PTL

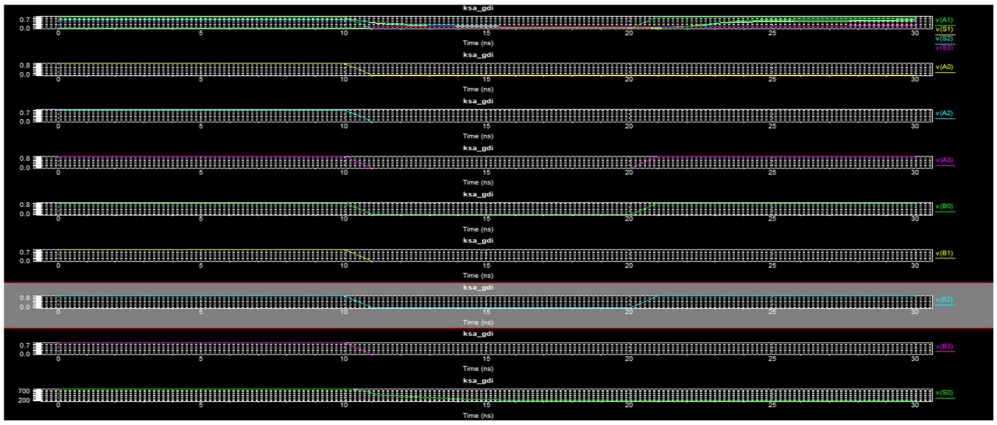


Figure 6. Output Waveform of KSA in GDI Logic

VII. CONCLUSION

Finally, compared to PTL and CMOS logics, the suggested architecture of the space and power-efficient Kogge Stone adder employing GDI logic offers a number of advantages. The use of GDI logic produces a more straightforward architecture with fewer transistors, which reduces the amount of power used and the amount of space needed. The GDI logic also enables simple scaling and enhanced noise immunity. A high-performance parallel adder known as the Kogge Stone adder is widely utilized in applications for digital

signal processing and computation. The suggested architecture offers a practical method for implementing Kogge Stone adders, with enhanced functionality and lower power usage. Microprocessors, high-speed communication systems, and digital signal processing are only a few of the potential uses for this architecture. Overall, the GDI logic-based suggested architecture is a promising strategy for creating effective and reliable Kogge Stone adders.

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