

Design and Implementation of LVCMOS18 I/O Buffer

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Abstract— The VLSI integration technology is growing at a rapid rate. As a result, there is a need for smart devices with high performance operation. This plays a vital role in the consumer industry at larger scale in day-to-day life. To enhance performance of the new devices, more robust interfacing standards are required. Hence, the proposed paper discusses the design of the I/O standard LVCMOS18 buffer with 0.9V interface at the transmitter with an operating frequency of 150 MHz. The interface I/O design uses 90nm GPDK technology and is tested with various process corners with 4 mA current drive capability. The results obtained are found to be encouraging for all the design specifications of LVCMOS 18 I/O standard for the transmitter.

Index Terms— LVCMOS18, transmitter, driver, level up shifter, Schmitt trigger, level down shifter and ESD protection.

I. INTRODUCTION

A vast majority of innovations in the communication field are happening to make user life more comfortable. Simultaneously, there is fast growth in an integration technology which enables the smart gadgets to be reachable to all parts of the world. The development of System-on-Chip (SoC) and Network-on-Chip(NoC) integration technologies have created significant changes in consumer electronics field. We can also witness the tremendous growth happening in the field of AI, ML and IoT technologies. To be in pace with current trends, the standard matching compatibility issues need to be addressed. In this aspect, the input/output (I/O) device interfacing is a major concern in terms of signal integrity and voltage level standards. Interfacing is the way of establishing link between two devices, allowing the designer to adapt the input and output configurations of both devices so that devices can work together. Input/output devices enable the communication between systems. This may be in the form of chip with external world. They are connected on the periphery of the chip with matching interfacing standards. The processing speed and efficiency of internal circuitry grows as it processes the data faster, to communicate effectively to the external world matching I/O circuits are required. As semiconductor technology has being advanced, Low Voltage Complementary MOS transistor(LVCMOS) power supply voltage and interfacing standards for effective use are defined by Joint Electron Device Engineering Council(JEDEC)[1] for digital logic with operating voltage less than 5V. LVTTTL and LVCMOS offer compatible voltage standards like V_{IL}/V_{IH} , V_{OL}/V_{OH} and current drive strength for effective interfacing.

II. LITERATURE REVIEW

The dynamic power reduction of LVCMOS based ALU [2] is designed and verified for reduction for 30% power and 27% current drive strength. The energy efficient frequency meter with different LVCMOS I/O standards[3] is designed by considering current drive strength of 2mA. The power dissipation of different LVCMOS standards are

investigated with different frequency ranges. FPGA implementation of low-power ROM is designed with matching LVC MOS standards [4]. The results obtained showed the ROM designed with LVC MOS12 consumes less power compared to LVC MOS33. The authors report of low power ROM design that is compatible to be used with i7 processor. An energy and power-efficient D flip-flop is designed for FPGA in [5] by considering different LVC MOS standards. The design is implemented with frequency scaling and I/O scaling techniques. An optimal result on D flip-flop design with low frequency ranges is indicated. The processor specific comparator [6] is designed based on LVC MOS standards. The power consumption of comparator with LVC MOS12 standard for 2 GHz operating frequency was found less when compared to the comparator design of other LVC MOS standards. LVC MOS based designs are implemented for most of domain-specific applications. Energy-efficient Sindhi language Unicode reader [7] based on LVC MOS standards is implemented on 28nm based FPGA for natural language processing. The new ultra-level shifter is designed [8] for high-speed and wide-band applications. The voltage-based energy-efficient mobile charge sensor [9] is designed and tested with different LVC MOS standard configurations for verifying power consumption. It is found that power consumption is minimum with LVC MOS15 standards. Many different level shifter architectures based on the voltage specifications are reported in [10]. The high voltage tolerant level shifter design is reported in [11-13] for the buck converter operation. In the paper reported in [14], the LVC MOS I/O standard in FPGA is implemented for energy efficient processor. The implementation with corresponding low voltage operates at 1×106 MHz device operating frequency. The paper reports 67.42% reduction in clock power and 75.99% reduction in IO power. With 90nm CMOS process, a new level-up shifter [15] is reported. Aravind Anant Bhat et. al. have reported the design of low-voltage CMOS 3.3V I/O interfaces for electronic circuits operating at 3.3 volts [15]. The authors present a detailed analysis of the design requirements and challenges of low voltage CMOS I/Os for various applications. The paper highlights importance of low-voltage CMOS I/Os for reduced power consumption.

The work in [16] describes the design of Low voltage CMOS 3.3V I/O. The resources [17-20] are used for consolidating the technical specifications of LVC MOS 18 I/O standard. The resource [21] briefs on LVC MOS buffers providing single ended IO interface to the external devices in system on chip (SoC) designs. This paper covers functional operations of basic blocks of the LVC MOS output buffer and input buffer in detail and the design considerations and challenges at each phase of the design. The paper [22] reports a 4-bit register is designed using Xilinx ISE design suite 14.2. The LVC MOS I/O standard is used here in achieving the goal of minimum power dissipation. The scaling is done for the frequencies 1 Ghz, 2 Ghz, 3 Ghz, 4 Ghz and 5 GHz. Another significant work [23] reports of an energy and power efficient Data flip-flop on FPGA with LVC MOS IO standard. Two energy and power efficient techniques like Frequency Scaling and IO standard scaling have been implemented. As the semiconductor industry is achieving rapid growth in technology, the reduction in the sizes of transistors and supply voltage are the key issues. This in turn is applicable to the design of I/O buffers like LVTTTL and LVC MOS migration with changing trends. The proposed paper describes the design of LVC MOS18 transmitter buffer which works at a data rate of 150 MHz with current driving capacity of 4 mA. The proposed work includes the design of LVC MOS18 I/O buffer at the transmitter side and it is verified for worst PVT case conditions. The required specifications of proposed system are as indicated in Table I.

TABLE I. SPECIFICATIONS OF PROPOSED LVC MOS 18 I/O ON THE TRANSMITTER

Parameter	Description	Min	Typ	Max	Units
VDDO	IO supply	1.62	1.8	1.98	V
VDD	Core supply	0.81	0.9	0.99	V
Temp	Temperature	-40	25	125	deg C
Frequency	Data frequency			150	MHz
VOH	Output High Voltage	$0.75 \times VDDO$			V
VOL	Output Low Voltage			$0.25 \times VDDO$	V
IOH	Output High Current	4			mA
IOL	Output Low Current	4			mA
Rpup, Rpdn	Weak Pullup and Pulldn resistor	10k			K Ohm
Ileak	Supply leakage			Measured	uA
Ioz	Pad leakage			Measured	uA
Tr, Tf	Output Rise time, Fall time			0.3	ns

T_{plh}, T_{ppl}	Output Rise delay, Fall delay			1	ns
Duty Cycle	Output Duty cycle	45		55	%
C_{load} (Tx)	Tx load capacitance			10	pF
T_r, T_f	Input slew to Tx			100	ps
Supply ramp rate				100	mV/us

III. METHODOLOGY

The block diagram of LVC MOS18 I/O buffer is shown in Fig.1. It shows that the proposed device is connected to transmitter and receiver blocks as I/O interfacing support. The transmitter block is connected to internal circuit which acts as input end with pad acting as an output end. For receiver block, pad is the input and the output of receiver is connected to internal circuit.

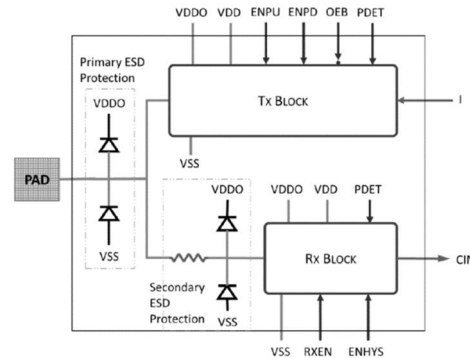


Figure 1. Main block diagram of LVC MOS18 I/O buffer

The I/O has primary and secondary ESD protection to protect the circuits from ESD events which occur during normal operations and during lifetime. The primary circuit provides ESD protection to transmitter block. The secondary circuit along with the primary circuit provides ESD protection to the receiver block. Some of the I/O pins of the transmitter and receiver will be power supply connections as shown in the Fig.1. Other pins PDET, RXEN, ENHYS of receiver and ENPU, ENPD, OEB and PDET of the transmitter are active-high signals that are enabled as per the requirement of transmitter or receiver switching ON mode. PDET is common signal for both transmitter and receiver blocks and it is kept high for either working for transmitter and receiver mode ON. The transmitter block consists of level-shifter, pre-driver, driver and control blocks. In the transmitter, the signal from the core is connected to level shifter where signal level conversion takes place. Later, it is fed to pre-driver and driver blocks to enhance the signal level. All the operations of the transmitter block are controlled by control block. The block diagram of transmitter is shown in Fig.2.

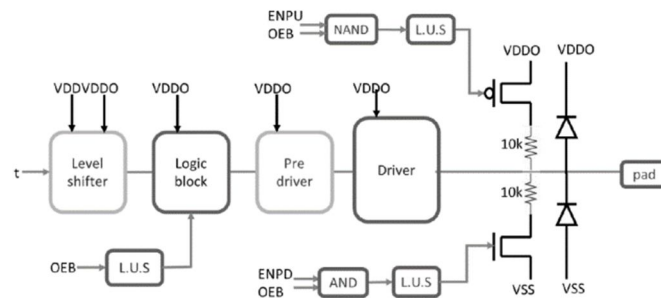


Figure 2. Block diagram of the transmitter

The supply pins are indicated as VDDO, VDD and VSS. OEB is active-low pin used to turn ON or OFF the transmitter block. 'I' is the input pin of transmitter. ENPU, ENPD pins are active-high pins used for forcing the pad to some voltage when transmitter is OFF. Pad acts as output of the transmitter.

One of the main blocks of the transmitter is level shifter. The input signal from the core is sent to level shifter, where the signal voltage level conversion take place. Later, it is passed to the logic block and then the signal is

further strengthened by pre-driver and driver blocks. The enhanced signal is transmitted from the transmitter. Looking into the design specifications of Table I, the schematic diagram of Contention mitigated level shifter is proposed. The same design is shown in Fig.4 on the next page. It has two supply voltages, one for each side (VDD, VDDO). VDD is connected to same voltage supply for the source of the input single ended signal, and VDDO is connected to the I/O supply of the device.

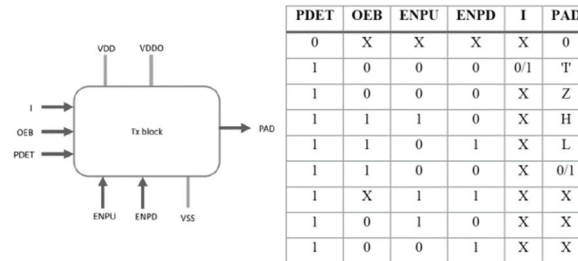


Figure 3. Pin diagram of Transmitter block with pin details

The next blocks of LVCMOS18 I/O are pre-driver and driver blocks. The pre-driver interfaces the small core logic circuit to the large capacitances. It includes the gate capacitance and the parasitic capacitance of the driver's metal route. Pre-driver must be able to drive the large capacitance in the driver transistors. The level-shifter input is fed to the pre-driver circuit.

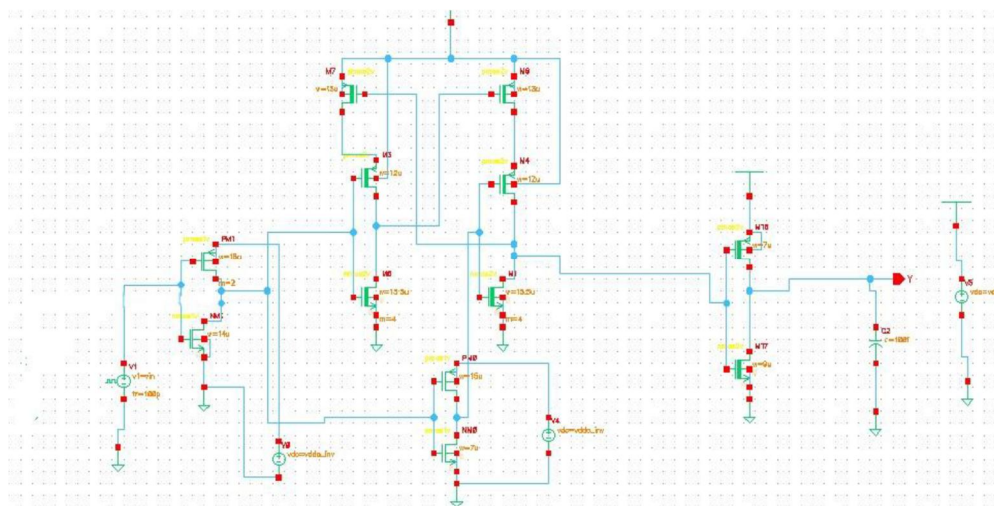


Figure 4. Schematic diagram of level shifter

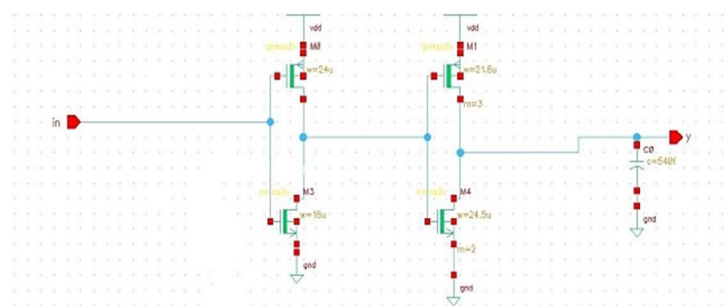


Figure 5. Schematic diagram of PMOS pre-driver

The design of PMOS pre-driver and NMOS pre-driver are considered with determination of load capacitance, input capacitance and number of stages required. The schematic diagram of PMOS pre-driver is shown in Fig.5. Both the pre-driver and driver blocks are used to enhance the signal level. Hence the driver stage schematic is shown in Fig.6.

The driver circuit is designed to drive a load capacitance with 4mA current driving strength. The specifications of LVCMOS18 I/O buffer are satisfied by varying width parameter of transistor keeping length parameter as gpdk 90nm with worst case corner analysis.

The control logic is implemented depending of signal drive capacity for pre-drivers and driver. The logic implementation of the control logic is shown in Fig.7 and Fig.8, and the logic conditions are as listed in the Table II and Table III.

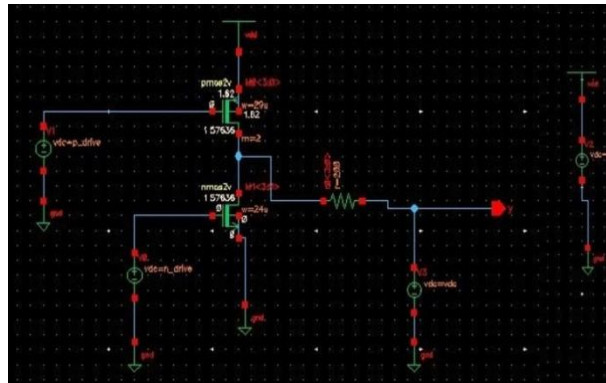


Figure 6. Schematic diagram of driver circuit

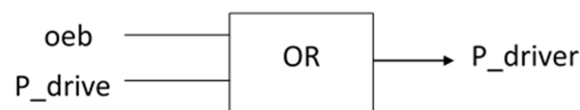


Figure 7. Block diagram of p-pre-driver control block

TABLE II. TRUTH TABLE FOR PMOS PRE-DRIVERS

oeb	P_drive	P_driver	P_driver state
0	0	0	ON
0	1	1	OFF
1	0	1	OFF
1	1	1	OFF

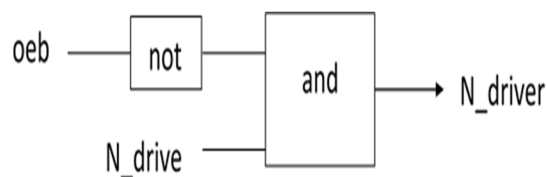


Figure 8. Block diagram of n-pre-driver control block

TABLE III. TRUTH TABLE FOR NMOS PRE-DRIVER

oeb	N_drive	N_driver	N_driver state
0	0	0	OFF
0	1	1	ON
1	0	0	OFF
1	1	0	OFF

The contention mitigated level shifter results are shown in Fig.9. It is designed to provide the VDD and VDDO as per the requirement of core and I/O processing. The subsequent blocks in the LVCMOS 18 I/O transmitter are pre-

driver and driver, which enhances the signal level by matching with large capacitance load and current driving capability.

- The design of PMOS pre-driver stage implementation is considered with design parameters: $C_{ggpmos}=C_{out}=540fF$, $C_{in}=24fF$, $N=\ln(C_{out}/C_{in})=3.11$ with increasing factor $A=(C_{out}/C_{in})^{1/N}=2.72$.
- According to the specifications given the driver should be able to drive at least 4mA in the worst Process Voltage Temperature (PVT) corner (slow, 1.62 V and 125°C).

So, the design of driver block and the implementation is listed as:

- Width W, is the only variable since all other quantities are either fixed for a particular PDK or fixed for design experiment.
- Providing the worst-case corner inputs, the width is varied until the driver is able to source 4mA of current at the worst operating condition, starting from least possible width for the technology.

Taking these and ESD guidelines into consideration, a 200 ohms resistor is connected at the output.

Width is adjusted to get 1mA current and 4 such slices are instantiated to meet the specification of 4mA. A current in worst cases.

III. RESULTS AND DISCUSSION

Level up shifter schematic which converts the core voltage of 0.9V to 1.8V of I/O domain is one of the main blocks of LVCMOS18 transmitter, implemented using Virtuoso Cadence software as per the specifications listed in Table I. The simulation result obtained are shown in Fig.9.

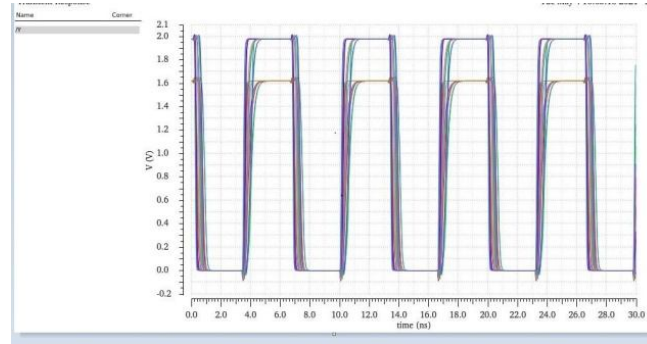


Figure 9. Simulation Results of contention mitigated level up shifter

The transient and DC response of driver block results are tabulated in Table IV and Table V.

TABLE IV. TRANSIENT RESPONSE OF DRIVER BLOCK

Design Parameters	Measured	
	Minimum Value	Maximum Value
DC	48.98mV	51.9mV
T_r	90.71pS	340.5pS
T_f	86.39pS	246pS
T_{PHL}	127.6pS	366.3pS
T_{PLH}	122.8pS	414.pS

TABLE V. DC RESPONSE OF DRIVER BLOCK

Design Parameters	Given specifications	Minimum	Maximum
I_{OH}	>4mA	4.243mA	7.253mA
I_{OL}	>4mA	4.276mA	7.223mA

The design of 3-stage PMOS driver schematic is verified with an output load capacitance of 540fF and input capacitance of 24fF. The results obtained with transient analysis are matching with specifications listed in the Table I. Similarly, the driver block schematic is designed to drive large load capacitance with current drive strength of >4mA. The DC analysis results shown in Table IV are matched with the given specifications with worst case process corner(PVT) analysis. The findings of power dissipation results of the proposed block are 22% better than the [3] for 4mA operation of LVCMOS18I/O.

IV. CONCLUSION

The LVCMOS18 I/O buffer is designed to work at the data rate of 150 MHz. The driver in the transmitter block is designed to drive 4 mA of current even in the worst-case conditions. The working and implementation of Contention mitigated Level up shifter is understood and analysed for all the PVT process corners. The level up shifter effectively shifts the core domain voltage to IO domain voltage level. Similarly, the required pre-driver and driver designs with PMOS and NMOS buffers for capacitive load driving capabilities are understood and designed. The results obtained are found to be satisfactory as per the specifications. LVCMOS18 I/O is designed to work with microcontrollers, microprocessors, memory devices etc., with low voltage for highly computational digital processing operations. Recently, it is found that LVCMOS18 is being used in IoT enabled applications, industrial control systems and automotive electronics domain specific appliances to name a few. The future scope may include the enhanced usage of LVCMOS 18 I/O as an interfacing standard that finds vital role in the development of IoT devices, AI accelerated architectures and quantum computing devices etc.

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