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Design of Three Super Compact 5G Band Pass Filters with Integrated Passive Device Technology for 802.11a Wireless LAN

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***Abstract*—A highly miniaturized low loss Si integrated passive device (IPD) based 5G band pass filter (BPF) design is presented in this paper. Three multilayer (ML) square spiral inductors and a square spiral capacitor are designed and simulated. The constant width, variable width and a novel double split inductors possess maximum quality factors of 19.258, 20.852 and 25.353 and self-resonating frequencies of at 9.4, 9.2 and 12.9 GHz respectively. The simulated capacitor has capacitance of 0.352, 0.403 and 0.385 pF and Q value of 32.82, 25.09 and 28.21 at the respective center frequency of each BPF. The three LC resonant BPFs simulated using above ML inductors and capacitor have yielded bandwidths of 1200, 950 and 800 MHz respectively at respective center frequencies of 4.9, 5.5 and 5.25 GHz. The three filters have shown good return loss of -19.8, -27.5 and -30.96 dB respectively. Also they have produced excellent insertion loss of -0.67, -0.49 and -0.37dB. BPF designed employing the double split inductor gave 0.3113 dB (53%) lower insertion loss and 11.2 dB (156%) lower return loss, compared to constant width inductor BPF. The double split inductor BPF showed 0.1369 dB (72%) lower insertion loss and 3.41 dB (112%) less return loss, against the variable width spiral inductor BPF. All the three filters are designed with same on chip occupied area of only 0.068 mm^2. The filter models are simulated in HFSS, as per the physical parameters obtained. We found that it has least occupied area against the reported bandpass filters under reference. These simulation results clearly indicate that the developed bandpass filters possess excellent responses that will surely satisfy the sub-6GHz band 5G WLAN access applications.**

***Index Terms*— Double Split Inductor, Insertion Loss, Return Loss, Quality factor, On Chip Area.**

I. INTRODUCTION

Global data explosion due to availability of low cost high speed and best quality smart devices enforced an extraordinary demand for affordable ultra speed multimedia networking with higher service quality. High-speed 5G wireless local area network (WLAN) standards like IEEE 802.11a (UNII) band WLAN/ ETSI HIPERLAN2 (5.15-5.825 GHz); RFID (4.9-5.8GHz); ISM (5.2-5.35 GHz); WiMAX IEEE 802.16 (4.5 – 5.97 GHz) are emerging worldwide to satisfy above requirements [1]. Researchers face big challenges to develop integrated single chip wireless radio-frequency IC (RFIC) transceiver designs that easily support 5G communications [2]. Low-cost integration has driven the radio front end electronics (RFFE) to use silicon CMOS technologies that can offer high quality factors at 5G frequencies. Hard to design onchip BPF is the most critical component that

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strongly influences a wireless transceiver performance. Minimum insertion loss and high selectivity coupled with smallest onchip area, pose big challenging task for onchip bandpass filter (BPF) designs [18]. Hence a big demand for small size low loss integrated passive inductors and capacitors to realize high performance compact onchip BPF in an RFIC.

IPD technology is successfully employed to realize high performing miniature passive inductors, capacitors, and LC BPF designs on silicon CMOS RFICs. Easier dicing, enhanced thermal conductivity and thinning options (< 10 mils) are promising benefits of Silicon IPD process [13]. It permits easier component integration with smaller footprints, smaller power, and flexible bandwidths. Spiral inductors and capacitors became most successful silicon IPD passive components. In fact, they occupy major proportion of RFIC chip area (60-70%). In recent past, passive IPD based BPF and LNA circuits are being fabricated as CMOS ICs, co-located as a system in package (SIP) [18].

A 5.5 GHz single chip IEEE WLAN BPF developed by Iason Vassiliou et al., showed higher S_{11} of -12dB and a large chip area of 18 mm^2 [1]. A 5.5 GHz RFIC fabricated by A. Italia et al., showed Q value of 10 and higher S_{11} of -12.2 dB and high area of 4.84 mm^2 [2]. Sanduleanu reported a 6 GHz CMOS RFFE BPF with Q value of 7.05, poor return loss of -10 dB and larger chip area of 1.05 mm^2 [3]. A 6 GHz glass IPD BPF from C.H. Chen et al had a higher S_{11} of -18 dB and large 0.9 mm^2 area [4]. The 5.2 GHz Al_2O_3 resonator BPF from Chia et al. had poor insertion loss of -2.5 dB, small Q of 1.82 and large area of 0.55 mm^2 [5]. A Multiband BPF from M. A. Abdalla reported excellent S_{11} of -50 dB, but it occupied colossal onchip area of 3000 mm^2 [6]. A microstrip UWB BPF from Ruifang Su had excellent Q of 71, but it occupied very huge area of 73.9 mm^2 [7]. The 180 nm CMOS 40 GHz BPF from Nagesh Deevi possessed good Q of 12.5 and lowest onchip area of 0.0256 mm^2, but showed large S_{12} of -2.1 dB [8]. A super compact Si IPD BPF reported by Nan Li et al, had good S_{11} of -15 dB but poor S_{12} of -2.0 dB and a large area of 0.5 mm^2 [9]. Compact passive BPFs at higher frequencies are developed with LTCC technology, but suffer from heat and larger size problems [5]. A multilayered quad-band BPF reported by Yung-Wei Chen had very good Q of 25, S_{11} of -28 dB, but occupied very huge area of 545 mm^2 [10]. A 2.5 GHz Si IPD LC BPF from Chongchong Mao has good S_{11} of -18 dB but occupied large area of 7.5 mm^2 [11]. Ki-Hun Lee implemented a 2 GHz GaAs IPD BPF with very good S_{11} of -26.8 dB, but with large 7.84 mm^2 area [12]. Ki R. Shin had developed a 3.6 GHz Si IPD 5G NR n78 BPF with good Q of 7.2 and very good S_{11} of -26 dB, but poor S_{12} of -1.8 dB and large area of 1.28 mm^2 [13]. Md. Jamil Uddin reported a 90nm CMOS active inductor 21 GHz BPF with least occupied area of only 0.0013 mm^2, but it had smaller Q of 4.16[14]. Yang Chen produced a compact 1.8–3.0 GHz GaAs IPD BPF with excellent S_{11} of -33 dB but it suffers from poor S_{12} of -3 dB and large area of 2.86 mm^2 [15]. A compact 4.9 GHz UWB BPF from Parchin et al., had excellent S_{11} of -30 dB, but it suffered poor S_{12} of -1.5 dB and also very huge chip area of 225 mm^2 [16]. The 4.15 GHz VSDR LTCC Filter from Liangfan Zhu showed an excellent S_{11} of -43 dB and very good S_{12} of -0.5 dB but occupied very large area of 29.4 mm^2 [17]. V.R. Machavaram and B.R. Nistala, produced a 5.1 GHz 5G WLAN BPF with excellent S_{11} of -25.6 dB, very good S_{12} of -0.432 dB and least chip area of 0.16 mm^2. But it had smaller Q value of 3.65 only [18]. A 3.75 GHz Si HRS IPD BPF by Xiaomei Li et al, reported very good S_{11} of -35.65 dB but large insertion loss of -1.52 dB and large area of 2.5 mm^2 [19].

Like many of above authors, we optimized the filter parameters to yield significant performance improvements over the above filters. In this paper, three IPD miniaturized LC resonator BPFs are designed and simulated using RF design software HFSS. Their performance is compared with above results to prove the improvements obtained. We achieved the least possible layout size of 0.012 mm2 for simulated BPFs, an ideal size for smart mobile devices that require high degree of miniaturization and minimal losses. Section II illustrates the design and development of three multilayer spiral inductors and a spiral capacitor. It also explains the simulation of three bandpass filters using above passive components along with s parameters explained. The performance comparison of our filters with earlier reported BPF results is discussed. Section III presents the conclusions and further discussion.

II. Design of Band Pass Filters

This paper narrates the design and simulation of three super compact BPFs for 5G WLAN standards in the 5 GHz license exempt band. Multi-layer passive reactive components are designed and simulated in high frequency simulation software (HFSS). Hybrid lumped element model analysis is carried out to simulate good performing series LC BPF designs. Rectangular spiral geometry simplifies the fabrication complexity along with uniform current density. Hence this shape is employed to design both the inductors and capacitor for developing the BPFs. Device geometry parameters are traded with process parameters to develop low loss and yet super compact BPFs.

A. Multilayer Onchip Spiral Inductors

Most RFIC fabrication processes are employing multilayer structures with easier integration capabilities utilizing popular IPD technology. So we propose a novel 3-Dimensional series stacked structure with full CMOS compatibility for all the three ML inductors. Placement of non-orthogonal metal layers with parallel conductor geometry enhances inductance and
Q values yet possessing minimal proximity effects and parasitic capacitances. 3D inductors need fewer turns for given inductance. Fewer turns not only reduce inductor size but also help reduction of substrate related losses, which further enhances Q value of 3D structures. A 300 μm thick silicon substrate layer and 12 μm thin oxide layer are chosen to reduce losses, which increased the operating frequency and also the Q-factor. Series stacked multiple turn spiral inductor structure geometry shown in Fig. 1 will have high inductance of 1-10 nH and Q around 10.

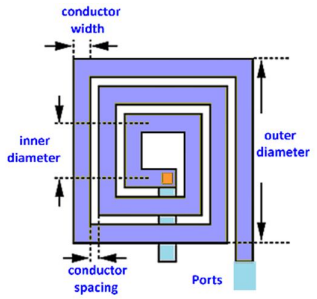


Fig. 1. Typical View of the Spiral Structure of a Passive Onchip Inductor

Higher inductance values are mainly due to the self-inductance as well the associated mutual inductances between the individual sides (segment) of the inductor. The ratio of outer to inner diameter is chosen as 1:5 for high to enhance the quality factor and inductance at higher frequencies Overall inductance of spiral is given by standard expression

$$L_{Total} = L_{Self} + \sum M_{+ve} + \sum M_{-ve} \qquad (1)$$

The inductance of rectangular spiral is extracted using modified Wheeler's formula, using Eq. 1. The Q value of inductor is evaluated from Eq. 2.

$$Q = \frac{\omega L_s}{R_s} \frac{1}{1+\frac{R_s}{R_p}\left\{\left(\frac{\omega L_s}{R_s}\right)^2+1\right\}} \left[1 - \frac{R_s^2(C_s+C_p)}{L_s} - \omega^2 L_s(C_s + C_p)\right] \qquad (2)$$

Series stacked inductor structure is employed for developing multilayer inductors. ML inductors have very high self-inductance and mutual inductance due to presence of vertical and lateral conductor coupling. The upper layers are protected from the substrate losses and effects as the lowermost metal layer acts as a shield to them and hence the same inductance of planar structure is achieved with lesser area in stacked inductor. These three inductors are designed with 3 conductor turns per each layer.
The first ML spiral inductor (Constant Width Inductor) designed has constant width of 10 μm for all the turns in each layer. The spacing between each conductor path is 2 μm. Conductor thickness is 2 μm. The inductor has 3 turns per each layer. The inner and outer diameters are 61 μm and 180 μm. Onchip area occupied is just 180 μm x180 μm (0.0324 μm^2) excluding the ports.
The second ML spiral inductor (Variable Width Inductor) designed has different width for all the turns in each layer. The outer conductor run has same width of 10 μm like the constant width inductor. As we turn the spiral inside, the outer conductor turn has 10 μm width. However the width is gradually increased for the two inner turns by 2 μm size. The middle turn has 12 μm width while the inner most turn has widths of 14 μm. The spacing between each conductor path is 2 μm. Conductor thickness is 2 μm. The inductor has 3 turns per each layer. The inner and outer diameters are 57 μm and 180 μm. Onchip area occupied is 180 μm x180 μm (0.0324 μm^2) excluding the ports.
The third ML spiral inductor (Double Split Inductor) designed has same overall width for all the turns in each layer. Similarly the 10 μm width of every spiral turn of constant width inductor is separated into two individual

tracks with a width of 3.25 µm each separated by a spacing of 1.5 µm. Conductor thickness is 2 µm. The inner and outer diameters are 61 µm and 180 µm. Onchip area occupied is 180 µm x180 µm (0.0324 μm^2) excluding the ports.

The geometrical dimensions of all the three inductors are optimized to result in greater inductance vales for each. This further enhanced the filter selectivity and loss characteristics. The L and Q values of these simulated inductors were found from the obtained S parameters via Y parameters employing following standard expressions.

$$Q = \frac{Im\,[Y_{11}]}{Re\,[Y_{11}]} \qquad (3)$$

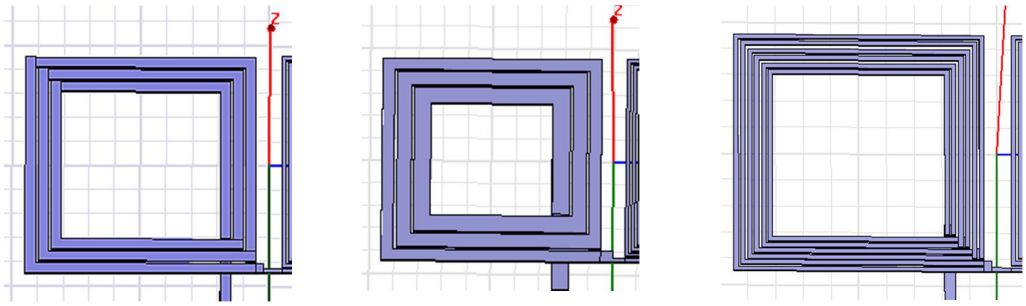
$$L = \frac{-1}{2\pi f\{Im\,[Y_{11}]\}} \qquad (4)$$

To verify the proposed modeling, three multilayer inductors are designed. The top view of geometrical structure for the three inductors is depicted in Fig. 2 shown below. The constant width, width variation and double splitting of each conductor turn into two separate tracks with in between spacing are reflected in this Fig. 2.

The layout dimensions and electrical parameters obtained for the three inductors are shown below in Table-I. These results indicate a clear possibility of geometry optimization, which simultaneously improved the quality factor, inductance and area efficiency significantly.

TABLE I. INDUCTOR'S GEOMETRICAL AND ELECTRICAL PARAMETERS UNDER SIMULATION

Inductor Capacitor	Conductor Width, µm	Spacing µm	Thickness µm	Number of Turns	L, nH ; C, pF @ 5.25GHz	Q_{max}	On Chip Area, μm^2
Constant Width L	10 - 10 - 10	2	2	3	3.891	19.2577	180x180
Variable Width L	10 - 12 - 14	2	2	3	4.052	20.8516	180x180
Double Split L	3.25 -_1.5 -_3.25	2	2	3	3.458	25.3532	180x180
Constant Width Capacitor	3	2	2	3	0.385	495	180x180



Constant width L Variable Width L Double Split L

Fig. 2 Layout Structure of 3 Multilayer Square Spiral Inductors

Variation of inductance for each ML inductor is compared in the following Fig. 3. The double split structure has extended resonant frequency above 12 GHz. Variation of Q factor for each ML inductor is compared in the following Fig. 4 below. Double split inductor exhibited highest Q value of 25.3532. The constant width, variable width and a novel double split inductors possess maximum quality factors of 19.258, 20.852 and 25.353 with self-resonating frequencies (SRF) of 9.4, 9.2 and 12.9 GHz respectively. They exhibited inductance of 3.38, 3.45 and 2.86 nH respectively at 3.4 GHz. At the center frequency 5.25 GHz of BPF, these inductors showed inductance values of 3.9, 4.05 and 3.45 nH respectively. These results have indicated that the three inductors designed here, will surely meet the requirements of 5G lower band (sub-6GHz) requirements due to their high Q and lowest occupied chip space.

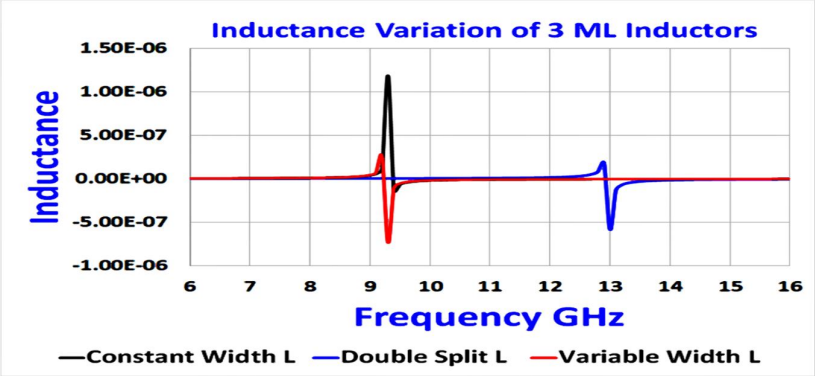


Fig. 3 Comparison of the Inductances of three Multilayer Inductors

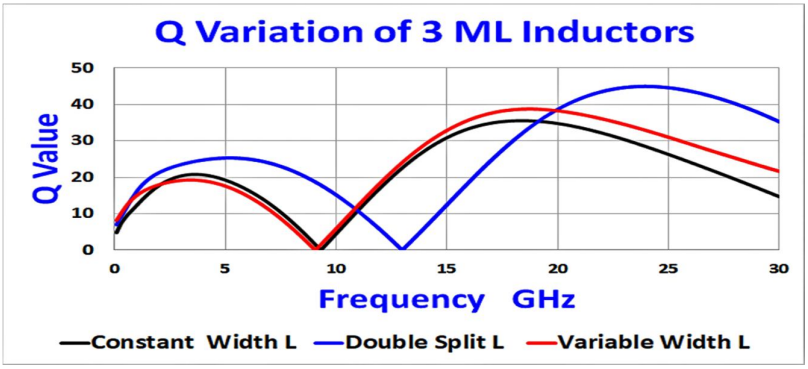


Fig. 4 Comparison of the Q values for three Multilayer spiral Inductors

B. On chip Square Spiral Capacitor

In this work, the design and simulation of a single layer square spiral capacitor in HFSS is presented. The copper conductor material and substrate silicon materials enhanced its performance for getting high performance 5G LC BPF. All the 3 turns are placed in one layer with a constant conductor width of 3 µm as given in Table-I above. The spacing between each conductor path is 2 µm. Conductor thickness is 2 µm. This capacitor occupied lowest chip space of only 180 x 180 μm^2. The conductor dimensions, utilized materials influences the capacitance value. Like the inductor, the quality factor and capacitance values are extracted from the simulated S parameters from following expressions.

$$C = \frac{-Imaginary\,[Y_{21}]}{\omega} \qquad (5)$$

$$Q = \frac{Imaginary\,[Y_{11}]}{Real\,[Y_{11}]} \qquad (6)$$

The capacitor HFSS simulation showed capacitance of 0.385 pF and higher Q value of 28.21 in 4.8 to 5.6 GHz passband. Its self-resonant frequency (SRF) is located at 10.3 GHz. The variations of capacitance and Q value with frequency are shown in the following Fig. 5. This square spiral capacitor simulated on 180 nm CMOS technology had reflected significant enhancement in the quality factor Q of filters developed in present work.

C. Onchip Bandpass Filters

The simulated BPF is modeled with series LC configuration cascading the three ML inductors and the spiral capacitor. Under simulation, the designed components will replace the L and C circuit components. HFSS software tool is used to simulate the three filters. It has been verified that the component values are stable throughout the pass bands. The structures of the three series LC filters using constant width, variable width and

double split spiral inductors with same spiral capacitor are given in following Fig. 6. These filters are simulated using a first order LC series resonant BPF configuration with lumped model.

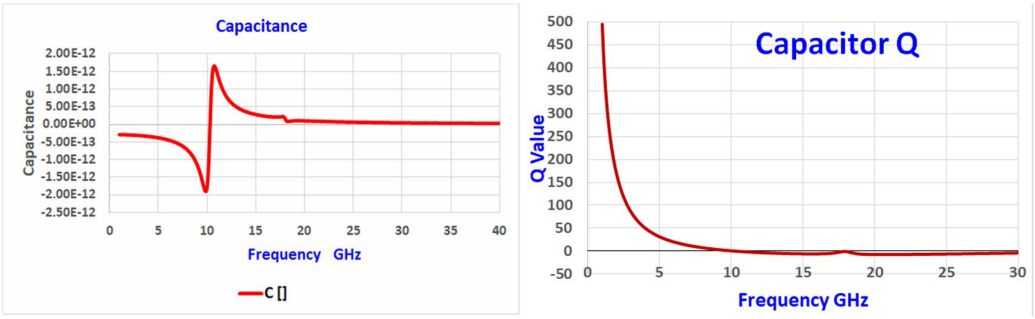
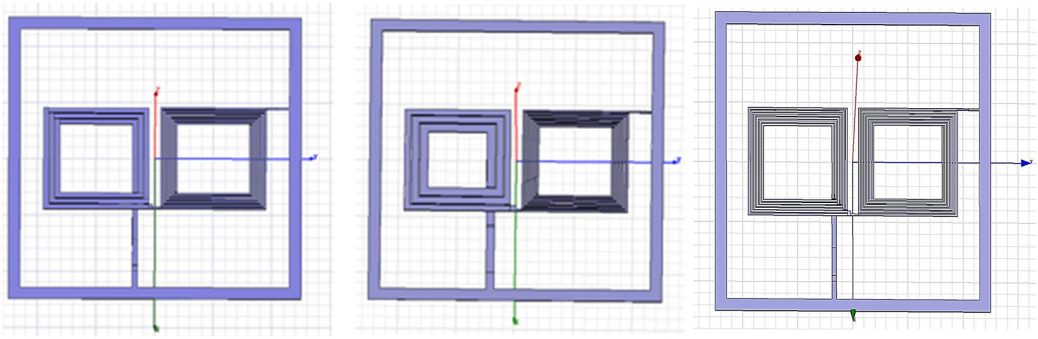


Fig. 5 Variation of the Capacitance and Q Value of the Planar Capacitor



Constant Width L BPF b) Variable Width L BPF c) Double split L BPF

Fig. 6 Constant width L BPF Structure with 3 ML spiral Inductors and planar spiral capacitor

Filter S parameters are obtained from HFSS terminal solution report. The return loss S_{11} and insertion loss S_{12} characteristics obtained from HFSS simulations are reported in the following Fig. 7 and Fig. 8. The center frequencies of three simulated LC resonant BPFs are located at 4.9, 5.5 and 5.25 GHz. The three BPFs have bandwidths of 1200, 950 and 800 MHz respectively. They have reported good return loss of -19.8, -27.5 and -30.96 dB respectively. The three filters have produced excellent insertion loss of -0.67, -0.49 and -0.37dB at center frequency of their respective pass bands. The BPFs simulated have Quality factor values of 4.08, 5.79 and 6.56 respectively. They possessed fractional bandwidths of 24%, 17.2% and 15.2% as per simulation reports. The design plan and simulation reports are compared in the following Table-II.

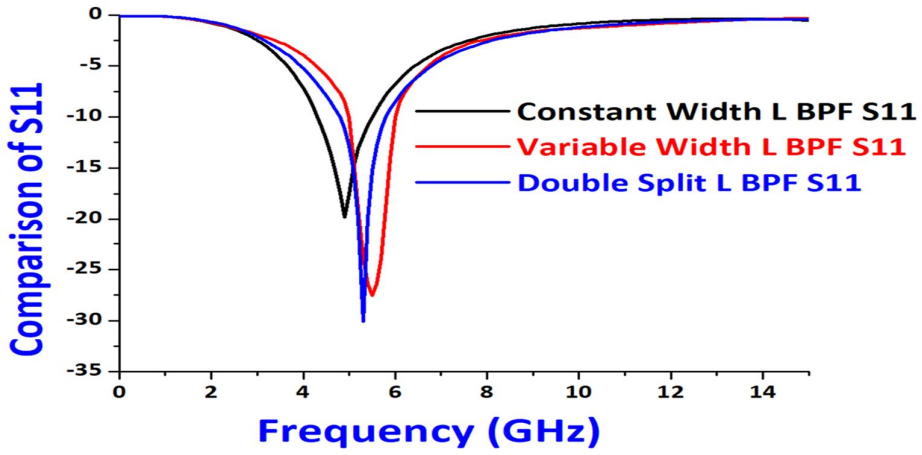


Fig. 7 Comparison of the Return Loss S_{11} for the three simulated BPF filters

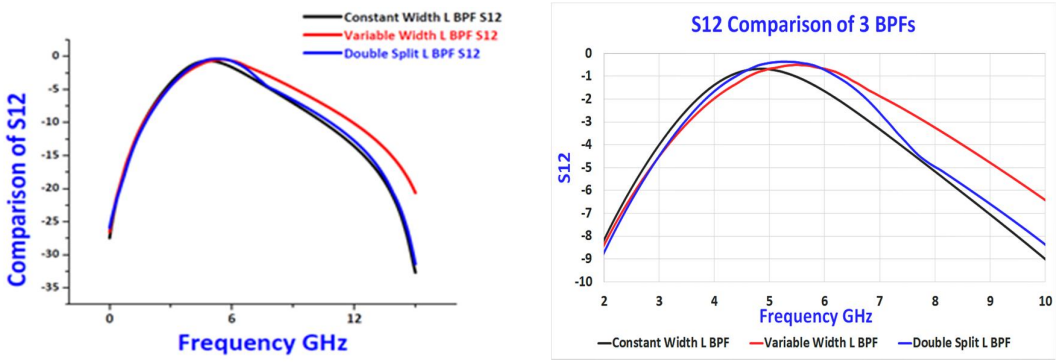


Fig. 8 a) Comparison of the Insertion Loss S_{12} for the three BPF filters b) Expanded view of S_{12} vs frequency

TABLE II. COMPARISON BETWEEN THE DESIGN PLAN AND SIMULATED FILTER PERFORMANCE

BPF	Design Specifications	Simulation Results		
		Constant Width L BPF	Variable Width L BPF	Double Split L BPF
Sub-6GHz 5G NR bands	IEEE 802.11a (UNII) band WLAN (5.15–5.35 GHz); WiMAX IEEE 802.16 (4.5 – 5.97 GHz) RFID (4.9-5.8GHz); ETSI HIPERLAN/2 (5.15-5.825 GHz); ISM (5.2-5.350 GHz);			
Center Frequency, f_0 GHz	5.15-5.35	4.9	5.5	5.25
Fractional Bandwidth, % ΔF	15-20	24	17.2	15.2
Quality Factor, Q	5-10	4.08	5.79	6.56
Return Loss S_{11}, dB	-25 to -35	-19.8	-27.5	-30.96
Insertion Loss, S_{12}, dB	-0.5 to -1	-0.67	-0.49	-0.37
On Chip Area, mm^2	0.05-0.1	0.068	0.068	0.068

The double split inductor based BPF had better sensitivity as it has lowest fractional bandwidth relative to other 2 filters. All the three filters are designed with same on chip occupied area of only 0.068 mm^2. All the filters exhibited very well out of band attenuations and better pass band characteristics. The superior loss of these filters will surely reproduce good quality RF output signals much suitable for 5G WLAN accessing.

D. Results and Discussion

The above three proposed heavily miniaturized BPFs had demonstrated best possible insertion loss and sufficient return loss results. The BPF designed using the double split inductor has 11.2 dB (156%) smaller return loss, when compared with constant width inductor BPF and also showed 3.41 dB (112%) smaller return loss, against the variable width spiral inductor BPF. The filter designed using the double split inductor has 0.3113 dB (53%) less insertion loss against constant width inductor BPF and also showed 0.1369 dB (72%) less insertion loss against the variable width spiral inductor BPF. The occupied chips pace of 0.068 mm^2 for all three filters is the least possible on chip area amongst all the referred bandpass filters [1] to [17]. The performance of three designed filters is compared with that of similar reported BPFs in the following Table-III. The above comparison clearly depicts the superior performance of the filters under this work. Especially when it comes to optimization against multiple filter performance parameters like on chip area and insertion loss. Our proposed filters perform well above the other state of art filters with lowest S_{12} and chip occupied area.

III. CONCLUSIONS

Purpose of this work is to verify the key enhancements easily feasible in terms of the area occupied on the chip and the filter performance by employing IPD technology. This paper presents carefully designed 5G suitable BPFs, including three ML inductors and a spiral capacitor, emphasizing the optimization of geometry and device parameters, for the frequency band of interest being sub-6 GHz 5G standard. In particular the design concentrates on minimizing the onchip area for the filters. For any given inductance value, 3D structures possess a higher quality factor. Double split inductor exhibited higher Q value of 25.3532. It is found that capacitance and Q values of capacitor are decreasing with increasing operating frequency, as per literature.

Proposed 5G BPFs demonstrated the least possible insertion loss (< -0.5 dB) over the 5–6 GHz bandwidth. Notably, a very compact 0.068 mm^2 area BPF has been successfully designed and verified in this work. Because of many performance enhancements, the above super compact sub-6 GHz IPD filters can surely realize an RFFE system-in-package, to meet the emerging demands of the 5G WLAN applications.

TABLE III. ELECTRICAL PERFORMANCE OF THE SIMULATED BPF COMPARED WITH THE STATE OF THE ART

References [.]	Technology	Center Frequency GHz	Fractional Bandwidth %	Q Value	Return Loss S_{11} dB	Insertion Loss S_{12} dB	On Chip Area mm^2	No. of Layers
I Vassiliou 2003	Si CMOS	5.24	3.8	26	-12	-	18.45	6
A Italia 2008	AlSiCu HSB3	5.5	9	10.57	-12.2	-	4.84	1
Sanduleanu 2008	90nm CMOS	6	14	7.05	-10	-	1.05	1
Chen 2011	Microstrip	4.8	6	16.66	-18	-2.5	0.9	3
ChiaSong Wu 2011	Al_2O_3 IPD	5.1	55	1.82	-27	-5.8	0.55	3
MA Abdalla 2014	Microstrip	5	18	5.55	-50	-0.5	3000	1
Ruifang Su 2015	Microstrip	3.1 – 10.9	1.4	71	-16	-0.8	73.9	1
BVN Deevi 2016	CMOS	40	7.9	12.62	-18	-2.1	0.0256	3
Nan Li 2017	CMOS IPD	1.7	29.4	3.4	-15	-2.0	0.3	1
Ki R Shin 2018	Si IPD	3.6	13.8	7.2	-26	-1.8	1.28	2
Yang Chen 2019	GaAs IPD	1.8-3.0	50	2	-33	-3	2.86	1
NO Parchin 2020	Microstrip EBG	4.9	12.7	7.85	-30	-1.5	225	1
Xiaomei Li 2020	Si HRS IPD	3.75	24	4.16	-35.65	-1.52	2.5	1
Raghunadh 2020	CMOS IPD	5.1	27	3.65	-25.64	-0.43	0.16	3
This Work Constant Width, Variable Width and Double Split L BPF	CMOS IPD	4.9	24	4.08	-19.8	-0.67	0.068	3
	CMOS IPD	5.5	17.2	5.79	-27.5	-0.49	0.068	3
	CMOS IPD	5.25	15.2	6.56	-30.06	-0.37	0.068	3

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