

Implementation and Performance Analysis of Boundary Scan Testing

Urmila Pariya¹, Shreya Patel², Divyesh Nariya³ and R.A. Thakker⁴

^{1,2}Department of ECE, GTU – GSET, Ahmedabad, India

Email: urmilapariya081@gmail.com

³Lead Engineer, MicroCircuits Technology, Ahmedabad, India

Email: divyeshnariya009@gmail.com

⁴Adjunct Professor, GTU – GSET, Ahmedabad, India

Email: rathakkar@gtu.edu.in

Abstract—Testing refers to the process of checking the accuracy of a device manufactured using specific test stimuli and observing the output signals. Boundary Scan is a technique of testing interconnections to printed circuit boards or small blocks contained in an IC. The boundary scan circuitry is included in the ICs input and the test is performed by supplying test patterns. The proposed work is about the study and analyzing recently reported boundary scan testing techniques. This work mainly focuses on IEEE Std 1149.1 and 1500 because these are widely used nowadays as compared to other standards. In the proposed work, boundary scan testing is carried out by considering SoC design as core logic. Some issues are analyzed in proposed SoC testing and an appropriate solution is provided. The effectiveness of this method is analyzed by measuring fault coverage and speed of execution for the design.

Index Terms— DFT (Design for Testability), IEEE std 1149.1, IEEE std 1500 Core Logic, Boundary Scan testing, Boundary Scan Cell.

I. INTRODUCTION

Today, semiconductors are among the most progressive developments in the entire electronics industry. The introduction of new technologies, especially nano meter technology with 14 nm or small geometry, has allowed the semiconductor industry to adapt to the growing demand for the working capacity of consumers. This has illuminated the prospects for future industrial growth. However, new technologies come with new challenges. Smaller die sizes increase the chances of further errors and testing the designs with smaller die sizes becomes more complex.

The solution to these problems is DFT (Design for testability). It is a design technique that produces testing a chip possible and cost-effective by adding additional circuitry to the chip. Nowadays there are dozens of designs and it is almost impossible to imagine a test unit dedicated to each device. IEEE, therefore, created a standard test known as IEEE 1149 by the Joint Test Action Group (JTAG) also known as a boundary scan in the 1980s. Boundary Scan is a technique for testing connections to printed circuit boards or small blocks contained in an IC, and it is widely used to measure the voltage at various pins or current or reading memory blocks. Since then, electronics manufacturers around the world have used this technique. It includes board level testing, infrastructure testing, connection testing, and additional functions such as logical component test, RAM test,

external connector test, LED or display test, FLASH test, System / ID read, etc.

This standard eliminates the idea of creating a dedicated test unit for a different design. Instead, it describes how to test any PCB or Integrated Circuit (IC) board using 5 PINs and a controller. These PINs are Test Data In (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset (TRST), and Test Clock (TCK). The controller is known as a Test Access Port (TAP) Controller. Fig.1 describes the basic boundary scan procedure. The JTAG testing standard defines a wrapper around the core logic known as Boundary Scan Cell (BSC) which is shown in Fig.1. Each port of core logic has one BSC. It is connected to the ports of core logic as well as connected to each other and forms a scan chain. This combination of BSCs is known as a boundary scan register. There exist boundary scan testing methods for different core logics that utilize boundary scan design. The method proposed in [1] uses ALU as core logic, and area, power, and speed are evaluated. Boundary scan logic for a 64-bit floating point subtractor unit is designed in [2], and it was also successfully synthesized on a Virtex – 6 FPGA. Testing of RISC-V-like processor is carried out in [3] by developing a virtual tester for it with the help of IEEE Std. 1149.1. An enhanced boundary scan architecture is introduced in [4] for inter-die interconnect leakage measurement in 2.5D and 3D ICs. Delay faults are tested in 3D ICs using boundary scan design in [5] and test time reduction is achieved.

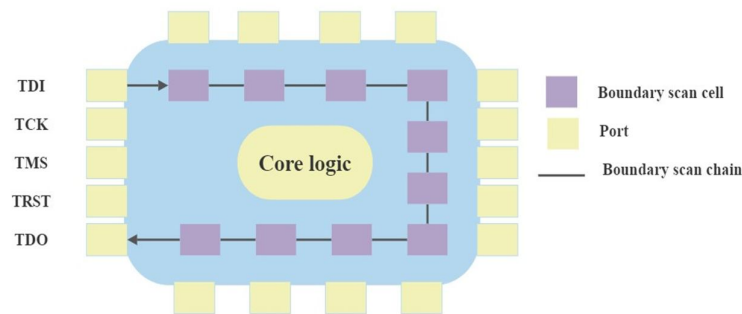


Fig. 1. Boundary scan test basic diagram

The proposed work is to analyze different methods of boundary scan testing, which is followed by boundary-scan testing for SoC using the 1149.1 and 1500 standards.

II. ARCHITECTURE OF BOUNDARY SCAN TESTING

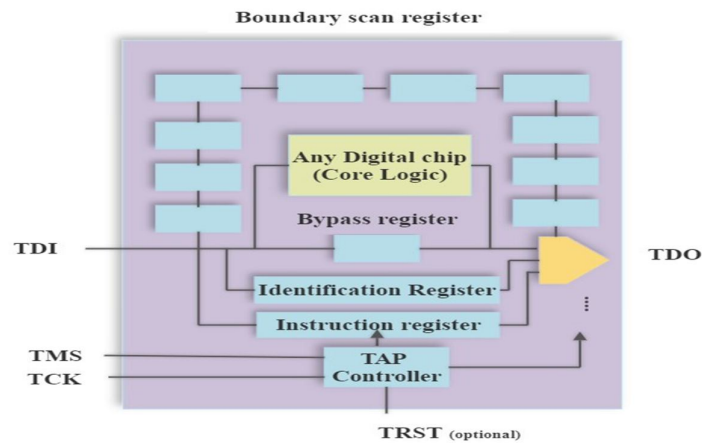


Fig. 2. Architecture of boundary scan testing

Boundary scan test architecture is having four mandatory pins TDI, TDO, TMS, and TCK, and one optional pin TRST. TDI and TDO pins are test data input and output pins. TCK pin is used to provide a clock to boundary scan circuitry. TMS is test mode select pin to select the mode which can be either test mode or functional mode. Test mode is selected to enable boundary scan testing and functional mode is selected to work with normal functions of the circuit. TAP controller is used to control the whole circuitry. Architecture contains data registers and instruction register. The data registers include the bypass register and a boundary scan register. Boundary

scan register is a chain of BSCs as we have discussed earlier. It is used to control the input and output of the circuit in test mode. Bypass register is used to bypass the test input in functional mode. The instruction register and instruction register decoder are used to control the data registers by decoding the instructions provided by the TAP controller.

III. DESIGN AND IMPLEMENTATION

The proposed boundary scan testing technique uses a SoC design as core logic. The design contains IEEE std 1149.1 and IEEE std 1500 are both standards of boundary scan testing. IEEE Std 1149.1 describes a wrapper architecture and access mechanism designed for the purpose of testing components of a board whereas IEEE Std 1500 has a similar structure targeted towards testing cores in an SoC. Design contains total 86 boundary scan registers, 16 serial input pins and 16 serial output pins, a single TAP controller of 1149.1 std, and 86 WSC (Wrapper Serial Controller). It also contains Star Memory System server logic to test the memories and to connect 1149.1 and 1500 pins.

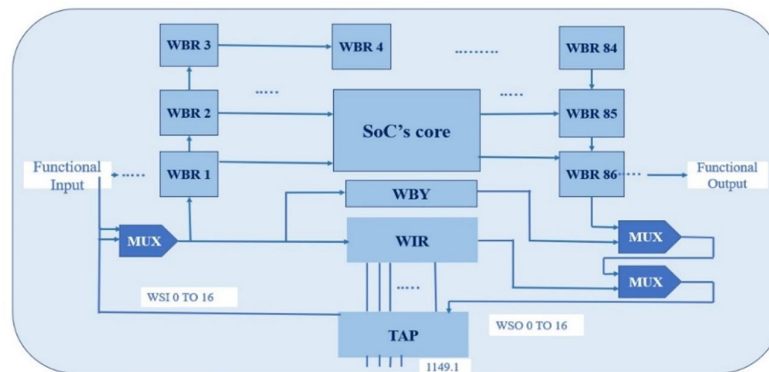


Fig. 3. Architecture of SoC under consideration

The specifications of the proposed SoC are shown in Table I.

TABLE I. SPECIFICATIONS OF SOC

SoC parameter	Value
Technology	7nm FinFET
No. of macros	11 (6-submacro, 5-IP)
Memory size	2.3 Mbit
Total memory	239 memory cells
Memory type	RAM, ROM
Area of SoC	50mm
Frequency of CPU	1.2 GHz

Table.II describes Boundary scan pins used for boundary scan test purposes in the proposed SoC.

TABLE II. BOUNDARY SCAN PINS FOR SOC BEING TESTED

Pin	Pin Type	Pin name
Test data input	Inout	tdi_o
Test data output	Inout	tdo_i, tdoen_i
Test clock	Inout	tck_o
Test mode select	Inout	tms_o, tm_clk_o
Test mode enable	Input	TME, tme_o
Test reset	Inout	trst_o

A. Connection of IEEE std 1149.1 and 1500

SMS stands for Self-test and repair Memory System. It is a comprehensive, integrated test, repair, and diagnostics solution that supports repairable or non-repairable embedded memories [6]. In this work, SMS is used for connecting two standards of boundary scan testing and also to test the memories with the help of IEEE std 1500.

D. BST Instructions

Boundary scan testing instructions that are used to test the proposed SoC are described below.

Sample/Preload

During the execution of the SAMPLE/PRELOAD instruction, the boundary scan register can be accessed through a data scan operation to obtain a functional data sample to input or output the device. Test data can be preloaded at the boundary scan register before executing the EXTEST instructions.

Extest

The EXTEST command will test the interconnection of the PCB. The 1149.1 compliant device enters the external test mode and selects the boundary scan register to be connected between TDI and TDO.

Intest

INTEST instruction is used to test the internal circuitry of design. During this instruction TDI and TDO lines will be connected to the Boundary Scan Register (BSR). While the EXTEST instruction allows the user to set and read pin states, the INTEST instruction relates to the core-logic signals of a device.

Bypass

Using the BYPASS instruction, a device's boundary scan chain can be skipped, allowing the data to pass through the bypass register. Bypass instruction bypasses a particular core logic from testing, and the remaining portion of the chip will be considered in testing

IV. RESULTS AND DISCUSSION

In this section, we discuss issues that are faced in boundary scan testing along with the proposed solution, fault coverage, and speed of execution of the Proposed SoC.

A. Issues faced in proposed SoC testing

Connection issue of ports

We observed a connection issue between WSO (Wrapper Serial Output) and TDO (Test Data Output) because of the SMS server. When output data is passing from the wrapper of IEEE 1500 to the TAP controller, there is a delay of half cycle or more. It is solved by adding a delay of half/full clock cycle by including a latch or flip-flop.

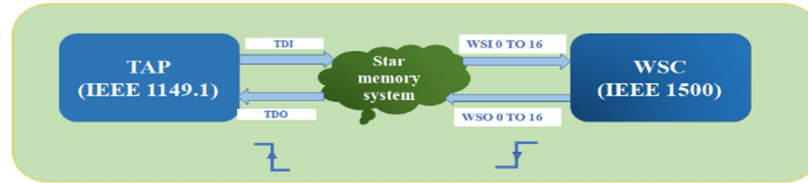


Fig. 7. Issue of connection between WSO and TDO

Clock Gating

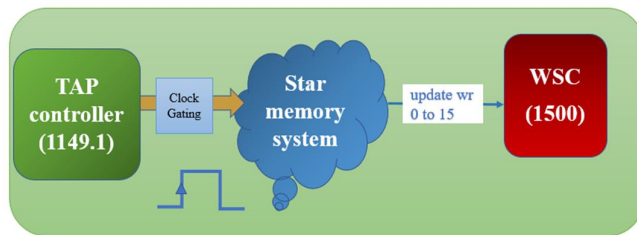


Fig. 8. Clock gating issue

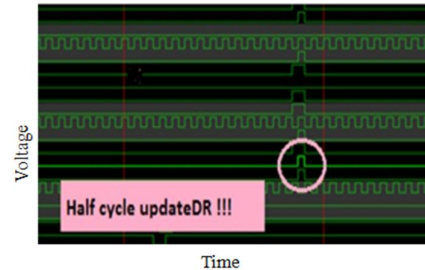


Fig. 9. Simulation results of clock gating issue

A clock gating structure is introduced in this design to reduce power dissipation, and due to this structure, some port states remain the same as the previous state. So that there was synchronization problem between the SMS

server and the Wrapper of IEEE 1500 std. Because of this, we are facing an issue to update the wrapper pin - update sWR (wrapper) pin. This issue is shown in FIG.9. Where we are getting a half clock cycle at update WR pin, ideally there should be full clock cycle at update WR pin.

The solution is to Update the RTL of the design. By updating the RTL of JTAG Macro we have resolved the issue. Here JTAG macro is memory cell where we were facing this issue.

Race around condition

We observed that when TCK and TMS signals arrive together, there will be a data loss. This situation is known as Race around condition. It is shown in Figs. 9 and 10. The race around condition can be solved by introducing some delay between TCK and TMS signal as shown in Fig. 10.

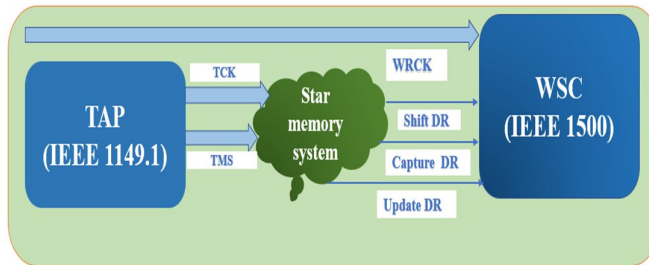


Fig. 10. Issue of Race around condition.

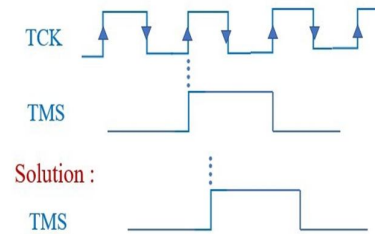


Fig. 11. Solution of race around condition issue

B. Fault coverage of the design

Design is first tested without Boundary scan testing (BST) by using manual testing methods and also using the BST technique. The results of both techniques are described in Fig.11.

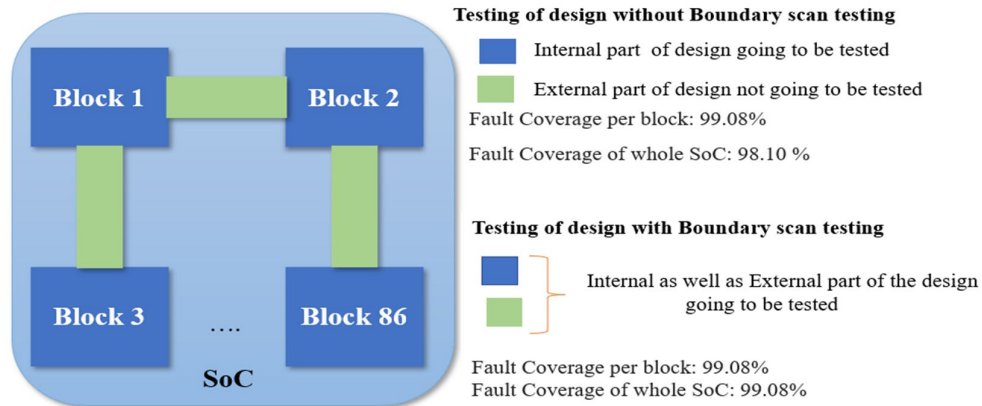


Fig. 12. Fault coverage of proposed SoC

In manual testing only, internal testing is done. We are getting per Block fault coverage of 99.08% and the whole SoC fault coverage is 98.10%. Since BST can test both internal and also external circuitry of design by using Intest and Exttest instructions, we can get higher fault coverage of overall SoC as compared to manual testing methods. Fault coverage by utilizing the BST method is 99.08% for both per block as well as whole SoC.

TABLE IV. FAULT COVERAGE OF PROPOSED SOC

Fault Coverage	Without BST	Boundary scan testing technique
Per Block	99.08 %	99.08 %
Whole SoC	98.10 %	99.08

C. Speed of execution of the design

Manual testing requires probes for testing, whereas Boundary scan testing will carry out the testing without any probes. In boundary scan testing Bypass register is used to skip the blocks which are not going to be tested. so, boundary scan testing will consume less time compared to Manual testing.

- Time taken for manual testing: 10 seconds
- Time taken for Boundary scan testing: 1.10 μ s

V. CONCLUSION

The boundary scan testing for SoC is discussed in this paper. The design includes IEEE standards 1149.1 and 1500. Both standards are for boundary scan testing. During boundary scan testing, we identified various issues and the solution is also proposed. The design is also tested manually as well as with the help of boundary scan testing. The fault coverage in the testing of the individual block remains the same. But, in the testing of the entire SoC, the fault coverage improves in the case of boundary scan testing. There is a significant reduction in testing time with boundary scan testing. It reduces from 10 seconds to 1.10 μ s.

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