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Investigation of Dependence of Breakdown Voltage on the N-pillar Doping Concentration of Deep Trench Super-Junction Vertical Double Diffused MOSFET

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***Abstract*— In this paper, the dependence of breakdown voltage on the N-type pillar doping concentration of a silicon-based Deep Trench Super-Junction Vertical Double Diffused MOSFET is carried out using TCAD simulation. The variation of the electric field distribution and impact ionization rate under high drain bias conditions are studied in detail. Also, a peak electric field localization and avalanche initiation within the drift region with varying N-pillar doping concentration are studied. From the analysis, it is clear that the moderately doped N-pillar enables uniform depletion and delays the onset of impact ionization, leading to improved breakdown voltage. However, higher doping levels cause partial depletion and premature field crowding away from the drain junction, leading to earlier breakdown. This study highlights the need for optimized N-pillar doping concentration for improved device performance.**

***Index Terms*— TCAD simulation, Vertical Double Diffused MOSFET, electric field, impact ionization rate, super-junction device and breakdown voltage.**

I. INTRODUCTION

The advancement of machine learning and artificial intelligence have resulted increase in the requirement of power electronics devices for power integrated circuits. Power electronic devices have high electrical stress tolerance and long-term reliability [1] which are necessary for AI infrastructure including data centres, edge-level platforms, and intelligent transportation infrastructure. Hence, improving the reliability and energy efficiency of power semiconductor devices is crucial for sustainable AI-driven technologies.

Vertical Double Diffused MOSFETs (VDMOS) are the most popular power devices for AI enabled workloads due to their features like large input impedance, high switching speed and high thermal stability. The ON resistance of a VDMOS device being one of the important parameters should be low, as it directly influences the amount of current the device can safely conduct before excessive internal heat generation which leads to a failure. Alongside one more important parameter, that is, device's maximum blocking voltage should be high, which defines the highest voltage it can withstand in the OFF state without undergoing breakdown. Hence a better understanding of breakdown behavior in VDMOS structure is needed for developing circuits like voltage regulators, power converters and motor drive units [2][3]. Though materials like Silicon Carbide (SiC) have gained attention because of their superior thermal performance and high critical electric field, silicon still dominated the power electronics because of its cost-effectiveness and ease of fabrication [4].

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In this work, two-dimensional TCAD simulations are employed to extract electric field profiles using cut-plane analysis and to evaluate the corresponding impact ionization behavior under high drain bias conditions. The study aims to quantify the material-dependent breakdown characteristics and highlight the constraints imposed by silicon in advanced VDMOS architectures.

A. Simulated Device Structure

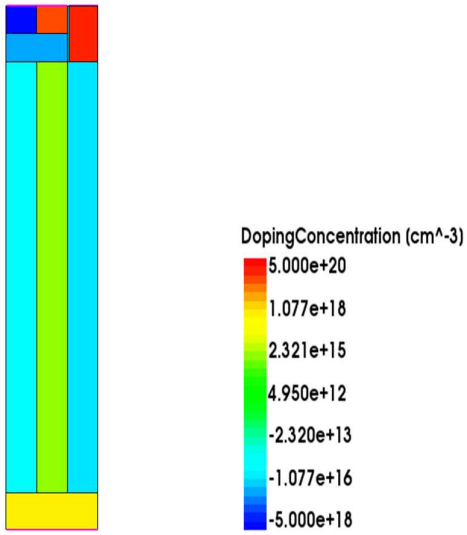

Figure 1. Structure of the simulated DTSJVDMOS

DTSJVDMOS device simulated using Sentaurus TCAD is depicted in Fig 1 [5]. P+ layer's doping concentration, which forms the bulk-contact is 5x1018/cm3 and it has a length and width of 1µm and 0.795µm respectively. Source is N+ layer having a length of 1µm and doping concentration of 5x1019/cm3. P-well forms the channel with gate length of 0.755µm. Channel doping concentration is 1x1017/cm3. P-pillar is having a length and width of 12µm and 1µm respectively with doping concentration of 1x1015/cm3. N-pillar is also having a length and width of 12µm and 1µm respectively with doping concentration of 1x1015/cm3. N-pillar doping concentration is varied to obtain the breakdown voltage trend.

II. Results and Discussions

The results obtained from the TCAD simulation of DTSJVDMOS is analyzed in this section. Id-Vd characteristics obtained for various N-pillar doping concentration (1×10^{15}, 2×10^{15}, 5×10^{15}, 1×10^{16} cm^{-3}) is as shown in Fig 2. From the figure, it is clear that the breakdown voltage improves slightly and then it reduces as the N-pillar doping concentration is increased.

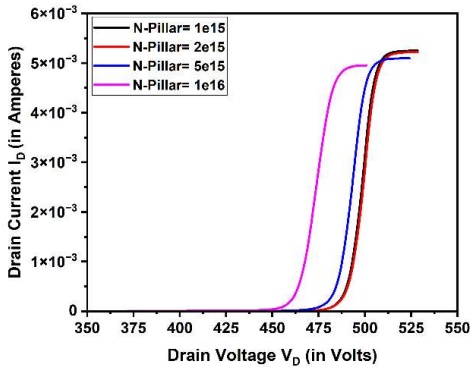

Figure 2. Id-Vd characteristics of DTSJVDMOS for varying N-pillar doping concentration at Vgs = 0 V

At low drain voltages, low drain current indicates that the device is operating in off state with negligible leakage. As drain voltage increases, the electric field becomes stronger in the drift region near the drain end of MOSFET. This strong electric field is the cause of several failure mechanisms, because of which drain current raises significantly even when the device is in off state (V_g=0 V). As the field increases, high energy carriers undergo impact ionization leading to generation of electron hole pairs, causing chain reaction. This leads to abrupt increase in the current. The sharp rise is observed in the range 450-500 V based on N-pillar doping concentration. The breakdown appears at higher V_ds for lower doping concentration because of complete depletion in the drift region. But for higher concentration, breakdown occurs at lower V_ds due to electric field crowding and partial depletion.

In order to understand the physics behind this trend, the 2D impact ionization profiles are analyzed. Fig. 3(a), 3(b), 3(c), 3(d) and 3(e) show the impact ionization distribution profile of DTSJVDMOS at various Vds. From the figures, it is clear that the impact ionization is increasing near the drift-drain junction. This eventually leads to breakdown.

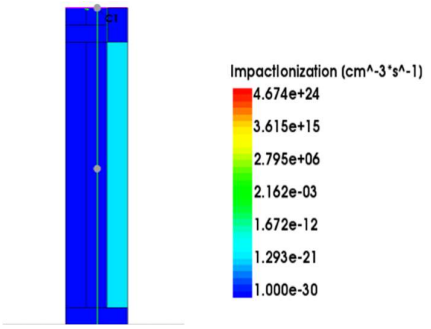

Figure 3(a). Impact Ionization profile for V_{ds} = 0 V (with N-pillar=$1\times10^{15}/cm^3$)

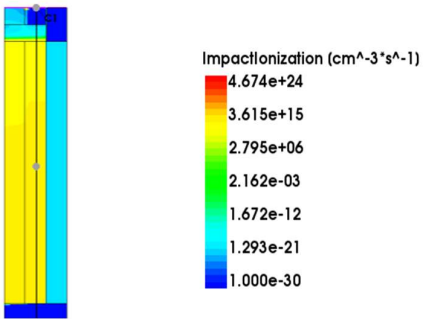

Figure 3(b). Impact Ionization profile for V_{ds} = 200 V (with N-pillar=$1\times10^{15}/cm^3$)

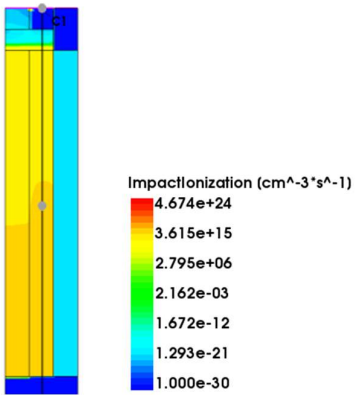

Figure 3(c). Impact Ionization for V_{ds} = 300 V (with N-pillar=$1\times10^{15}/cm^3$)

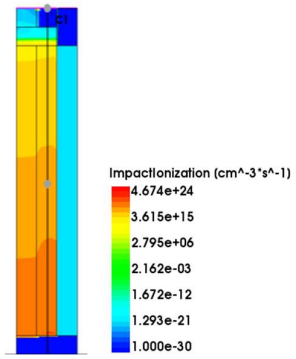

Figure 3(d). Impact Ionization for V_{ds} = 400 V (with N-pillar=$1\times10^{15}/cm^3$).

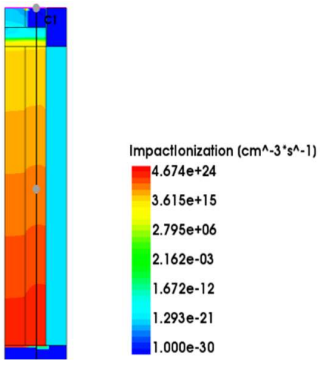

Figure 3(e). Impact Ionization for V_{ds} = 450 V (with N-pillar=$1\times10^{15}/cm^3$).

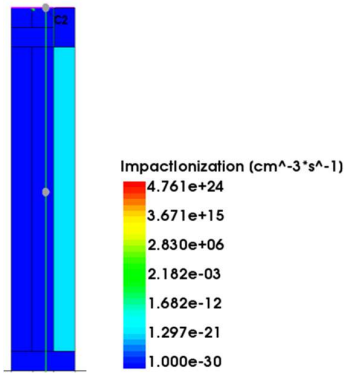

Figure 4(a). Impact Ionization for V_{ds} = 0 V (with N-pillar=$2\times10^{15}/cm^3$)

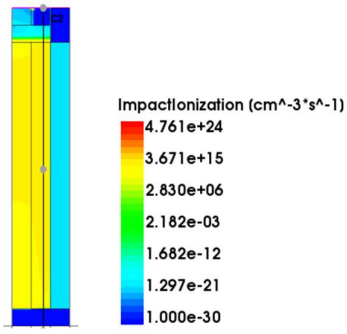

Figure 4(b). Impact Ionization for V_{ds} = 200 V (with N-pillar=$2\times10^{15}/cm^3$).

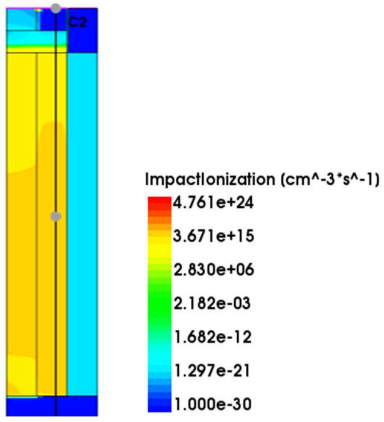

Figure 4(c). Impact Ionization for V_{ds} = 300 V (with N-pillar=$2\times10^{15}/cm^3$)

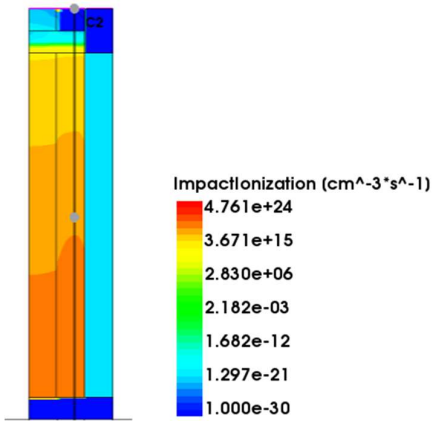

Figure 4 (d). Impact Ionization for V_{ds} = 400 V (with N-pillar=$2\times10^{15}/cm^3$)

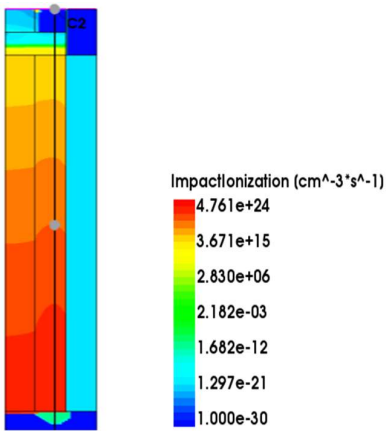

Figure 4 (e). Impact Ionization for V_{ds} = 450 V (with N-pillar=$2\times10^{15}/cm^3$)

However, for the devices with heavily doped N-pillar, the drift region is not fully depleted. As a result, the peak impact ionization occurs away from the drift-drain junction at a lower voltage. This leads to an earlier breakdown which is evident from Figs. 5(a) to 5(e). Hence the N-pillar doping concentration has to be optimized to obtain high breakdown voltage and low on-resistance. Comparison of the reported VDMOSFETs is shown in Table 1. This work shows comparatively less specific ON-resistance with higher breakdown voltage.

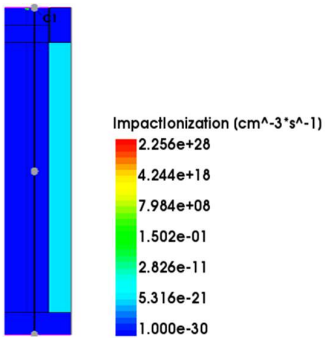

Figure 5(a). Impact Ionization for V_{ds} = 0 V (with N-pillar=$1\times10^{16}/cm^3$)

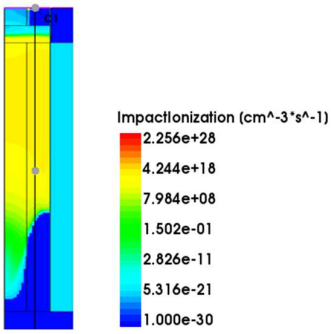

Figure 5(b). Impact Ionization for V_{ds} = 200 V (with N-pillar=$1\times10^{16}/cm^3$)

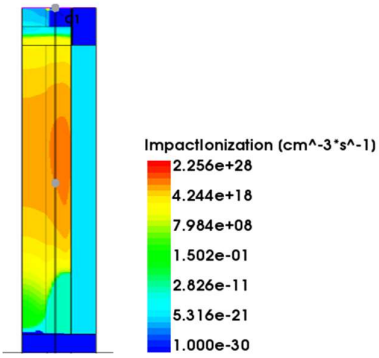

Figure 5(c). Impact Ionization for V_{ds}= 300 V (with N-pillar=$1\times10^{16}/cm^3$)

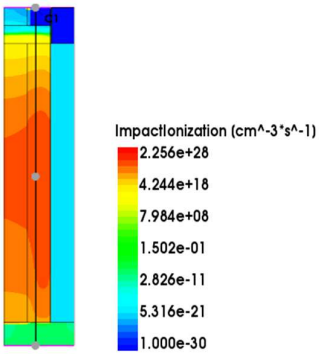

Figure 5(d). Impact Ionization for V_{ds} = 400 V (with N-pillar=$1\times10^{16}/cm^3$)

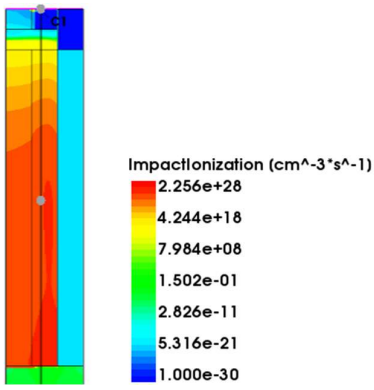

Figure 5(e). Impact Ionization for V_{ds} = 450 V (with N-pillar=$1\times10^{16}/cm^3$)

III. CONCLUSIONS

This work has demonstrated, through systematic TCAD simulations, how the variation of N pillar doping concentration critically controls the onset of impact ionization in Deep Trench Super Junction VDMOS devices. For DTSJVDMOS with lightly doping N-pillar, the drift region is fully depleted and results in higher breakdown voltage. But it results in lower current and higher on-resistance. As N-pillar doping increases, the drift region depletes only partially leading to impact ionization peak away from the drift-drain junction at a lower voltage. Hence the breakdown voltage reduces. The combined analysis establishes a clear trade off: lightly doped pillars ensure uniform depletion and higher breakdown strength, while heavily doped pillars lower on resistance but compromise breakdown voltage. These insights emphasize that precise control of pillar doping is the decisive design lever for balancing conduction efficiency with breakdown reliability. Optimized doping profiles can help silicon-based super junction VDMOS devices achieve strong high voltage performance. They can also fulfil the energy needs of today's AI and high-power electronic systems.

TABLE I: COMPARISON OF THE REPORTED VDMOSFET

Devices	Work	N_D of drift region (cm^{-3})	L (µm)	R_{on} ($\Omega.cm^2$)
4H-SiC UMOSFET	[6]	7.5 x 10^{14}	115	228
4H-SiC DMOSFET	[8]	8 x 10^{14}	85	123
UMOSFET	[7]	3 x 10^{15}	29	1
DTSJVDMOS	(This Work)	1 x 10^{15}	12	3.31

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