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Modelling and Simulation of a Novel Multilevel DC-AC Inverter

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***Abstract*—In this paper, a Novel multilevel DC-AC inverter has been proposed. The Proposed multilevel inverter (MLI) generates seven level AC output voltage with appropriate gate signals design. Here the operating principles of proposed MLI and voltage balancing of input capacitors are discussed by implementing RSCC circuit to proposed topology of inverter. The MLI is controlled with carrier-wave based Sinusoidal Pulse Width Modulation (SPWM) technique to produce different operating modes to generate respective voltage level at each mode by giving input of 400V DC across the capacitors and generating an output of 220Vrms AC voltage.**

***Index Terms*— Multi-level Inverter, Pulse Width Modulation, Sinusoidal Pulse Width Modulation, Total Harmonic Distortion, Phase Distortion, Resonant Switched Capacitor Converter, Cascaded H-Bridge.**

I. INTRODUCTION

Because of high technology development, the demand and the quality of electric power is higher than before. Due to the advancement of semiconductors, the specification of power devices and power conversion techniques is promoted. One of the power converters which can transform DC to AC is called "inverter". In past few years, many standards and regulations have been introduced to limit quality of harmonics and power factor in electrical equipment's. The industry demands high power applications, which results in high power switches. Even though Insulated Gate Bipolar Transistor (IGBT) have high power application characteristics, it cannot operate at high frequencies and designing of its gate-driver circuit is complex. To solve this problem, we can implement Metal Oxide Semiconductor Field Effect Transistor (MOSFET) instead of IGBT i.e., many different topologies of multilevel inverters are developed using low power rating component at high power applications [1].

To meet the requirements in high power applications, such as high-power rating of power electronic converters, MLI concept has been introduced. Cascaded H-bridge MLIs are widely used in both symmetrical and comparison asymmetrical topology (i.e., unequal voltage sources across the input side) has better performance results than symmetrical configuration topology and produces higher number of output voltage levels with same power switches requirement that is implemented for symmetrical topology [2][3][6].

The main drawback of MLIs are using IGBTs and diodes as power components which are less capable of operating at high frequencies [1][4]. If the input sources are utilized alternately in full cycles of output waveform, voltage balancing must be achieved in two cycles. To implement equal load sharing in MLIs, Carrier-

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wave based modulation scheme is employed for basic modules, called as “carrier rotation scheme” [7]. We can also implement 16F877A PIC microcontroller in control circuit of an MLI with Sinusoidal Pulse Width Modulation (SPWM) [8]. Control circuit of an MLI can be implemented using various schemes of PWM strategies such as Phase Disposition (PD), Phase Opposition Distortion (POD) and Alternate Phase Opposition Distortion (APOD). Among them, Phase Distortion technique is better in Total Harmonic Distortion (THD) and generates higher Vrms value of output voltage than other schemes having same requirements [12] [13]. A novel multilevel inverter is modelled and designed in this paper. The main feature of proposed topology is reduction in power components and producing higher levels of AC output voltage with lower % of THD in it. Carrier-wave based SPWM technique is used to control proposed inverter.

II. Power Stage

A. Circuit Configuration

Fig. 1 shows the proposed novel topology used in the seven-level inverter. An input voltage divider is composed of three series capacitors C_1, C_2, and C_3. The divided voltage is transmitted to H-bridge by four MOSFETs and four diodes (S1, S2, S3, S4 and D1, D2, D3, D4). The voltage is sent to output terminal (i.e., to load) by H-bridge which is formed by four MOSFETs (i.e., S5, S6, S7 and S8). The proposed MLI generates seven levels AC output voltage with the appropriate gate signals design.

B. Modes of Operation

The required seven voltage output levels ($\pm 1/3V_{dc}$, $\pm 2/3V_{dc}$, $\pm V_{dc}$, 0) are generated as follows:

1) In this mode we get an output voltage +1/3Vdc i.e., the first step in the output voltage waveform. The switches which are conducting in this mode of operation follow: S1-S5-Load-S8. The switches which are non-conducting are: S2, S3, S4, S6, S7. Now only three switches operate at a time to give the desired output form. The current flow path is follows S1-S5-Load-S8-(+1/3Vdc). Fig. 2 shows the current path at this mode.

2) In this mode we get an output voltage +2/3Vdc, i.e. the second step in the output waveform. The switches which are conducting in this mode of operation follow: S1-S5-Load-S4-S8. The switches which are non-conducting are: S2, S3, S6, S7. The current flow path follows S1-S5-R load-S8-S4-(+2/3Vdc). Fig.3 shows the current path at this mode.

3) In this mode we get the output voltage as +Vdc, i.e. third step of the output voltage in the positive cycle. The switches which are conducting in this mode of operation follow: S1-S5-Load-S8-S2. The current flow path follows: S1-S5-Load-S8-S2-(+Vdc). Fig. 4 shows the current path at this mode.

4) In this mode we get an output voltage -1/3Vdc i.e., the first step in the output voltage waveform. The switches which are conducting in this mode of operation follow: S7-Load-S6-S2. The switches which are non-conducting are: S1, S3, S4, S5, S8. The current flow path follows S7-Load-S6-S2-(-1/3Vdc). Fig. 5 shows the current path at this mode.

5) The switches which are conducting in this mode of operation follow: S3-S7-Load-S6-S2. The switches which are non-conducting are: S1, S4, S5, S8. The current flow path follows S3-S7-Load-S6-S2-(-2/3Vdc). Fig. 6 shows the current path at this mode.

6) In this mode we get an output voltage -Vdc i.e., the first step in the output voltage waveform. The switches which are conducting in this mode of operation follow: S1-S7-S6-S2. The switches which are non-conducting are: S3, S4, S5, S8. The current flow path follows S1-S7-Load-S6-S2-(-Vdc). Fig. 7 shows the current path at this mode.

7) In this mode all the switches are turned off as shown in figure below. The output voltage is zero hence the name 0Vdc. Fig. 8 shows the current path at this mode.

Table I lists the switching combinations at different output levels.

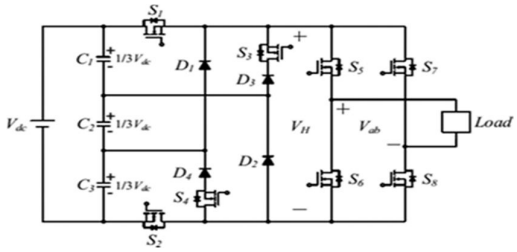

Fig. 1. Proposed seven-level inverter topology

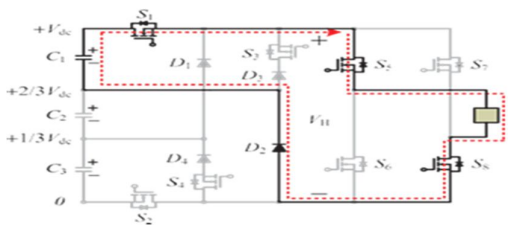

Fig 2. Switching combination of output voltage level $1/3V_{dc}$.

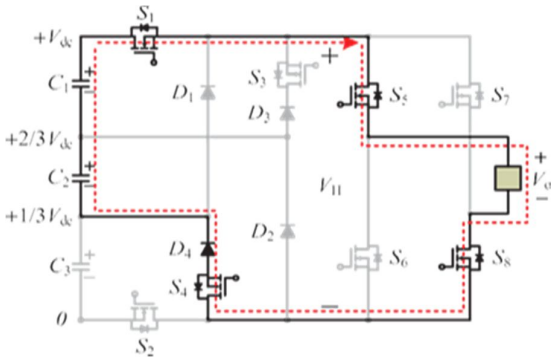

Fig. 3. Switching combination of output voltage level $2/3V_{dc}$.

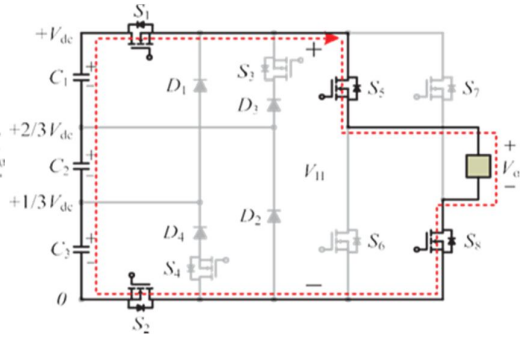

Fig. 4. Switching combination of output voltage level V_{dc}.

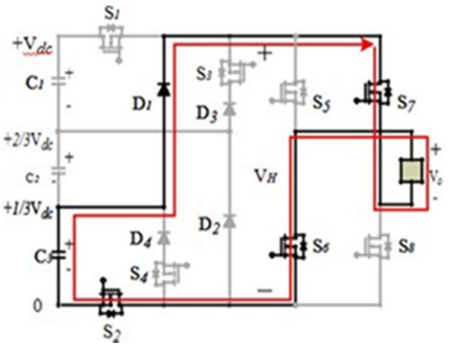

Fig. 5. Switching combination of output voltage level $-1/3V_{dc}$

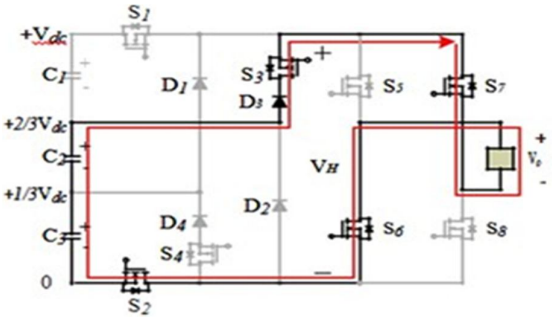

Fig. 6. Switching combination of output voltage level $-2/3V_{dc}$.

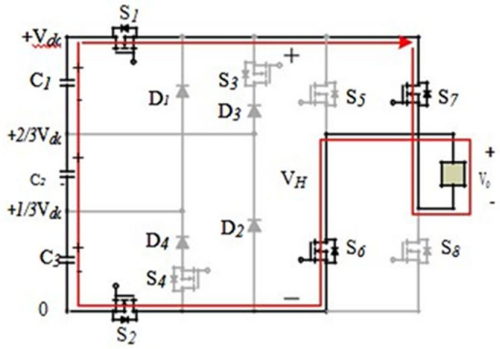

Fig. 7. Switching combination of output voltage level $-V_{dc}$.

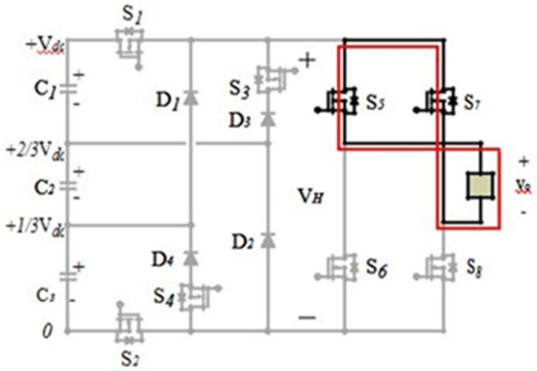

Fig. 8. Switching combination of output voltage level 0.

C. Topology Comparison

Table II presents the number of components required to implement a seven-level inverter using the proposed topology and other topologies [13]: such as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multi-cell inverter.

III. WM STRATEGIES

In this paper, several triangular carrier waves are distributed by phase disposition technique. The advantage of PD technique is uncomplicated, to realize and less total harmonic distortion. The frequency of carrier-wave is the switching frequency of inverter. The advantages possessed by PWM techniques are, the output voltage control can be obtained without any additional components, lower order harmonics can be eliminated or minimized along with its output voltage control, filtering requirements can be minimized as higher order harmonics can be filtered easily [12].

TABLE I. SWITCHING COMBINATIONS REQUIRED TO GENERATE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	On	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

TABLE II. COMPONENTS COMPARISON BETWEEN THREE DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-Clamped	Cascaded
Input Sources	1	1	3
Input Capacitors	3	6	3
Clamped Capacitors	0	0	0
Power Switches	8	12	12
Diodes	4	10	0

The rules for the POD method, when the number of levels is N = 7, then there are N –1 = 6 carrier waveforms are produced so that all the carrier waveforms are arranged in-phase. Fig. 9 shows the reference sine wave, carriers, and control signals of switches.

The method to determine switch signals in Fig. 9 are as follow:

(a) $v_{sin} < 0$ and $v_{sin} > v_{tri2} \rightarrow S_2$ is turned on

(b) $v_{sin} > v_{tri4} \rightarrow S_4$ is turned on

(c) $v_{sin} < v_{tri8} \rightarrow S_7$ is turned on

(d) $v_{sin} > v_{tri8} \rightarrow S_8$ is turned on

(e) $v_{sin} > 0$ and $v_{sin} < v_{tri1} \rightarrow S_1$ is turned on

(f) $v_{sin} < v_{tri3} \rightarrow S_3$ is turned on

(g) $v_{sin} > v_{tri6} \rightarrow S_5$ is turned on

(h) $v_{sin} < v_{tri6} \rightarrow S_6$ is turned on

IV. VOLTAGE BALANCING CIRCUIT BASED ON RSCC

Voltage deviation causes larger harmonics distortion in the output voltage, therefore voltage balancing circuits are necessary for the capacitors in the multilevel inverters [14]. By using resonant switching capacitor converter (RSCC), the voltage balance of input capacitors is achieved. Fig. 10 shows the circuit configuration of a unit of

the RSCC. The duty cycle of every switch is equal to 50%. The voltage of C_1 is higher than the voltage of C_2. Since the average current of C_1 is higher than that of C_2 at one switching cycle, most of the charges flow from C_1 to C_2. After few switching cycles, the voltage of C_1 and C_2 are equal. Fig. 10 shows the configuration of proposed seven-level inverter with RSCC. To apply RSCC at seven-level configuration, two switches S_{b5} and S_{b6}, resonant inductor L_r, and resonant capacitor C_r are added. In this application, switches S_{b1}, S_{b3}, and S_{b5} are turned on at the same time; S_{b2}, S_{b4}, and S_{b6} are turned on at the same time. The duty of each switch is equal to 50%. Fig 11 shows the six carrier waves and a reference wave which is used to generate appropriate gating signals for generating different level of voltages i.e., which describes the output waveform of the control circuit for proposed MLI.

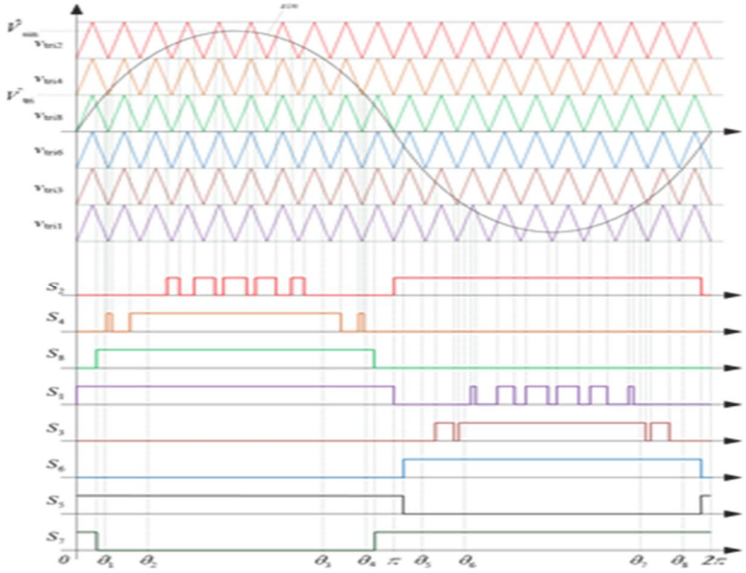

Fig. 9 the reference sine wave, carriers(N-1=6), and control signals of switches

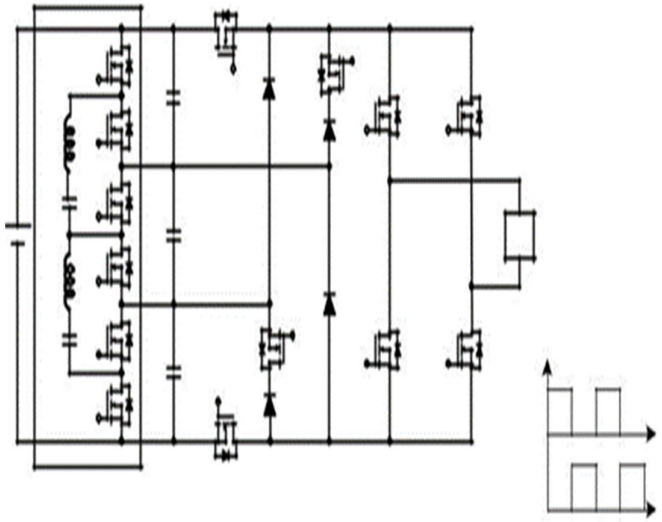

Fig. 10. The proposed multilevel inverter with RSCC

The output waveforms of proposed MLI which generates seven-level output voltage are shown in Fig.12 (without) and Fig.13 (with) RSCC respectively. The THD of proposed MLI is about 18.43% without implementing RSCC to it. Addition of RSCC circuit on the input side of MLI, is to enhance the performance of MLI by further decreasing the value of THD to 13.65%, such that its output is purely in sinusoidal waveform and provides voltage balancing.

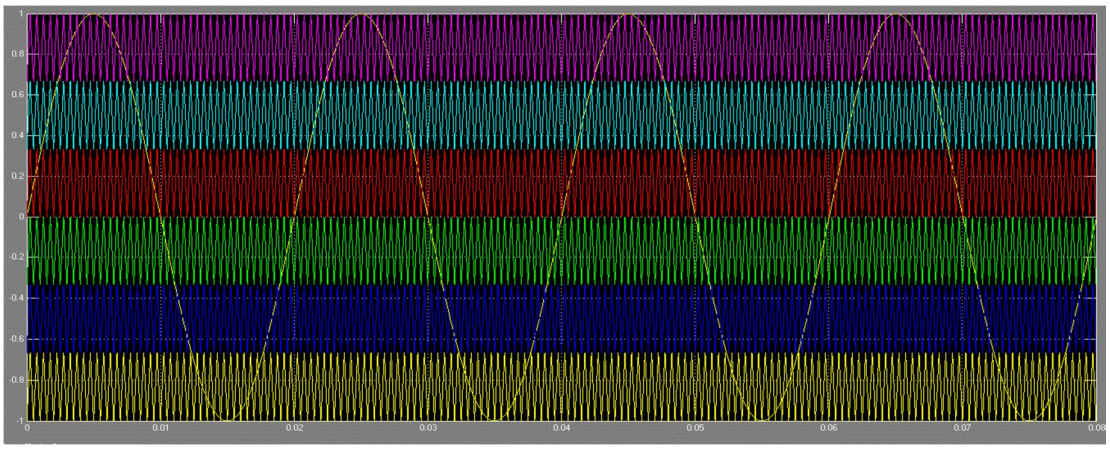

Fig. 11. Output waveform of control circuit

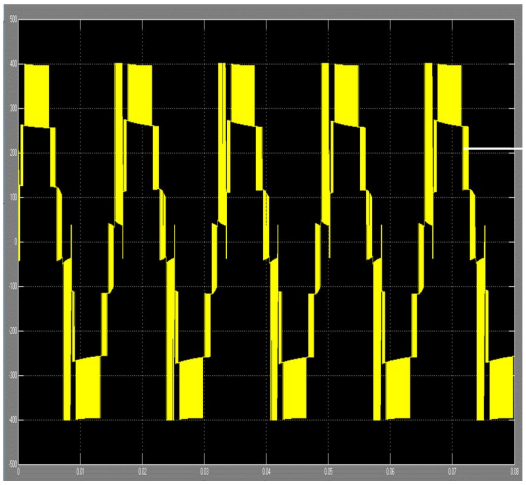

Fig. 12. Output Waveform of proposed multilevel inverter without RSCC

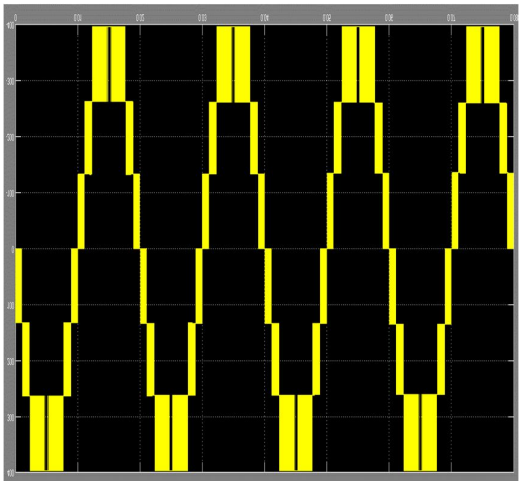

Fig. 13. Output Waveform of proposed multilevel inverter with RSCC

V. Conclusion

A novel seven-level inverter is modelled and simulated by implementing carrier-wave based SPWM technique. The main intension of proposed configuration is to reduce the number of power devices and reduction of % in THD in AC output voltage waveform. The reduction of power devices is proved by comparing it with other topologies. Finally, a seven-level inverter with 400V DC input voltage is applied across the voltage divider circuit (i.e., across the input capacitors) producing an output of 230 V_{rms} (approx.) i.e., 400V peak-peak.

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