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Review of Noise, Errors and Reliability in Digital Circuits

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***Abstract*— Digital systems are becoming more vulnerable to many types of noise, mistakes, and reliability issues as a result of the quick development of semiconductor technology and the increasing complexity of integrated circuits. The mechanisms that cause noise and mistakes in digital circuits, as well as the effects they have on the overall dependability and performance of the system, are thoroughly examined in this review paper. Important elements that affect logic integrity and timing behavior are examined, including crosstalk, electromagnetic interference, thermal noise, power supply oscillations, and process variances. The report also addresses the origins of many mistake types in deep submicron and nanoscale technologies, including as transient faults, soft errors, and permanent failures. A thorough study is conducted of methods for improving circuit reliability, including robust design-for-reliability approaches, fault-tolerant design, error detection and repair schemes, and redundancy approaches. Additionally highlighted are new dependability issues in contemporary computer paradigms, such as low-power, high-speed, and nanoscale devices. In order to guarantee the resilience and durability of upcoming digital systems, the review's conclusion highlights the significance of co-design approaches that incorporate reliability-driven and noise-aware design processes.**

***Keywords*— Interference in Digital Circuits, Mitigation Techniques for Interference, Error in Digital Circuits, Error detection and correction, Reliability of Digital Circuits, Circuit Hardening.**

I. Sources of Noise in Digital Circuits

Internal electronic phenomena like transistor switching and thermal noise, external electromagnetic interference (EMI) from the environment or other components, and power supply flaws like ripples and fluctuations are some of the sources of noise in digital circuits. Impedance mismatches, ground bounce from inadequate grounding, and crosstalk between traces on a PCB are other frequent causes.
Noise in a digital circuit can also be referred as unwanted electrical signals that interfere with proper operation.

A. External Interference

Cosmic rays, radio transmissions, and other electrical devices can all produce electromagnetic interference (EMI) and radio frequency interference (RFI). Disturbances may result from power or signal cables picking up these signals. Data mistakes, malfunctions, or even total equipment failure may result from this. Radio transmissions, cell phones, power lines, lightning, and even static discharge are examples of sources. Grounding, shielding, and using high-quality components are common mitigating techniques.

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B. Types of External Interference are

- Radiated Interference: Unwanted electromagnetic fields traveling through the air, like radio waves from a cell phone or Wi-Fi network.
- Conducted Interference: Electrical noise that travels through shared conductors or power lines.

C. Sources of External Interference

There are two types of external interference sources in digital circuits: radiated and conducted. Man-made sources include wireless devices, power lines, and industrial equipment, while natural sources include solar flares and lightning. Radiated interference spreads over the atmosphere as radio waves, whereas conducted interference moves through actual wires and power lines.

Man-made sources of Interference:

- Cellular networks and Wi-Fi signals
- Power lines and electrical motors
- Radio and television transmitters
- Switches and arc welders
- Microwave ovens

Natural sources of Interference:

- Lightning and electrical storms
- Solar flares
- Cosmic background noise from the sky

D. Effects of Interference on Digital Circuits

- Increased error rates: Noise can introduce erroneous bits, leading to incorrect data.
- Signal distortion: The desired signal can be corrupted by the unwanted noise.
- Component malfunction: Critical components may not operate as intended.
- System failure: In severe cases, the interference can cause the entire system to stop working.

E. Mitigation Techniques for Interference

- Grounding: Proper grounding of circuits provides a safe path for noise currents to dissipate.
- Shielding: Using conductive shields around sensitive circuits can block external electromagnetic fields from affecting the components.
- Component selection: Choosing high-quality electronic components can make them less susceptible to interference.
- Error correction: Modern digital systems use error correction codes to detect and correct data errors caused by noise.

F. Sources of Internal noise:

- Ground bounce: The ground reference may "bounce" or change as a result of current spikes in circuits with high-frequency switching, particularly on printed circuit boards (PCBs). This happens because the ground path's parasitic inductance keeps the voltage from dropping to zero right away, which can lead to double or false switching.
- Unwanted electromagnetic interaction between neighboring signal lines is known as crosstalk. A signal passing on one trace may cause noise on a nearby one because circuit traces are positioned closer together on PCBs.
- Johnson-Nyquist noise, also known as thermal noise, is a fundamental noise that results from the haphazard thermal mobility of electrons in a conductor. Resistance and temperature both increase its amplitude.
- Shot noise: This noise is produced by random variations in the arrival of charge carriers across a potential barrier, like a p-n junction, and arises from the discontinuous, quantized nature of electrical charge.
- Single-Event Transients (SETs): Sensitive areas of a semiconductor may be struck by high-energy cosmic radiation particles such as neutrons and alpha particles, producing a brief current pulse. A "soft error" could result from the circuit misinterpreting this pulse.

G. Types of Internal Noise

- Thermal Noise (Johnson Noise): The random thermal migration of electrons in conductive materials, such as resistors, is the source of thermal noise, also known as Johnson noise. Its power is evenly distributed across all frequencies (white noise), and it is proportional to both temperature and system bandwidth.

- Shot Noise: The discrete character of charge carriers (electrons and holes) in active devices like transistors and diodes causes shot noise. Current variations are caused by the erratic movement of these carriers, which is reliant on the bandwidth and DC current.
- Flicker Noise (1/f Noise): A low-frequency noise in which frequency and power have an inverse relationship. It is brought on by flaws in semiconductor materials and is predominant below a few kHz.
- Transit-Time Noise (High-Frequency Noise): This type of noise appears at higher frequencies when the period of the signal is equal to the time it takes for a charge carrier to pass a junction.

H. Causes of Internal Noise

- Random Movement of Electrons: Because of thermal energy, electrons in conductors are constantly moving randomly, which causes variations in voltage and current.
- Discrete Nature of Charge Carriers: Current fluctuates as a result of the random arrival of electrons and holes, which travel in discrete packets in semiconductor devices.
- Crystal Imperfections: Defects in the crystal structure of semiconductor materials can cause flicker noise.

I. Minimizing Internal Noise

- System Design: Careful design of the circuit and components can reduce the impact of internal noise.
- Bandwidth Reduction: Limiting the system's bandwidth can decrease thermal noise power, as it's directly proportional to bandwidth.
- Component Selection: Choosing components with lower inherent noise levels and proper layout can also help reduce noise.

II. Error in Digital Circuits

Digital circuit defects can be caused by transmission mistakes such bit corruption from noise and interference, or stuck-at problems, in which a signal is persistently fixed at a high or low value. By introducing redundant bits into the data, techniques like parity checks, check sums, and Cyclic Redundancy Checks (CRC) can identify and, in some situations, fix these flaws that result in improper data processing or transmission.

A. Types of errors caused by noise

Noise can lead to different types of errors, from temporary data corruption to permanent hardware damage.

- Soft errors: These are transient, non-destructive faults that change the data in the circuit without resulting in long-term hardware harm.
  - Single-Event Upset (SEU): A form of soft error, an SEU happens when a high-energy particle strikes a memory cell or latch, causing it to flip its stored bit.
  - Logic errors: A combinational logic circuit may momentarily generate an inaccurate output value due to noise. This brief pulse may turn into a chronic fault if it is "latched" or stored by a flip-flop or memory device.
- Hard errors: These are permanent failures caused by physical damage to the circuit.
  - Electrical Overstress (EOS): An overvoltage or overcurrent incident can result in catastrophic physical harm, like gate oxide punctures or connection melting.
  - Electrostatic Discharge (ESD): An abrupt spike in static electricity can produce strong electric fields or localized heat, which can lead to latent damage that reduces the lifespan of the component or instantaneous device failure.
  - Component failure: A number of failures can result from physical flaws in the component's construction, corrosion, or material deterioration over time.

B. Common errors caused by noise

- Bit Errors: The most basic type of noise-induced error occurs when a single bit's voltage level is changed, leading to an inaccurate reading.
  - Corrupted data: During digital transmission, noise can flip a bit (e.g., changing a '1' to a '0'), leading to incorrect data being received.
  - Logic malfunction: A quick, undesired pulse known as a noise spike may be confused with a clock signal or data pulse, leading to an incorrect value being recorded by a register or an incorrect state change by a logic gate.

- Signal integrity errors: These mistakes arise when noise tampers with the digital waveform's timing or shape, particularly in high-speed systems.
  - Jitter: This is the undesired departure of a digital signal's edges from the optimal time. Jitter can result in bit errors and violations of setup and hold times by causing data to be sampled at the incorrect moment.
  - False switching: A logic circuit may switch when it shouldn't because noise might cause the voltage level on a digital line to momentarily surpass the threshold between a high and low signal.
  - Overshoot and undershoot: Voltage dips and spikes that go beyond the typical high and low levels are referred to as overshoot and undershoot. If severe, these can cause data corruption, interfere with internal memory components like charge pumps, and harm integrated circuits.
- Ground and power-related errors: Noise in the power delivery system can cause widespread issues across a circuit.
  - Ground bounce: This happens when many transistors change states at once. The local "ground" reference may differ from the system's actual ground due to a voltage spike on the ground plane brought on by this abrupt shift in current. False switching and logical mistakes may result from this.
  - Power supply noise: Any component that draws power from a loud power source may be impacted by contaminated or erratic electricity. This may result in resets, clock jitter, or data corruption in delicate parts like memory.
- Communication and bus errors: In multi-chip or board-to-board communication, noise can disrupt the shared bus.
  - Crosstalk: This occurs when an undesirable noise is introduced onto a neighboring trace on a printed circuit board (PCB) by a signal on one trace. The receiving component may view crosstalk as a legitimate signal and record an inaccurate value.
  - Interface corruption: Noise can result in excess, invalid clock pulses on serial communication buses such as SPI or I2C. This could disrupt the transaction and lead to the recipient misinterpreting commands or missing information.
  - Increased bit error rate (BER): Noise raises the BER, or the total number of bit errors over a given period of time, in any data transmission. An excessively high BER may be too much for error correcting systems to handle.
- Memory errors: Storage components, especially volatile memory, are susceptible to noise.
  - Write/erase corruption: In memory devices like flash, noise can interfere with the delicate voltage levels needed for writing or erasing data. This may result in inaccurate data storage or accelerated memory cell deterioration.
  - Intermittent faults: Errors that are difficult to recreate are frequently caused by noise. In certain instances, a component could be held accountable for a malfunction that was actually brought on by outside noise on its communication bus.
- Statistical analysis of noise
  - Power Spectral Density (PSD): PSD can be used to study the frequency domain properties of random noise and display the strength of the noise at various frequencies. This makes it possible to create suitable filters and assists designers in determining which frequency components are the most troublesome.
  - Probability Distribution Function (PDF): The PDF describes the properties of noise in the temporal domain. The amplitude distribution for a large number of noise sources, such as thermal noise, is Gaussian (normal).
  - Statistical modeling: To examine the likelihood of noise-related occurrences, including multiple trap-induced Random Telegraph Noise (RTN) in transistors, simulation tools employ statistical models.
  - Input-referred noise: By computing the total noise at the output and referring it back to the input, this method enables engineers to examine a circuit's noise performance. This aids in locating the system's most important noise sources.

C. Mitigation techniques

- PCB design:
  - Proper grounding: Ground bounce and common-mode noise can be reduced by using solid ground planes and single-point grounding systems.

- Decoupling capacitors: By positioning capacitors near an integrated circuit's (IC) ground and power pins, high-frequency noise can be reduced and a steady power supply can be provided while switching.
- Twisted pair cables: By guaranteeing that each wire in the pair is equally exposed to the interference, twisting signal wires helps eliminate external magnetic noise.

➢ Error detection and correction:
- Error-Correcting Codes (ECC): ECC methods are able to identify and fix burst and single-bit faults in data storage and transmission by adding redundant bits.
- Parity bits: Parity checking, a fundamental technique for identifying single-bit mistakes, adds an extra bit to a data block to show if the number of "1s" is odd or even.

➢ Circuit-level techniques:
- Filtering: Low-frequency noise can be eliminated using high-pass filters, whereas high-frequency noise can be eliminated by low-pass filters.
- Shielding: A circuit can be protected from external electromagnetic interference by utilizing shielded wires or enclosing it in a metallic enclosure.
- Differential signaling: This technique eliminates common-mode noise that equally affects both signal lines by using two signal lines carrying complimentary versions of the same signal.

III. Reliability of Digital Circuits

The capacity of digital circuits to carry out their intended activities accurately under given circumstances and for a predetermined amount of time is known as reliability. This is a crucial consideration for high-dependability applications such as military, aerospace, and medical systems. Reliability issues include radiation-induced faults (SEUs), environmental factors (temperature, dust), hardware failures (dust, dampness), software problems, and aging-related degradations (such as BTI and HCI). Developing precise techniques to calculate failure probability, strengthening circuits against faults, and utilizing virtual validation tools to anticipate and lessen failure modes are all part of evaluating and enhancing dependability.

A. Factors affecting digital circuit reliability

The reliability of a digital circuit is its ability to perform its intended function without failure over a period of time.

➢ CMOS scaling: As transistors get smaller (sub-nanometer scale), noise margins get smaller and components are more susceptible to radiation-induced soft mistakes.
➢ Voltage and temperature: The circuit is more susceptible to disruptions at lower operating voltages because they offer less noise margin. On the other hand, greater temperatures speed up physical wear-out processes like electromigration and increase thermal noise.
➢ Design and layout: Bad PCB design techniques can seriously reduce noise immunity. Examples include inadequate signal routing, a lack of decoupling capacitors, and erroneous grounding schemes that result in ground loops.
➢ Aging effects: Over time, all electronic parts deteriorate. This encompasses phenomena such as Time-Dependent Dielectric Breakdown (TDDB) and Bias Temperature Instability (BTI) in semiconductors.
➢ Manufacturing defects: Early-life failures may result from flaws introduced during manufacture, such as weak connections or vacancies in metallization layers.

B. Physical and Environmental Factors

➢ Temperature: Circuit components can deteriorate and have their lives shortened by excessive or quickly fluctuating temperatures.
➢ Humidity: Wet conditions can lead to corrosion and impair protective film function, which can result in circuit failures.
➢ Electrostatic Discharge (ESD): Components may sustain immediate, irreversible damage from static electricity originating from human bodies or other sources.
➢ Electromagnetic Interference (EMI): Unwanted currents and voltages can be induced by external electromagnetic fields, resulting in temporary operational faults.
➢ Mechanical Stress: Internal damage and open or short circuits might result from physical stress brought on by handling, shipping, or vibration.
➢ Radiation: Single Event Upsets (SEUs) and other temporary malfunctions in semiconductor devices can be brought on by ionizing radiation.

C. Design and Operational Factors

- Electrical Overstress (EOS): Components may sustain instant damage when operating at unreasonably high voltages or currents.
- Aging Effects: Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) are two deterioration processes that transistors experience over time, resulting in increasing gate delays and parameter drifts.
- Component Quality and Design: Reliability is increased by using high-quality components and integrating strong design elements such sufficient heat dissipation and appropriate stackup designs.
- Manufacturing and Assembly Defects: Mistakes made during the manufacturing and assembly process, like loose connections or short circuits, may result in problems right away or later.

D. Software and System-Level Factors

- Software Faults: Software errors that affect the circuit as a whole might be caused by bugs in the CAD tools or by mistakes made during design.
- Fault Tolerance: The probability of system failure rises when fault-tolerant techniques are lacking to manage transitory defects, particularly with contemporary, smaller technologies.

E. Assessing Digital Circuit Reliability

- Functional Reliability vs. Signal Reliability: Functional reliability is unduly pessimistic and assumes that a circuit would fail if there is any problem. A more accurate evaluation is provided by signal reliability, which calculates the likelihood that the circuit will provide the right output signals.
- Probabilistic Methods: To calculate output error probability and overall circuit dependability, methods such as Probabilistic Transfer Matrix (PTM) schemes treat digital circuits as matrices.
- Fuzzy Arithmetic: When it is challenging to gather accurate quantitative data, fuzzy arithmetic can be used to evaluate failure probabilities and dependability for complicated systems with numerous interacting components.

F. Improving Digital Circuit Reliability

- Reliability Enhancement Techniques: These include employing evolutionary algorithms to search the search space for more dependable designs or adding multiplexers at gate inputs to create global VHDL files for simulation.
- In-situ Monitors: By installing monitors inside the circuit, timing violations caused by aging-related degradations can be prevented before they happen and intervention is possible.
- Hardening Circuits: By adding redundancy or other error-detection and correction procedures, circuits are made more fault-resistant for high-reliability applications.
- Virtual Validation: Proactive design modifications are made possible by using simulation tools to evaluate component performance and possible failure modes (such as solder joint fatigue and vibration) earlier in the design process.

G. Analysis and mitigation techniques

In order to guarantee circuit dependability, effective analysis and mitigation techniques are necessary.
Whereas mitigation entails redundancy, error detection and correction (EDAC), and circuit hardening by specifically fortifying weak parts like gates and memory cells, digital circuit dependability is assessed by probabilistic modeling, Monte Carlo simulation, and analytical techniques. Additionally, techniques include design-for-reliability (DfR) best practices, such as derating components and using stress-recovery timing to address aging effects like transistors' Negative Bias Temperature Instability (NBTI).

H. Analysis Techniques

- Probabilistic Modeling: By modeling circuit behavior using a variety of random variables and component values, probabilistic modeling helps to balance cost and robustness by predicting the likelihood of component failure over time.
- Monte Carlo Simulation: According to Cadence Design Systems, Monte Carlo simulation is a popular probabilistic technique that predicts the range of electrical values influencing performance and reliability by using a large number of random component values in simulations.
- Analytical Techniques: For precise dependability evaluation, use mathematical techniques and circuit transformations; these are frequently more effective than simulations for intricate circuits.

- Failure Mode, Effects, and Criticality Analysis (FMECA): FMECA, or Failure Mode, Effects, and Criticality Analysis, is a technique for determining probable failure modes, their causes, and how they affect the circuit's overall performance.

I. Mitigation Techniques

- Triple Modular Redundancy (TMR): To withstand single-point failures, three copies of critical logic are implemented, and a voter determines the appropriate output.
- Fault Tolerance: Designing systems that can continue to operate correctly even when some components are faulty.
- Error Detection and Correction (EDAC): This logic detects and fixes soft errors, or temporary errors, which are frequently brought on by radiation.

J. Circuit Hardening

- Selective Hardening: According to HAL-Pastel, selective hardening reduces cost, power, and space by fortifying only a circuit's most important and susceptible areas.
- Gate Sizing: Adjusting the size of gates to enhance their timing and resilience to soft faults.

K. Design for Reliability (DfR)

- Component Derating: According to the Space Applications Center, component derating is the process of operating electronic components at stress levels (voltage, current, and temperature) lower than those recommended by their manufacturer in order to lower failure rates.
- Stress-Recovery Timing: ResearchGate states that this technique reduces aging effects like NBTI in transistors by putting patterns in place that prevent interface traps from forming.

IV. Conclusion

Noise, transient faults, and error mechanisms resulting from both internal device features and external environmental conditions have a fundamental impact on the reliability of digital circuits. Fault-tolerant design methods are crucial as technology advances to nanoscale regimes because of the increased vulnerability to noise and soft mistakes. Adaptive noise reduction techniques, strong circuit topologies, and efficient error detection and correction are essential for preserving system performance and integrity. Enhancing dependability will require ongoing study on developing materials and low-power, noise-resilient design techniques. In the end, creating reliable digital systems necessitates a comprehensive strategy that combines circuit-level fault tolerance, device-level resilience, and system-level reliability management.

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