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Design and Hardware Development of 7 Level Inverter with Reduced Switches

Vijay Kumar V[1] and Sangeeta Modi[2]
[1-2] PES University/Electrical and Electronics Department, Bengaluru, India
Email: vijaykumar21vj@gmail.com

***Abstract*—Multilevel Inverters have been gaining increased utilization for their applications with PV generation and other renewable resources in smart grid. The main aim of this work is to develop a Seven Level Multi-Level Inverter circuit with reduced switches. Lesser number of power switches will reduce the switching losses and complexity of the system. Power Mosfets are used for the switches as they have better commutation speed and switching efficiency at lower voltage levels. Pulse Width Modulation technique is used to provide the gating signals for the mosfets and a microcontroller is used to generate these pwm signals. LC filters are used to obtain pure sinusoidal output. The proposed inverter focuses on reducing the number of switches used to obtain seven level output which in turn will reduce the number of gate driver circuits required for driving the mosfets. Simulation of the inverter is carried out in MATLAB Simulink. Hardware Model of this inverter circuit is been designed for 24V and the output of the inverter is used to run motor load.**

***Index Terms*— Multilevel Inverters, renewable resources, Pulse Width Modulation, Power mosfet, Gate driver circuit.**

I. INTRODUCTION

An Inverter is a power electronics circuit that changes Direct current (DC) into alternating current (AC).
The renewable energy integration has taken a dominant role in today's electricity market. Due to population growth and technological advancements the need for energy resources have kept on constantly rising and to compensate this demand various types of renewable sources like solar power generation using PV Panels, wind energy and various other methods are being implemented. The power generated from these sources are Direct Current and therefore these systems require an inverter to connect them to the AC loads [1]. The output from the solar panels is generated and stored in batteries which are used as input to these inverters which require a constant DC input and they produce a pulsating square wave or pulsated sinusoidal wave at the output. LC Filters can be connected at these outputs to get pure sinusoidal output which can be further fed to the grid or used to power the loads. The inverters can be both on-grid and off-grid based on their applications. PV generated for domestic loads and household purposes will use off-grid inverters and major solar generation plants where power is generated at higher capacities will use on-grid inverters where the generated output will be fed to the power grid [2].
The basic design of these inverters consists of high-speed switching circuits, which use power switches that switch on and off at a rapid pace thereby making the current to flow in a required manner to convert the DC wave into a pulsating signal [3]. In the latest advancement in designs there are various topology for the design of

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the inverters which are used to address different problems based on the requirements [4]. So, the design of the inverter is considered after analysing the type of loads and various parameters of its purpose.
Multilevel inverters are inverters that operate on high power are used where there are high power usages such as industrial applications. These applications require high power and integrating renewable energy sources for these applications have led to the requirement of multilevel inverters which can operate for higher power and better efficiency compared to two level inverters. Multilevel inverters have many advantages considered to the conventional inverters. They use fewer components which reduces their complexity and makes their design simpler. The power switches that are used in their design have switching speeds that are higher and accurate which also reduces the harmonics in the generated output. This makes the inverter to easily interact with the grid. The output of a multilevel inverter is obtained in multiple steps depending on the design levels thereby making it possible to generate a much nearer to pure sinusoidal output [5]. As the number of levels in a multilevel inverter increases, we can generate better sine waves that have reduced harmonic levels.
In this work we have simulated and developed a hardware model of a cascaded h bridge type seven level inverter [6] with reduced switch topology that has better advantages over conventional inverter design and has higher efficiency and lower harmonics.

II. SYSTEM UNDER CONSIDERATION

The block diagram of the project is represented in figure 1. The main objective of this system is the design of the Seven Level multilevel inverter section in both simulation as well as hardware circuit.
The block diagram depicts the various functional circuit blocks required in the project. The source power supply is basically DC source supplied from a battery or through a converter. Constant DC supply is required for the inverter section. This is obtained from the rectifier and filter section. This section consists of a bridge rectifier and filters through which we get a constant DC output. This output is fed to the seven level mosfet section where the switching takes place and stepped ac output is obtained. The gate drive signals for the mosfet bridge are obtained from the ATmega 328 microcontroller. PWM pulses are obtained from the controller and fed to the optocoupler gate drive circuit to regulate the signal levels to compatible levels to match the required mosfet drive signals. The obtained output is a seven-level stepped AC waveform that can be used as input for loads such as lighting or motor loads.

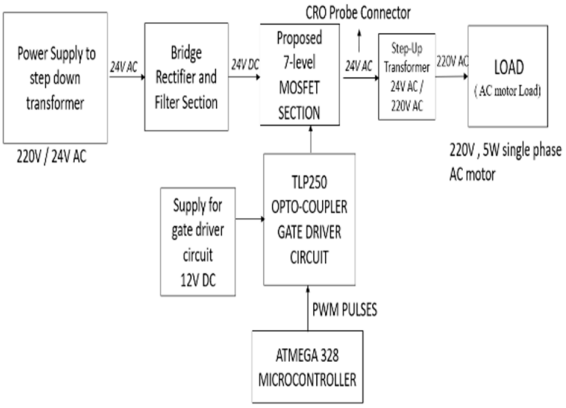

Figure 1: Block Diagram of the system

A. Circuit Configuration of Seven Level Mosfet Section

The figure 2 shows the topology design for the seven-level multilevel inverter. Unlike the traditional H-bridge inverter this multilevel inverter makes use of a reduced number of power switches in the circuit design. This design uses only 8 power switches to produce the seven-level output. As a result, there is reduce in switching losses in the system which makes the design more efficient compared to the conventional h-bridge design. The input dc voltage (Vdc) is given to a capacitive voltage divider circuit where the given voltage input is divided into three voltage levels of Vdc, 2/3Vdc and 1/3Vdc. The divided voltage after passing through the voltage divider is given to the H-bridge circuit of mosfet and diodes. According to the gate pulses provided the circuit path is completed and different levels of output are obtained. This output is given to the output h-bridge from where we obtain the seven-level output.

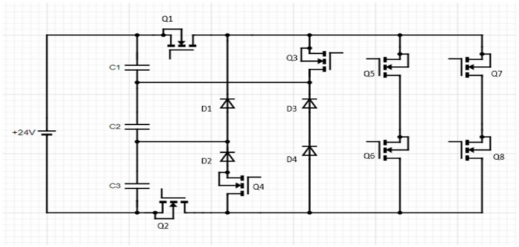

Figure 2: Circuit Diagram of mosfet arrangement

Total number of switches required for conventional H-bridge arrangement:

$N = (M - 1) / 2$ N = Number of H-bridge required

$N = (7 - 1) / 2$ M = Level of the Multilevel Inverter

$N = 3$ (H -Bridge)

Each H- Bridge requires 4 switches. Therefore total 12 switches.

Power Switches required for Reduced h bridge arrangement:

$S = 2 (N - 1) + 4$ S = Number of power switches required

$S = 2 (3 - 1) + 4$

$S = 8$

B. Switching Sequence of the Switches

Table I represents the switching pattern the mosfets operate for various voltage levels. Seven output levels are obtained for each cycle of the input given to the system. Considering an input of Vi, the obtained seven levels will be 0, 1/3 Vi, 2/3 Vi, Vi, -1/3Vi, -2/3Vi, -Vi. For each level the corresponding switches are turned ON according to the sequence table to get the specific level output. When the switch is ON it is represented as 1 and when its OFF it is represented as 0. Based on this switching sequence Arduino code is used to generate the switching pulses.

SWITCH	0 Vi	1/3 Vi	2/3 Vi	Vi	2/3 Vi	1/3 Vi	0 Vi	-1/3 Vi	-2/3 Vi	- Vi	-2/3 Vi	-1/3 Vi
S1	0	1	1	1	1	1	0	0	0	1	0	0
S2	0	0	0	1	0	0	0	1	1	1	1	1
S3	0	0	0	0	0	0	0	0	1	0	1	0
S4	0	0	1	0	1	0	0	0	0	0	0	0
S5	1	1	1	1	1	1	1	0	0	0	0	0
S6	0	0	0	0	0	0	0	1	1	1	1	1
S7	1	0	0	0	0	0	1	1	1	1	1	1
S8	0	1	1	1	1	1	0	0	0	0	0	0

Table I: Switching Pattern of the switches

C. Simulation of the Inverter

The simulation of the inverter is carried out in MATLAB SIMULINK. The input to the mosfet switches is given by pulse generator using PWM technique. The output is connected to the filter section and then the waveforms are obtained for RL load. Switching sequence is used to generate the switching pulses for each mosfet.

Pulse Width = (Switch ON position / Total Number of switching modes) * 100

Phase Delay = (Total Time Instants / Total Number of switching modes) * 0.02

The simulation of the inverter is done in MATLAB Simulink and the output waveform is obtained. The input to the mosfet switches is given by pulse generator using PWM technique. The output is connected to the filter section and then the waveforms are obtained for RL load. The input voltage is considered as 24V DC supply for the system. The gating pulses are generated according to the switching sequence of the mosfets.

The capacitor and inductor for the LC filter is calculated using standard formulas and added to the simulation to remove the unwanted signals and delay during the switching and to obtain a more exact sinusoidal output.

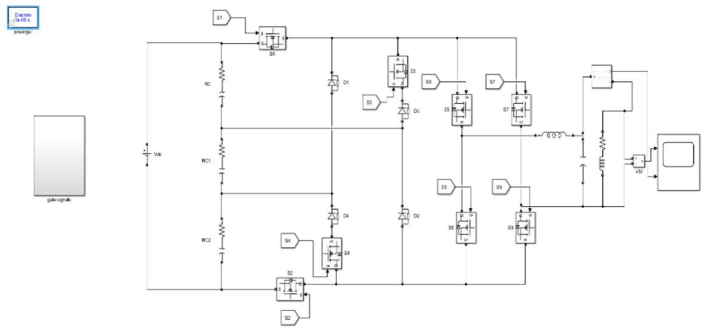

Figure 3: Simulation model of the system

Filter Design for Simulation

$$L = V_{dc} / 4 * \Delta I_L \max * F_{sw} \text{ ----------(1)}$$
$$= 12/ (4* 2*\sqrt{2} *500)$$
$$L = 2.1213 \text{ mH}$$

$$C = (10 / (2* \pi* F_{sw}))2 * (1/L) \text{ ----------(2)}$$
$$= (10 / (2* \pi* 500))2 *(1/ (2.121 *10\text{-}3))$$
$$= 2.389 \text{ mF}$$

where,

Vdc – is the input DC voltage
IL max – is 20 % of rated output current
Fsw – is the switching frequency.

D. Gating Pulses of each MOSFET

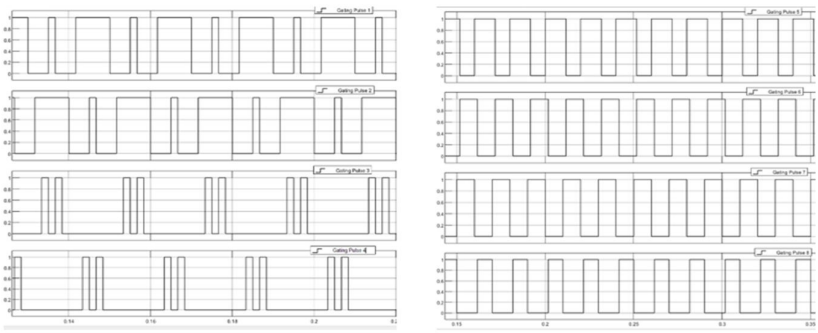

Figure 4: Gate Pulse of each mosfet

The Gate signals for each mosfet is generated using a ATmega 328 microcontroller that is programmed using Arduino board. These signals are generated according to the switching sequence operation of the mosfet switching. A delay of 1200ms is given between each switching operation to observe the step method between each switching state.

E. Simulation Results

The simulation output is obtained for 24V DC input and the seven-level output waveform is obtained. It can be observed that the obtained waveform is stepped at seven different levels and is verified with the theoretical values. The circuit is also simulated with the calculated filter values to obtain a clearer sinusoidal output. The Total Harmonic Distortion of the waveform is calculated and it is observed that the distortions are well inside the permissible limits of international standards <= 5%. This makes the considered design efficient and reliable.

The seven level output waveform obtained in simulation is shown in figure 5. It can be observed that the waveform has seven voltage levels. The highest level in the positive half is 24V and on the negative half is -24V. the other levels are 1/3 Vi, -1/3Vi and 2/3 Vi, -2/3 Vi and a zero level. The THD obtained is 3.09% which is well below the standard permissible limits of 5%.

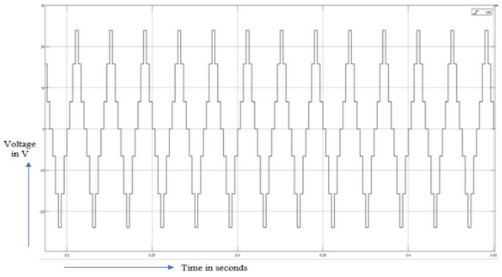

Figure 5: Simulated Seven Level Output Waveform

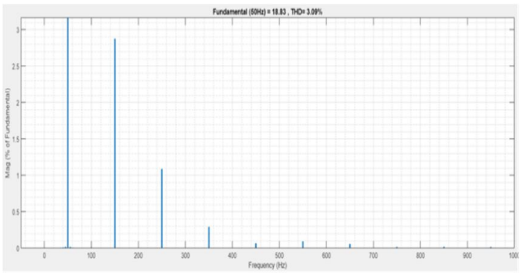

Figure 6: THD analysis of the obtained output

F. Input Supply with Bridge Rectifier

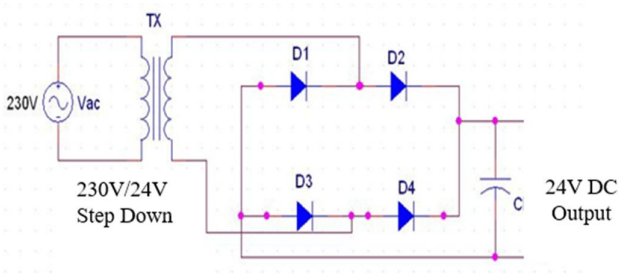

Figure 7: Input transformer with bridge rectifier

The primary supply for the system is given from a step-down transformer of 220/24V which is given to a full wave bridge rectifier which coverts AC to DC. A filter capacitor is connected to reduce ripple factor and increase the rectifier efficiency. The obtained 24V DC is used as the input source for the inverter circuit. The voltage divider circuit in the inverter circuit divides the voltage across the branches and each level is obtained during the operation of the inverter.

G. Gate Driver Circuit

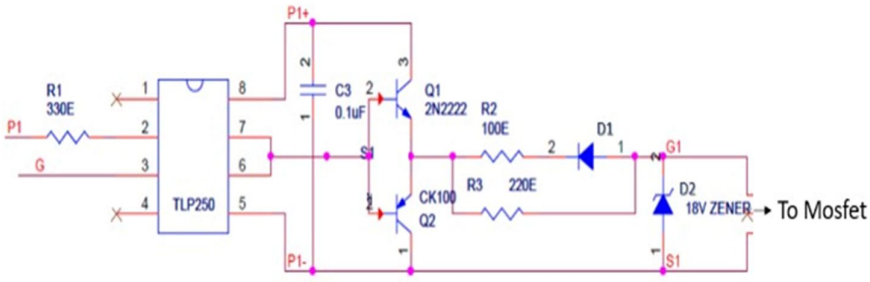

Figure 8: Gate driver circuit

The above circuit is considered for the gate driver circuit that is required to regulate the voltage of the pwm pulses that are generated from the Arduino microcontroller. The pulses generated from Arduino are just 5V and cannot be used to power a mosfet as the voltage required to turn on a power mosfet requires higher voltage of around 9 to 16V. Therefore, this gate driver circuit is used to regulate the voltage to the required level.
The circuit is constructed using a TLP250 optocoupler IC, which is used for designing gate driver circuits for its various advantages. Firstly, it is used to isolate the higher voltage side and lower voltage side in a system and it protects from voltage flowing from higher side to the lower side thereby protecting the components.

H. Hardware Model Developed

The complete hardware setup is mounted on a foundation cardboard as shown in figure 9 where all the working circuits are labelled. The power for the setup is given using adapter for the arduino and regular 230V AC input from the plug in cable in wall sockets for the input step down transformer. The components and the specification list is shown in figure 11.

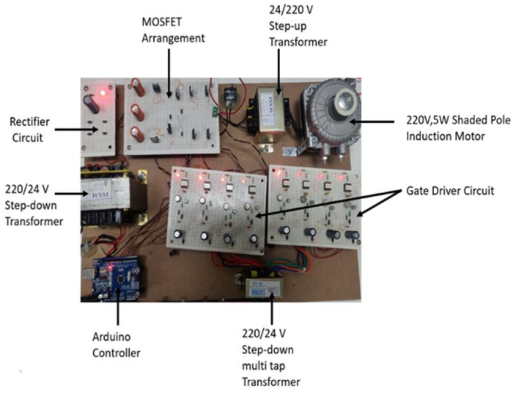

Figure 9: Complete hardware model

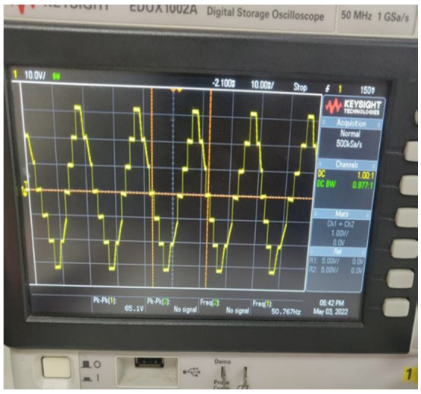

Figure 10: CRO output of Seven-level waveform

SL.no	COMPONENTS USED	RATINGS	QUANTITY
1	Rectifier Diodes	1N4007	16
2	Electrolytic Capacitors	50V, 2200 µF	12
3	IRF840 Mosfet	V_{DSS}= 200V $Vgs_{(th)}$=20V I_D=8A	8
4	TLP250 IC	V_{CC}= 10-35V	8
5	Ceramic capacitors	0.1 µF	8
6	CK100 (BJT)	V_{CBO}=60V V_{CEO}=50V	8
7	2N2222(NPN Transistor)	V_{CBO}=60V V_{CEO}=30V	8
8	Zener Diode	V_Z=18V,0.5W	8
9	AC Induction Motor	220V,5W	1
10	Step up Transformer	24/220KVA	1
11	Step down Transformer	220/24 KVA	1
12	Multi-tapped Step-down Transformer	220/12 KVA	
13	Arduino Controller	ATMEGA328	1
14	Shaded Pole Induction Motor	220V, 5W	1
15	Standard Resistors(Ω)	100,220 Ω	-

Figure 11: Components list and specifications used in hardware

The mosfet section recieves the DC input from the rectifier section and each mosfet recieves gate pulses from individual gate driver circuits. A switch is placed between the inverter output and the output transformer which can be used to run the motor. The inverter produces seven level waveform and the CRO output of the seven level waveform can be taken at this section. The 24V seven level AC output from the inverter is stepped up to 230V using a step-up transformer to run an AC motor load.

The seven-level output obtained from the designed inverter in figure 10 comparatively matches the simulation results output waveform and the theortical values of the levels obtained and it can be effectively used to run AC loads.

The obtained voltage levels in the output waveform is maximum voltage of Vi = 24V

Next step voltage of 2/3 Vi = 2/3 (24) = 16V and -16V in the negative half cycle.

The first step level is 1/3 Vi = 1/3 (24) = 8V and -8V in the negative cycle.

III. CONCLUSIONS

Multilevel Inverters have attained a very significant requirement due to their immense advantages. This work focuses on developing a seven-level inverter with reduced number of power switches used for the design. A total of 8 power mosfet are used in the design with a capacitive voltage divider circuit that drives the inverter section. Pulse width modulation technique is used to provide the gating signals.

Simulation of the proposed seven level inverter model with reduced switches is done for both RL load as shown in figure 5 and the harmonics are calculated as shown in figure6. It can be observed that these reduced switch multilevel inverters are highly efficient as they have lesser switching losses and are simple in construction. They have lower harmonic distortion and provide better performance compared to conventional low level inverters. Hardware model of the proposed seven level inverter with eight mosfet switches is developed as shown in figure 9 and the output is obtained and verified with the simulation output. The obtained output is used to run a variable AC motor load and the operation is observed. Further future developments can be made to utilize multilevel inverters in grid tied inverters to increase the efficiency of the utilization of solar and other renewable resources employed in smart grid.

REFERENCES

[1] G. R. Palaniswamy, Anna Chacko: “Implementation of 7-Level inverter with reduced switches based of grid connected PV system”, International Journal of Electrical Engineering and Technology, Vol. 11, Issue 03, May 2020.

[2] Subhashree Choudhury, Mohit Bajaj, Taraprasanna Dash: “Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects”, MDPI journal, September 2021.

[3] Mahammed Sameer m Attar: “single-stage five level inverter for grid connected (PV) system”, International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering, volume 3, special issue 2, 2016.

[4] Hulsi Karaca: “Analysis of A Multilevel Inverter Topology with Reduced Number of Switches”, Book of Transactions of engineering technologies, pp 41-52, January 2014.

[5] Muhammad Salman, Abdul Basit, Aemal Ahmad: “Modeling of Cascaded H-Bridge Multi-level Inverter Having Low Total Harmonic Distortion”, International Journal of Engineering Works, Vol. 6, Issue 03, March 2019.

[6] Abhil T Balakrishnan, Alan James, Jibson Thomas Job,Ayona Thomas: “Seven Level Inverter”, International Journal of Engineering Research & Technology (IJERT), Vol. 6 Issue 04, April-2017.

[7] Nurul Aisyah Yusof, Norazliani Md Sapari1, Hazlie Mokhlis: “A Comparative Study of 5-level and 7-level Multilevel Inverter Connected to the Grid”, IEEE International Conference on Power and Energy, December 2012.

[8] Dr. R. Arulmozhiyala, Dr. M. Murali, and K.R. Manjeri: “Design and Analysis of 7 Level Multilevel Inverter for Industrial Applications”, Journal of computer and mathematics education, April 2021.

[9] Niraj vijayshankar mishra, Keval mahyavanshi, Amitkumar Gautam: “single-phase five-level symmetrical cascaded h-bridge multilevel inverter with reduces number of switches”, International Journal of creative research thoughts, April 2020.

[10] N. Srinivas, S. Singh, M. Gowda, C. Prasanna and S. Modi, "Comparative Analysis of Traditional and Soft Computing Techniques of MPPT in PV Applications," 2021 IEEE 4th International Conference on Computing, Power and Communication Technologies (GUCON), 2021, pp. 1-6, doi: 10.1109/GUCON50781.2021.9573876.

[11] Nirupama P Srinivas, Sangeeta Modi, "Pole-to-Pole Fault Detection Algorithm Using Energy Slope for Microgrids", 2022 International Conference on Electronics and Renewable Systems (ICEARS), pp.288-294, 2022.

[12] N. Srinivas and S. Modi, “A Comprehensive Review of Microgrid Challenges and Protection Schemes”, SPAST Abs, vol. 1, no. 01, Oct. 2021.

[13] Nirupama P Srinivas, Sangeeta Modi."A Memory Based Current Algorithm for Pole-to-Pole Fault Detection in Microgrids", Volume 10, Issue V, International Journal for Research in Applied Science and Engineering Technology (IJRASET) Page No: 365-377, ISSN 2321-9653, www.ijraset.com

[14] Durgaprasad S., Nagaraja S., Modi S. (2022) HVDC Fault Analysis and Protection Scheme. In: P. S., Prabhu N., K. S. (eds) Advances in Renewable Energy and Electric Vehicles. Lecture Notes in Electrical Engineering, vol 767. Springer, Singapore. https://doi.org/10.1007/978-981-16-1642-6_18