

High-Performance Turbo Coder Design using MAP Algorithm and Gating Technology for Error Correction in Communication Systems

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Abstract—This paper proposes a novel Very Large-Scale Integration (VLSI) design for the Turbo decoder, a popular communication tool to achieve optimal data reception with minimal errors. The Turbo decoder includes SISO decoders, interleavers, and deinterleavers, which use the Maximum-a-Posteriori (MAP) algorithm to reduce the number of iterations required for decoding. Additionally, the encoder part uses two Recursive convolutional encoders and a pseudorandom interleaver to enhance the error correction capability of the Turbo code. The paper also suggests using clock gating technology to improve the decoder's performance by selectively activating specific blocks based on the decoding performance. The proposed Turbo decoder is designed in Xilinx Vivado 2018.3 achieves high performance and provides a scalable and efficient solution for implementing Turbo decoders in communication systems.

Index Terms—Turbo Coder, Recursive Convolutional Encoders, Interleaver, MAP, SISO Decoder.

I. INTRODUCTION

As the demand for high-speed data transmission and reliable communication systems continues to grow, the need for effective error correction techniques becomes increasingly crucial. Turbo codes have emerged as a popular choice for their high error correction capability, which is essential for ensuring optimal data reception with minimal errors. However, implementing Turbo codes in communication systems can be challenging due to their complexity and high computational requirements. To address these challenges, the paper proposes a novel VLSI architecture for the Turbo decoder, which includes SISO decoders, interleavers, and deinterleavers employing the MAP algorithm. This method greatly lowers the number of decoding iterations necessary, improving system effectiveness and lowering processing demands. A system with two Recursive convolutional encoders and a pseudorandom interleaver is also suggested in the paper to improve the Turbo code's capacity to repair errors. The paper's contribution is significant as it proposes an efficient and scalable solution for implementing Turbo decoders in communication systems. Moreover, the paper suggests using clock gating technology, which selectively activates specific blocks based on the decoding performance, further improving the decoder's performance and power consumption. The proposed VLSI architecture can achieve high performance while overcoming the challenges associated with Turbo codes, making it a practical solution for implementing Turbo decoders in communication systems. The proposed VLSI architecture for Turbo decoders addresses the challenges associated

with Turbo codes' complexity and high computational requirements. The approach provides a scalable and efficient solution for implementing Turbo decoders in communication systems while achieving high performance and reliability. The paper's contribution is significant, as it presents a practical solution that can help to improve data transmission quality and reliability in communication systems.

II. LITERATURE REVIEW

Deepa et al. evaluated the impact of optimizations made to the architecture and algorithm levels on power usage and throughput in their article [1], where they examined the primary functional components of the turbo decoder. The authors utilized two recursive convolution encoders and an interleaver to form turbo encoders, with RSC encoders being preferred due to their low-weight parity codes over conventional convolutional encoders [2]. Kesari et al. investigated both serial and parallel computing techniques of turbo coders [3]. The article [4] presents a detailed analysis of the design and implementation of the proposed architecture and demonstrates its effectiveness in achieving high throughput and low power consumption. While authors in [5] modeled and synthesized various Turbo decoder output variants using XILINX-ISE 12.4i, the authors in [6], reported the design and implementation of a Page 2 memory-reduced Turbo decoder on the field programmable gate array (FPGA) in the LTE-Advanced standard. A clock gating method is suggested by Naim et al. for both the turbo encoder and decoder. The simulation results presented in the research demonstrate the efficiency of the suggested method in lowering power consumption in both the encoder and decoder [7]. A novel dynamic clock gating method is presented by Silvino et al. [8] that dynamically modifies the gating signal in response to the decoder's activity. The study demonstrates how the suggested method can drastically cut power usage while retaining good decoding efficiency. Al-Bahadili et al. provide a clock gating and parallelism-based design methodology for low-power turbo decoders. The research offers a clock-gating approach that preserves decoding efficiency while utilizing the parallelism built into turbo decoding [9]. In order to save energy, the authors of [10] suggest a unique clock gating mechanism that gates the clock signal to the interleaver memory's address generator during the feedback decoding stage. The simulation findings in the research demonstrate how the suggested technique effectively lowers power consumption without compromising decoding performance.

III. THE DESIGN OF A TURBO CODER

A Turbo encoder and decoder make up the Turbo coder architecture in Figure 1. Two identical Recursive Convolutional Encoders (RSC) plus a pseudorandom interleaver make up the Turbo encoder in Figure 2. In LTE, a turbo code with a 1/3 rate parallel concatenation is used. Two separate sets of data are processed by each RSC: the first encoder receives the original data, while the second encoder receives the input data in an interleaved fashion. The data bits are scrambled by the Interleaving method using a predetermined algorithm. When in use, the interleaving method significantly affects how well the decoder functions. As demonstrated in Figure 2, the Turbo encoder produces a 24-bit output using the systematic input, the RSC1 and RSC2 encoder outputs, and the Turbo encoder's output. According to the typical turbo decoder block diagram in Figure 3, this output is sent across the channel to the Turbo decoder, which is made up of two modules of SISO decoders, two pseudorandom interleavers, and a pseudorandom deinterleaver. Commonly used for deciphering turbo codes is the BCJR algorithm. The turbo decoding technique is based on an iterative process between the two SISO component decoders. The decoder pair refines and improves its estimation of the original information bits concurrently. The convolutional code generated by the first or second CE is decoded by the first and second SISO decoders, respectively. One cycle of the first component decoder followed by a pass of the second component decoder is referred to as turbo-iteration.

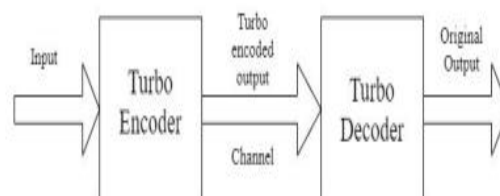


Figure 1. Block diagram for Turbo Coder

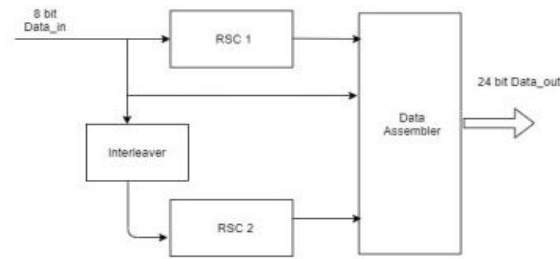


Figure 2. Turbo Encoder

A. Recursive Convolutional Encoders

Recursive Convolutional Encoders (RSCs) are used in the Turbo Encoder, which is a critical part of the Turbo Code. The RSC encoder is a type of Convolutional Encoder that generates the parity bits by performing a recursive convolutional encoding of the input data. The Recursive Convolutional Encoder is essentially a finite state machine that encodes the input data stream into a code stream. The state machine has a number of internal states, and the current state of the machine determines how the input data is transformed into the output code stream. The encoder has a set of feedback connections that allow it to perform recursive encoding of the input data. The function of the Recursive Convolutional Encoder is to take a stream of input bits and produce an encoded output stream that has additional redundant bits. The encoded output stream is designed to have certain properties that make it easier to detect and correct errors in the data. These properties include low cross-correlation, good distance properties, and good interleaving properties. In the Turbo Code, two identical Recursive Convolutional Encoders are used in the Turbo Encoder. One encoder takes the original data stream as input, while the other encoder takes an interleaved version of the input data. The output of the two encoders is combined to form the encoded output stream. The use of two Recursive Convolutional Encoders in the Turbo Encoder, along with interleaving, allows the Turbo Code to achieve excellent error correction performance. The Turbo Code is capable of correcting errors that would be impossible to correct with a single Convolutional Code of the same rate.

B. SISO Decoders

"Soft-Input Soft-Output" or SISO refers to a particular kind of decoder used in turbo coding. An error-correction method called turbo coding is used in communication networks to enhance the accuracy of data transmission by lowering mistakes. By decoding the received signal and giving the soft decision information to the subsequent iteration of decoding, SISO decoders play a significant part in turbo coding. On the basis of the received signal and the a priori knowledge, the SISO decoder calculates the probability of each potential value of the information bits. The information that has already been deciphered by the decoder is known as a priori information, and it is supplied back to the decoder to help with further decoding. The SISO decoder decodes the data bits utilizing the Maximum-a-Posteriori (MAP) technique. The MAP approach calculates the likelihood of each potential value and then chooses the information bit with the highest likelihood. This step is repeated iteratively by the algorithm until an acceptable level of error correction is reached. The SISO decoder can speed up decoding and decrease latency by using the MAP algorithm to cut down on the number of iterations needed to decode the data bits. As a result of fewer iterations, power consumption is reduced and performance is enhanced. Better error correction performance can be attained by the turbo coder with fewer iterations and less power consumption by utilizing the MAP algorithm in the SISO decoder, which is crucial in portable devices with limited battery life.

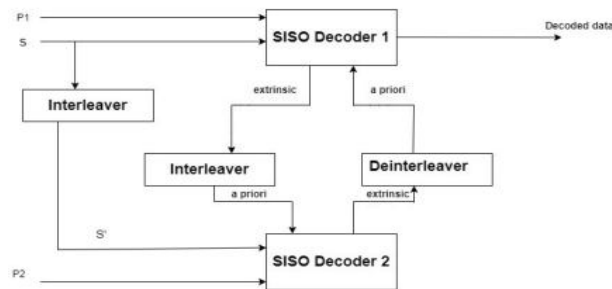


Figure 3. Turb Encoder

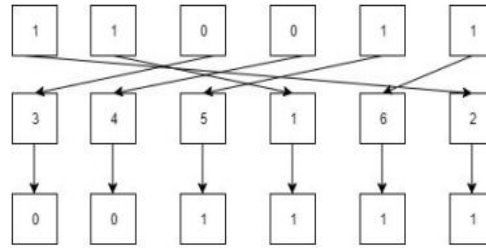


Figure 4. Pseudo-Random Interleaver

C. Interleaver & Deinterleaver

Interleaving and deinterleaving are important processes in turbo coding. Interleaving is the process of rearranging the input bits before encoding to minimize the impact of burst errors during transmission. Deinterleaving is the reverse process, which restores the original order of the bits at the receiver end. Interleaving is typically done using a pseudorandom interleaver, which generates a sequence of addresses that determine the new order of the bits. The pseudo-random nature of the interleaver is important to ensure that the interleaved bits are uniformly distributed, which helps to mitigate the effects of burst errors during transmission. The interleaved bits are then fed to the turbo encoder. At the receiver end, the received bits are first deinterleaved to restore the original order. This is important because the SISO decoders assume that the bits are arranged in a specific order. After deinterleaving, the SISO decoders perform softinput soft-output decoding to recover the original message. Deinterleaving is typically done using the same pseudorandom interleaver as used in the encoder but with the inverse sequence of addresses. This ensures that the original order of the bits is restored. The interleaver and deinterleaver circuits are typically implemented using memory and address generators. These circuits need to be fast and efficient to minimize the decoding delay and increase the throughput of the system.

IV. EXISTING METHODOLOGY

The Viterbi decoder is a frequently employed technique in the context of turbo coding for LTE (Long-Term Evolution) applications. The Viterbi decoder satisfies the criteria needed for LTE systems' error correction and decoding to operate well. It's crucial to keep in mind, nevertheless, that using Viterbi decoders can raise certain security issues. As there is only one convolutional encoder used by the Viterbi decoder, there may be security flaws. The security and robustness of the system are improved by the use of two recursive systematic convolutional (RSC) encoders in turbo decoders. An additional layer of defence against Page 4 potential attacks is provided by the dual-encoder architecture found in turbo decoders, which also assures a more secure communication system. Turbo decoders are able to offer better security features since they have two RSC encoders included. Parallel encoding of the data results in redundant information that can be used for error-correction. This redundancy makes it possible to identify and fix faults made during transmission, improving the communication system's overall dependability and integrity. As a result, using turbo decoders, which have a dual RSC encoder design, gives better security than using Viterbi decoders. Turbo decoders are more resistant to possible threats due to their increased redundancy and error correction capabilities, offering a more secure communication environment for LTE applications.

TABLE I. SYNTHESIS OF EXISTING METHOD

Parameters Analysed	Simulation Results
Board Used	xc7a15tcpg236-1
Power	238 mW
Delay	5.509 ns
Power Delay Product	1.311 mJ

The current approach of turbo coding utilizes 276 look-up tables (LUTs) for its implementation while consuming 238 milliwatts of device power. The delay in processing data for this method is 5.509 nanoseconds, and the power delay product, which represents the total energy consumption of the system, is 1.311 milli Joules. These

performance metrics offer valuable insights into the efficiency and effectiveness of the existing turbo coding method.

V. PROPOSED METHODOLOGY

By regulating the clock signal to flip-flops, clock gating is a power-optimization technique used in digital circuits to lower power usage. The fundamental building blocks of synchronous digital circuits are flip-flops, which are employed to store binary data. Clock gating involves inserting a clock gate between the flip-flops and the clock signal. A control signal is used to enable or disable the clock signal's ability to pass through the clock gate and reach the flip-flops. The flip-flops get the clock signal through the gate when the control signal is active, and the flip-flops stop switching when the control signal is dormant. Clock gating can be employed in different ways to optimize power consumption. One common way is to use clock gating in idle cycles, where the circuit is not performing any operation. In this case, the clock signal to the flip-flops is blocked during idle cycles, and the flip-flops are put into a low-power state, reducing the overall power consumption of the circuit. In the case of SISO decoders with MAP algorithm, clock gating can be employed by inserting a clock gate between the clock signal and the MAP unit. The control signal can be generated by a power management unit, which monitors the activity of the circuit and activates or deactivates the clock gate accordingly. By using clock gating in SISO decoders, power consumption can be significantly reduced, while maintaining the performance of the decoder.

VI. RESULTS & DISCUSSIONS

Xilinx Vivado 2018.3 was used to create the Turbo Coder. Obtaining the recommended methodology's RTL schematic and output simulation waveform. Analyzed and contrasted variables such as area utilization, device power, delay, and the power delay product of the proposed and existing work.

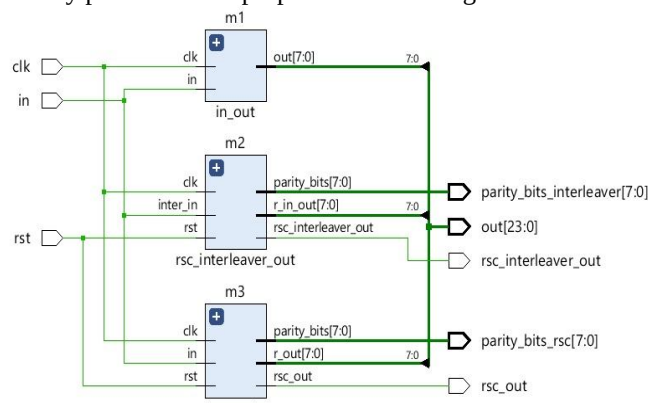


Figure 5. RTL Schematic of Turbo Encoder

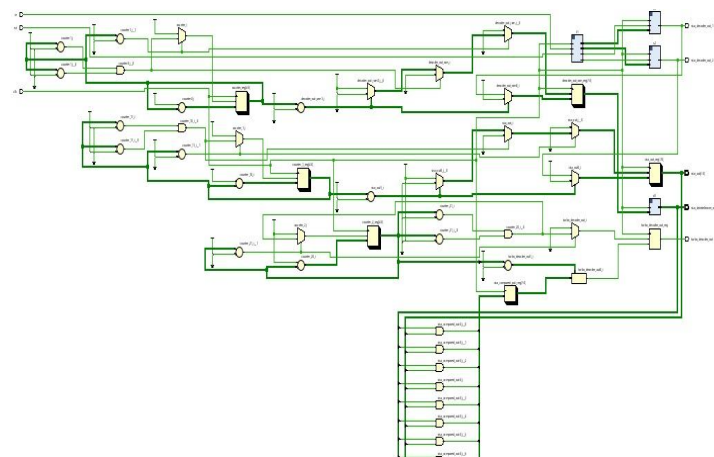


Figure 6. RTL Schematic of Turbo Decoder

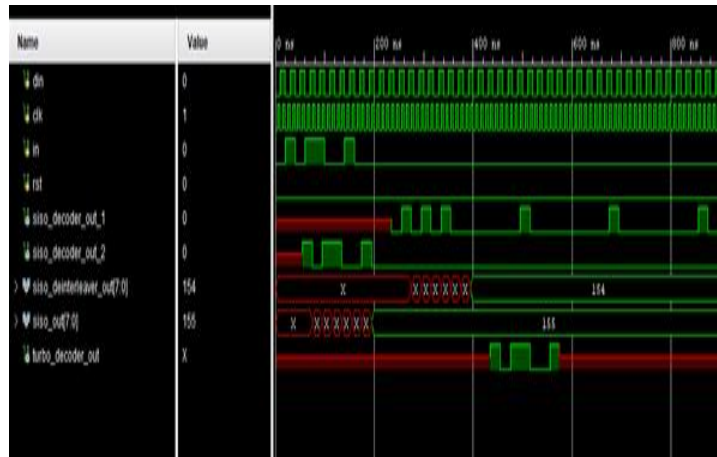


Figure 8. Simulation of proposed Turbo Coder

TABLE II. SYNTHESIS OF THE PROPOSED METHOD

Parameters Analyzed	Board Used		
	xa7a15tcsg324-1L	xc7a25ticsg325-1L	xc7a25ticpg238-1L
Power	218 mW	129 mW	168 mW
Delay	5.208 ns	5.099ns	5.072 ns
Power Delay Product	1.135 mJ	659.57 pJ	853.056 μ J

Here, we examine the power, delay, and power delay product (PDP) of various boards whose performance characteristics differ noticeably from one another. The circuits' power consumption ranges from 129 mW to 218 mW, with the circuit with the greatest power consumption having the highest power consumption. This shows that, in comparison to the other two circuits, the circuit with the highest power consumption requires more energy to run. The circuits' delays range from 5.072 to 5.208 nanoseconds. The fact that the delay of the circuits is comparatively similar despite a few minor changes suggests that the circuits have similar processing speeds. The circuits' PDP values vary considerably. The circuit with the highest power consumption has the highest PDP value, while the circuit with the lowest PDP value has the lowest PDP value. This shows that among the three circuits, the one with the lowest power use is the most energy-efficient. In general, the selection of a circuit design for a given application is based on the application's unique needs, such as power consumption, processing speed, and energy efficiency. Even if a circuit with a reduced power consumption may be more energy-efficient, the processing speed may suffer as a result. A circuit with higher power consumption, on the other hand, can offer a faster processing speed but will need more power. To create a circuit that fits the needs of the application, circuit designers must therefore balance power consumption, processing speed, and energy economy.

VI. CONCLUSION

In this research, we introduced a Verilog HDL-based Turbo coding and decoding architecture. We used clock gating techniques to further improve the circuit's performance, which produced improved simulation outcomes. The MAP method is used by our decoder to determine the most likely piece of sent data, which lowers the number of iterations needed for process decoding. We were able to extract the original message and repair the problems. For synthesis and simulation, we used Xilinx Vivado 2018.3, and the outcomes were tabulated. We examined the simulation data to verify the effectiveness of our suggested circuit. Our circuit's advancements make it ideal for use in contemporary communication systems, where precision and fast Page 6 throughput are crucial. Our system provides an effective and dependable method for error correction in data transmission because it combines a turbo encoder and decoder, clock gating techniques, and the MAP algorithm

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