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Power Reduction in Ripple Carry Adder Circuit using SAPON and LCNT Techniques

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***Abstract*— Ripple carry adders, however simple in design, retain precious operations that make them a necessary tool in the world of digital circuits. These adders find their place within the core of processors and Arithmetic Logic Units (ALUs), effortlessly performing essential computation operations with precision and reliability. Ripple carry adders exhibit commendable power efficiency, ensuring optimal energy utilization in digital circuits. With their streamlined design and efficient operation, these adders minimize power consumption, making them a smart choice for energy-conscious applications where every watt counts. Two cutting-edge techniques are opted to enhance the power efficiency of the ripple carry adder: Leakage Control NMOS Transistor (LCNT) and Stackly Arranged low Power ON transistor (SAPON). Less power is needed in the LCNT approach by making the route between the supply voltage (VDD) and the GND (ground) more resistive. During the changeover step, SAPON avoids leakage current from a short circuit. The power consumption is reduced in RCA circuit using low power reduction ways like LCNT, SAPON. These circuits are dissembled in the cadence tool with 45nm technology.**

***Index Terms*— Ripple carry adder (RCA), Full adder (FA), Arithmetic Logic Unit (ALU), Leakage Control NMOS Transistor (LCNT), Stackly Arranged low Power ON transistor (SAPON), Very Large-Scale Integration (VLSI).**

I. INTRODUCTION

A Ripple Carry Adder (RCA) is a digital circuit used in the field of computer engineering and digital electronics to add two binary numbers together. It's an important component in the design of arithmetic circuits and is widely used in microprocessors, digital signal processors, and other digital systems. In terms of utilization, RCAs are commonly used in Arithmetic Logic Units (ALUs), which are responsible for performing arithmetic and logical operations in microprocessors. Modern digital design must take power reduction in Ripple Carry Adders (RCAs) into account, especially for low power-consumption systems and mobile devices. Although RCAs are simple, they have the drawback of using a lot of power because of the way each bit depends on the carry propagation from the bit before it. The importance of Ripple Carry Adders lies in their simplicity and efficiency while they can be power-hungry. The techniques like SAPON and LCNT are used to reduce power consumption in RCA circuits.

A novel RCA circuit was created using SAPON and LCNT techniques after a study of the power usage in a

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conventional RCA circuit. As soon as we added SAPON and LCNT methods, it is observed that the average power consumption in RCA decreased. The least power was consumed by SAPON, as opposed to LCNT, more preferred. The paper's summary follows: Section II gives a review of the literature, and Section III details power-consuming elements.
RCA is covered in Section IV, whereas Section V discusses strategies for reducing power usage. The analysis and simulation results from the Cadence tool are illustrated in Section VI. The conclusion of the work is depicted in Section VII.

II. Literature Survey

This paper [1] adopted Transistor leakage current control methodology and Viterbi decoder utilizing a sleepy keeper method. This paper has [2] to understand the relevance of the proposed SAPON method in low-power VLSI, LECTOR, LCNT, and The STACK ONOFIC techniques were compared with the proposed SAPON technique [2]. The findings revealed that [2] SAPON consumes less power than traditional reduction strategies. This paper [3] opted for the Dynamic comparator design technology to perform on Gate Overlap Tunnel FET. This methodology was Transistor ON-OFF control. Pass transistor & transmission gate logic and Transistor count reduction were the technology and methodology of this paper [4] where hybrid 1-bit full adder was the main application.

III. Sources Of Power Consumption

The Average power dissipation observed in VLSI circuits dissipate power both statically and dynamically.

A. Static Power Dissipation

The power used when a circuit is not working, or you may say when it is in an inert state, is known as static power dissipation. The circuit will still use some power, referred to as "Stationary Power Consumption," in the existence of a force voltage, even if the clocks are removed and the circuit's inputs are left same.

B. Dynamic Power Dissipation

The device’s power dissipation occurs when it is in use, meaning we have provided supply voltage, a clock, and altered the inputs, dynamic power consumption is the amount of energy used.

C. Switching Power Dissipation

This is due to the output capacitance and other parasitic capacitors, which are part of the overall load and are charged and discharged, are to blame for this. The dissipation of switching power is what we can refer to at an extremely high degree [5].

$$P_{switch} = \alpha*(V_{dd})^2*C*f \qquad (1)$$

where α = switching activity, Vdd = supply voltage, C = load capacitance, f = frequency of operation

D. *Short-Circuit Power Dissipation*

A short-circuit channel from VDD to GND will occasionally occur within the pull-up or pull-down network [6] as some transistors switch "ON" concurrently for a period of time as the input voltage changes slowly.

$$P = I_{mean} *V \qquad (2)$$

IV. Full Adder (FA) And Ripple Carry Adder (RCA)

A. Full Adder

A full adder adds three inputs in total and generates two outputs. A and B make up the first pair of inputs, and C-IN makes up the third, which is an input carry. The characters S, which stand for “usual output,” stand for “sum,” whereas the letters “C-OUT" stand for “what you carry” [7]. The creation of a full adder logic that can merge eight inputs into a byte-wide adder. Every time a bit to carry-in is available, we must employ a full adder because a half-adder cannot accept it. Three operands are added by a 1-bit full adder, yielding output in 2-bits.

B. Ripple Carry Adder

The ripple carry adder is constructed by a series of linked full adders, it is a circuit that uses combinational logic to add two n-bit binary values. Two 4-bit numbers that are binary are added using a 4-bit RCA. Two N-bit numbers that are binary are added using N-bit RCA. For combining Its circuit requires n full adders to handle the two n-bit

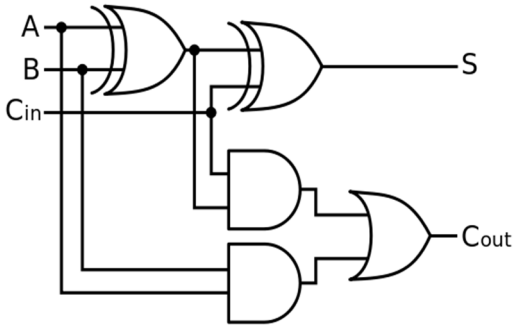

Fig. 1 Full Adder

binary values. It is also known as a “n-bit parallel adder” [8]. Each FA outputs a carry-out and a sum bit after accepting a carry-in as input. An FA’s carry-out functions serve as carry-in for its neighbouring most important FA. The FA is activated when carry-in is made accessible.

The two four-bit binary values (A and B) and the carry-in (Cin) must be thought of in all possible combinations in order to build the truth table for a four-bit ripple carry adder (RCA). For each combination, the sum (S) and carry-out (Cout) must be determined. Since we are working with four-bit values, there are 16 different input configurations that might be used.

Let's represent the four-bit numbers A and B as A[3:0] and B[3:0], respectively, where A[3] is the most significant bit (MSB), and A[0] is the least significant bit (LSB).

The truth table for the four-bit Ripple Carry Adder is as follows:

TABLE.II TRUTH TABLE FOR RIPPLE CARRY ADDER

A[3:0]	B[3:0]	Cin	Sum[3:0] (Result)	Cout
0000	0000	0	0000	0
0000	0000	1	0000	0
0000	0001	0	0001	0
0000	0001	1	0001	0
0000	0010	0	0010	0
0000	0010	1	0010	0
0000	0011	0	0011	0
0000	0011	1	0011	0
0000	0100	0	0100	0
0000	0100	1	0100	0
0000	0101	0	0101	0
0000	0101	1	0101	0
0000	0110	0	0110	0
0000	0110	1	0111	0
0000	0111	0	0111	0
0000	0111	1	1000	0

… (continue for all 16 combinations)

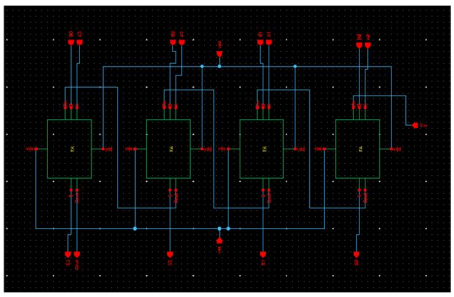

Fig.2 Ripple Carry Adder

V. Proposed Techniques

A. Lcnt

Leakage control in NMOS (N-channel Metal-Oxide-Semiconductor) transistors is a crucial component of CMOS (Complementary Metal-Oxide-Semiconductor) technology for lowering power consumption and improving the overall efficiency of integrated circuits. cnt

NMOS transistors have a specific leakage current known as sub threshold leakage, which occurs when the transistor is in the OFF state but still has some small current flowing between the drain and source terminals due to the presence of carriers in the channel region. Sub threshold leakage is a significant contributor to static power consumption, which is power consumed by the circuit when it is in a quiescent state or not actively switching. In contemporary CMOS design, a number of strategies are used to control leakage current in NMOS transistors.

A different NMOS is positioned after the pull-down portion of the LCNT, a strategy for decreasing leakage current power. This lowers loss of electricity. It is an autonomous NMOS transistor, therefore no extra external input is needed. To the NMOS, only the output provides feedback [9].

B. Sapon

It appears to be referring to a particular approach used in digital circuit design to lower power consumption in CMOS (Complementary Metal-Oxide-Semiconductor) technology. In order to lower the threshold voltage and hence reduce operating power consumption, the technique involves stacking many transistors in series. Stacking Transistors: The gate-source voltage (VGS) applied to the combined stack of transistors can be efficiently increased by stacking several transistors (NMOS or PMOS) in series. The effective threshold voltage of a stack of transistors is larger than that of a single transistor because the threshold voltages of the transistors in the stack add together.

Two [2] Reduced resistance between the supply voltage (VDD) and GND (ground) is achieved by using leakage-control transistors connected externally to the logic. This prevents current leakage during the changeover process due to short circuits. Additionally connected in series are CMOS SAPON transistors in order to limit below-threshold current loss during the levelling phase across the power voltage (VDD) and the negative terminal (ground).

VI. Analysis And Results

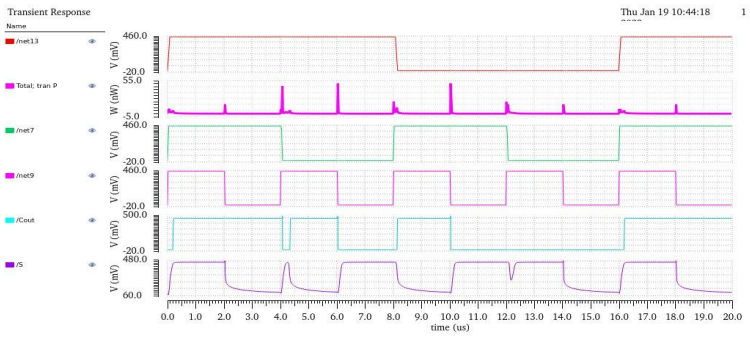

Fig. 3 Transient analysis of FA

Fig. 3 explains about of FA in which, net 7, net 9, net13 are inputs with 1,1,1 and it produces output sum(S) as 1 and Carry output(net13) as 1 and Total tran P is output Power.

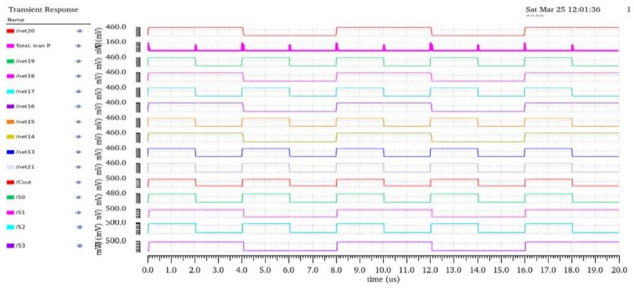

Fig. 4 Transient analysis of RCA

Fig. 4 explains about of RCA in which, net 12, net 13, net14, net15, net16, net17, net18, net19, net20(Cin) are inputs with 1,1,1,1,1,1,1,1,1 and it produces output sum(S0 S1 S2 S3) as1111 and Carry output(Cout) as 1 and Total tran P is output Power.

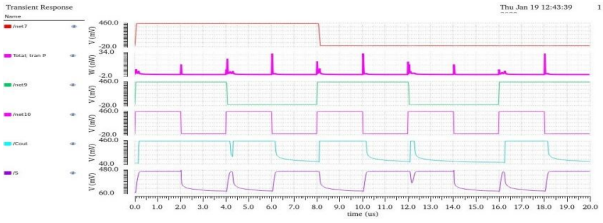

Fig. 5 Transient analysis of lcnt FA

Fig. 5 explains about of lcnt FA in which, net 7, net 9, net10 are inputs with 1,1,1 and it produces output sum(S) as 1 and Carry output(Cout) as 1 and Total tran P is output Power.

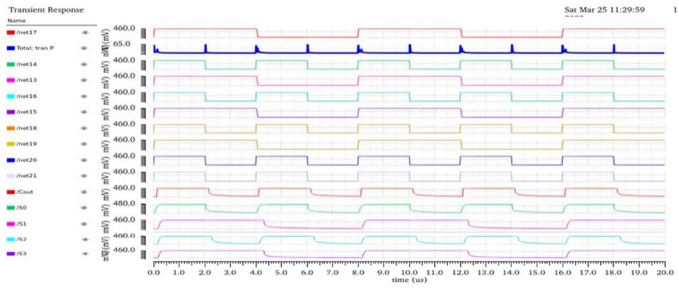

Fig. 6 Transient analysis of lcnt RCA

Fig. 6 explains about of lcnt RCA in which, net 13, net14, net15, net16, net18, net19, net20, net21, net17(Cin) are inputs with 1,1,1,1,1,1,1,1,1 and it produces output sum(S0 S1 S2 S3) as1111 and Carry output(Cout) as 1 and Total tran P is output Power.

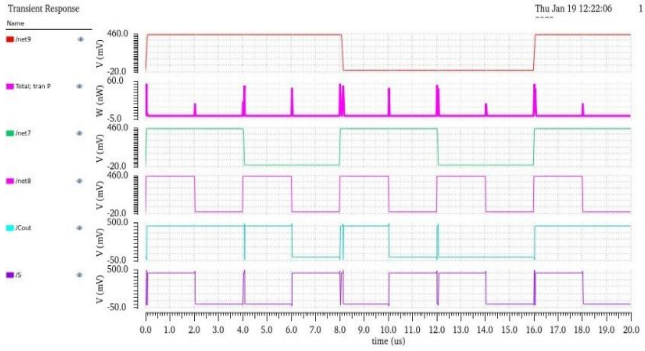

Fig. 7 Transient analysis of sapon FA

Fig. 7 explains about of sapon FA in which, net 7, net 8, net9 are inputs with 1,1,1 and it produces output sum(S) as 1 and Carry output(Cout) as 1 and Total tran P is output Power.
Fig. 8 explains about of sapon RCA in which, net 13, net14, net15, net16, net19, net20, net21, net26, net18(Cin) are inputs with 1,1,1,1,1,1,1,1,1 and it produces output sum(S0 S1 S2 S3) as1111 and Carry output(Cout) as 1 and Total tran P is output Power.

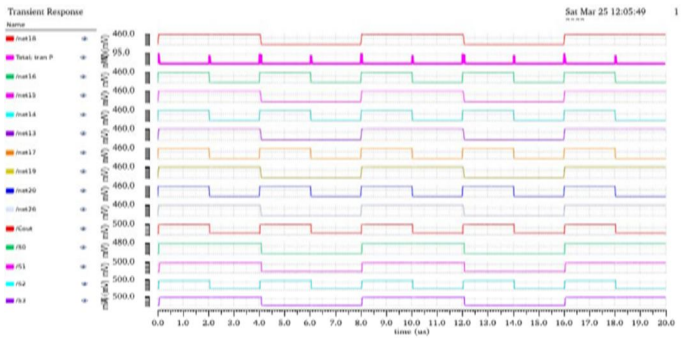

Fig. 8 Transient analysis of sapon RCA

TABLE.1 COMPARISON OF POWER CONSUMPTION OF FA AND RCA

Logic gates	CMOS	LCNT	SAPON
FA	**394.2E-12**	**417.2E-12**	**320.6E-12**
RCA	**643.4E-12**	**1.355E-9**	**617.4E-12**

VII. CONCLUSION

In this paper novel approach for the power consumption in Ripple Carry Adders can be effectively reduced using the LCNT and SAPON techniques. Through the implementation and simulation of various Ripple Carry Adder designs, it has been demonstrated that both techniques contribute to significant power savings compared to conventional architectures.
Overall, the research highlights the potential of LCNT and SAPON techniques for power-efficient Full Adder and Ripple Carry Adder implementations. These techniques offer effective strategies to mitigate power consumption. The findings from this study can guide future research and development efforts in designing energy-efficient digital systems and contribute to the overall advancement of low-power circuit design methodologies.

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